



AEROSPACE STANDARD

AS6171™/11

Issued

2016-10

Techniques for Suspect/Counterfeit EEE Parts Detection by Design Recovery Test Methods

RATIONALE

This document was created to provide guidelines for the application of Design Recovery and to define the compliance requirements for laboratories using this technique. Additionally, this document is intended to provide guidance for those unfamiliar with Design Recovery and its application to detection of counterfeit electronic parts. This technique can be used for any risk level as needed to support results from other analysis techniques.

INTRODUCTION

Design Recovery is a destructive process used to obtain design information directly from a microcircuit. In the context of counterfeit detection this method could allow for the determination of whether the recovered design information of a microcircuit matches the intended function or physical layout of a known "good" or "control" sample or matches the original design. This method can be applied to detecting changes in the microcircuit intended function through analysis of the physical layout of the circuit. These changes may be either non-malicious or unintentional, or they may be intentionally malicious (Trojan circuitry), such as a kill switch or to enable unauthorized access to the device or the product in which the device is used. Examples of physical defects which are indicators of a possible counterfeit device for which design recovery is particularly well suited include: wrong die, missing and/or misaligned contact window, parasitic transistors, cracks and other imperfections in a silicon die or passivation layer or electromigration. However, it must be noted that circuits with the same functional behavior may have different physical design either due to a revised design, newer technology or different implementations of the same functional behavior from different manufacturers and therefore may not be counterfeit.

This procedure requires the availability of either a known authentic sample or information on the design of the device.

This document is focused on Design Recovery as it pertains to microcircuits, although it can be related to other electronic products such as discrete semiconductor devices or electronic devices with embedded microcircuits. The technique is a fundamentally destructive technique that requires decapsulation and removal of the silicon die from its packaging. The procedure outlined in this document assumes the design information is recovered from a silicon die, a layer at a time by sequential imaging and layer removal, thus recovering the original layout information used to manufacture the microcircuit. This approach ensures all the circuit design information can be captured, if required, so any "hidden" function is not missed. Non-destructive techniques are being researched and may be available in the future.

Depending on the complexity of the microcircuit under investigation and the required level of analysis required, Design Recovery can be an extremely time consuming and complex process; therefore, it may only be practical for microcircuits with a Critical Risk Level.

A microcircuit is removed from its packaging and sequentially each circuit layer is imaged and then removed so that the original design can be reconstructed. Potential applications of Design Recovery for counterfeit detection include microcircuit die-level authentic sample or design comparison to assess possible design modifications.

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1. SCOPE

This method outlines the requirements, capabilities, and limitations associated with the application of Design Recovery for the detection of counterfeit electronic parts including: Operator training; Sample preparation; Imaging techniques; Data interpretation; Design/functional matching; Equipment maintenance and; Reporting of data. The method is primarily aimed at analyses performed by circuit delayering and imaging with a scanning electron microscope or optical microscope; however, many of the concepts are applicable to other microscope and probing techniques to recover design data. The method is not intended for the purpose of manufacturing copies of a device, but rather to compare images or recover the design for determination of authenticity.

If AS6171/11 is invoked in the contract, the base document, AS6171 General Requirements shall also apply.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this document to the extent specified herein. The latest issue of SAE publications shall apply. The applicable issue of other publications shall be the issue in effect on the date of the purchase order. In the event of conflict between the text of this document and references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2.1.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or +1 724-776-4970 (outside USA), www.sae.org.

AS6171	Test Methods Standard: General Requirements, Suspect/Counterfeit Electrical, Electronic, and Electromechanical Parts
AS6171/4	Techniques for Suspect/Counterfeit EEE Parts Detection by Delid/Decapsulation Physical Analysis Test Methods

2.1.2 Other Publications

ANSI/ESD S20.20	Protection of Electrical and Electronic Parts, Assemblies and Equipment
ANSI/ISO/IEC 17025:2000	General Requirements for the Competence of Testing and Calibration Laboratories
IDEA-STD-1010	Acceptability of Electronic Components Distributed in the Open Market
IPC/JEDEC J-STD-020	Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
IPC/JEDEC J-STD-033	Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices
JESD-625	Requirements for Handling Electrostatic Discharge Sensitive (ESD) Devices

2.2 Terms and Definitions

All terms that require definition are defined in the paragraph in which they are first used.

2.3 Acronyms

See 2.3 of AS6171 General Requirements.