



TECHNICAL REPORT

GEIA-STD-0005-2™

REV. B

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Superseding GEIA-STD-0005-2A

(R) Standard for Mitigating the Effects of Tin Whiskers in
Aerospace, Defense, and High Performance Electronic Systems

RATIONALE

SAE GEIA-STD-0005-2B was revised to incorporate the knowledge accrued from managing tin whisker risks using lead (Pb)-free materials in aerospace, defense, and high-performance (ADHP) soldered electronic products and to comply with the SAE Five-Year Review policy.

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INTRODUCTION

In 2002, the European Union enacted two regulations: 2002/95/EC Restriction of Hazardous Substances (RoHS) and 2002/96/EC Waste Electrical and Electronic Equipment (WEEE). These and other government regulations on the use of lead (Pb) have resulted in a global transition to Pb-free electronics, particularly in the commercial electronics sector.

The aerospace and defense electronics sectors (and some other high-performance sectors) have been more cautious in the adoption of Pb-free technologies for several reasons: stringent reliability requirements (e.g., safety critical or security critical applications), long service life, complex and harsh environments, and sustainment (i.e., existing SnPb products may require repair/rework). Pb-free materials require characterization for use in ADHP operational environments.

Given the commercial electronics transition to Pb-free, there are certain incentives for ADHP products and systems to transition to Pb-free materials. These incentives include the use of commercial-off-the-shelf (COTS) assemblies, the need to use new electronic package styles, availability, and affordability.

SAE G-24 and IPC PERM were formed by the aerospace and defense industry to develop standards, handbooks, and guidelines to manage the risks of transitioning to Pb-free technology. The GEIA-STD/HBK-0005 suite of documents, as well as documents released by IPC such as IPC/PERM-2901, are the approaches developed and recommended by these committees. While this suite of documents was primarily developed by the aerospace and defense industry, the techniques are applicable to any ADHP product needing mitigation to Pb-free material risks.

The restriction of Pb use generated a transition by many piece part and board suppliers from tin-lead (SnPb) finishes to pure tin or other Pb-free finishes. Pb-free tin finishes can be susceptible to the spontaneous growth of crystal structures known as “tin whiskers,” which can cause electrical failures. These whiskers can cause shorts, which may be intermittent or permanent depending on the electrical conditions. In some cases, they have caused catastrophic arcing events (see definition of Metal Vapor Arc below). They can also serve as a source of foreign object debris (FOD) and may interfere with sensitive optical surfaces or the movement of micro-electromechanical system (MEMS) structures. Though studied and reported for decades, the mechanism behind their growth is not well understood, and tin whiskers remain a potential reliability hazard. Furthermore, the growing number of piece parts with pure tin finishes means there are more opportunities for whiskers to grow and to produce failures.

The nature and meaning of “risk” posed by tin whiskers may vary considerably across the range of users of this standard. As in any assessment of risk, the probability and consequence of occurrence and failure must be considered in each application. Potential whisker failure modes for a particular hardware or system application must be carefully considered when making the determination of which mitigations to apply. For example, whisker-prone piece parts on a circuit card used in a system that is under frequent or continual power may only incur parametric deviations or interrupts as individual whiskers grow and short to an adjacent lead. On the other hand, the same circuit card employed in a space program could grow many long whiskers without an opportunity to repair or replace. For the purposes of this standard, risk refers to the chance and consequence of a failure due to a whisker, not just the chance of the presence of a whisker.

1. SCOPE

This standard establishes processes for performing and documenting mitigation steps taken to reduce the harmful effects of tin whiskers in electronic systems for ADHP applications. This includes electronic piece parts and mechanical hardware that are used on or in the proximity of electronics.

This document identifies the requirements for mitigating the effects of tin whiskers applicable to the requirements of the SAE GEIA-STD-0005-1 Lead-free Control Plan (LFCP). An LFCP documents the specific Pb-free materials and assembly processes the LFCP owner will use to eliminate or mitigate the Pb-free risks to assure customers that their ADHP soldered electronic products will meet the applicable reliability requirements of the customer. This standard may also be used independently of SAE GEIA-STD-0005-1.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this document to the extent specified herein. The latest issue of SAE publications shall apply. The applicable issue of other publications shall be the issue in effect on the date of the purchase order. In the event of conflict between the text of this document and references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2.1.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (U.S. and Canada only) or +1 724-776-4970 (outside U.S. and Canada), www.sae.org.

EIA-933	Requirements for a COTS Assembly Management Plan
GEIA-STD-0005-1	Standard for Developing a Lead-Free Control Plan to Manage the Risks of Lead-Free Solders and Finishes in Aerospace, Defense, and High-Performance Soldered Electronic Products
GEIA-STD-0006	Requirements for Using Robotic Hot Solder Dip to Replace the Finish on Electronic Piece Parts

2.1.2 ANSI Publications

Copies of these documents are available online at <https://webstore.ansi.org>.

ANSI/ESD S20.20	Protection of Electrical and Electronic Parts
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2.1.3 Global Electronics Association Publications

Available from Global Electronics Association, 3000 Lakeside Drive, 105 N, Bannockburn, IL 60015, Tel: 847-615-7100, www.electronics.org.

IPC-CC-830	Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies
IPC-HDBK-001	Handbook and Guide to Supplement J-STD-001
IPC-J-STD-001	Requirements for Soldered Electrical and Electronic Assemblies
IPC/PERM-WP-022	Mitigation of Pure Tin Risk by Tin-Lead SMT Reflow - Results of an Industry Round-Robin - Final Report
IPC-TR-587	Conformal Coating Material and Application "State of the Industry" Assessment Report

2.1.4 IEC Publications

Available from IEC Secretariat, 3 rue de Varembe, PO Box 131, CH-1211 Geneva 20, Switzerland, Tel: +41 22 919 0211, www.iec.ch.

IEC 61086	Coatings for loaded printed wire boards (conformal coatings)
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2.1.5 JEDEC Publications

Available from JEDEC, 3103 10th Street North, Suite 240S, Arlington, VA 2201, www.jedec.org.

J-STD-002	Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
J-STD-006	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solder for Electronic Soldering Applications

- JESD201 Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes
- JESD213 Standard Test Method Utilizing X-ray Fluorescence (XRF) for Analyzing Component Finishes and Solder Alloys to Determine Tin (Sn) - Lead (Pb) Content
- JESD22-A121 Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes

2.1.6 NASA Technical Standards Program Publications

Copies of these documents are available online at <https://standards.nasa.gov>.

- NASA-STD-8739.1 Workmanship Standard for Staking and Conformal Coating of Printed Wiring Boards and Electronic Assemblies

2.1.7 U.S. Government Publications

Copies of these documents are available online at <https://quicksearch.dla.mil>.

- MIL-I-46058 Insulating Compound, Electrical (for Coating Printed Circuit Assemblies)
- MIL-STD-202 Electronic and Electrical Component Parts
- MIL-STD-750 Test Methods for Semiconductor Devices
- MIL-STD-883 Microcircuits
- MIL-STD-1580 Destructive Physical Analysis for Electronic, Electromagnetic, and Electromechanical Parts

2.2 Related Publications

The following publications are provided for information purposes only and are not a required part of this SAE Technical Report.

2.2.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (U.S. and Canada only) or +1 724-776-4970 (outside U.S. and Canada), www.sae.org.

- ARP6415 Use of Pb-Free Ball Grid Array Component Soldered Using SnPb Solder
- ARP6537 Risk Mitigation for Pb-Free Solders Used Internally to Parts
- GEIA-HB-0005-1 Program Management/Systems Engineering Guidelines for Managing the Transition to Lead-free Electronics
- GEIA-HB-0005-2 Technical Guidelines for Aerospace and High Performance Electronic Systems Containing Lead-free Solder and Finishes
- GEIA-HB-0005-3 Rework/Repair Handbook to Address the Implications of Lead-Free Electronics and Mixed Assemblies in Aerospace and High Performance Electronic Systems
- GEIA-STD-0005-3 Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes

2.2.2 Global Electronics Association Publications

Available from Global Electronics Association, 3000 Lakeside Drive, 105 N, Bannockburn, IL 60015, Tel: 847-615-7100, www.electronics.org.

IPC/JEDEC J-STD-609 Marking and Labeling of Components, PCBs and PCBAs to Identify Lead (Pb), Pb-Free and other Attributes

IPC-PERM-2901 Pb-free Design & Assembly Implementation Guide

IPC-SPV-WP-006 Round Robin Testing and Analysis - Lead-free Alloys - Tin, Silver, and Copper

2.2.3 IEC Publications

Available from IEC Secretariat, 3 rue de Varembe, PO Box 131, CH-1211 Geneva 20, Switzerland, Tel: +41 22 919 0211, www.iec.ch.

IEC TS 62647-4:2018 Process Management for Avionics - Aerospace and Defence Electronic Systems Containing Lead-Free Solder - Part 4: Ball Grid Array (BGA) Reballing

2.2.4 Other Publications

See Appendix H for the complete list of references cited in this document.

2.3 Definitions

For the purposes of this standard, the following terms and definitions apply:

ASSEMBLIES: Electronic items that require electrical attachments, including soldering of wires or component terminations; examples include circuit cards assemblies (CCA) and wire harnesses. This may include soldered assemblies.

BUS BAR: A solid conduit, other than insulated wires and cables, that is used for distributing electrical energy.

CONTROL LEVEL: Details the amount of attention that should be paid to the risk of tin whiskers: no restrictions on Pb-free tin finish use, some restrictions on Pb-free tin finish use, and prohibition of Pb-free tin finish use.

CONFORMAL COAT: An insulating protective covering that conforms to the configuration of the objects coated (e.g., circuit cards) providing a protective barrier against deleterious effects from environmental conditions. This includes organic and ceramic coatings and traditional and ultra-thin coatings, but not pottings and encapsulations.

COTS (COMMERCIAL OFF-THE-SHELF PRODUCTS): One or more pieces, mechanical or electrical, developed for multiple commercial consumers and are generally available without any tailoring and whose design and/or configuration is controlled by the supplier's specification or an industry standard. They can include piece parts, subassemblies, or top-level assemblies.

CRITICAL: Item or function, if defective, will result in the system's inability to retain operational capability, meet primary objective, or affect safety.

CUSTOMER: Refers to an entity or organization that (a) integrates a piece part, soldered assembly, unit, or system into a higher level system, (b) operates the higher level system, or (c) certifies the system for use. For example, this may include end item users, integrators, regulatory agencies, operators, original equipment manufacturers (OEMs), and subcontractors.

EDS: Energy Dispersive (X-ray) Spectroscopy, a method for material composition analysis.

ENCAPSULATION: The introduction of an insulating material that fully coats and adheres to the tin surfaces and all adjacent conductive surfaces and is intended to completely fill the space in between the conductive surfaces without voids or bubbles. This material is typically liquid during processing but hardens into a solid and remains solid over the design life of the product. Materials that coat the surfaces but do not fill the space in between are defined as coatings, not encapsulations.

FINISH: The outermost surface layer or distinct layers such as underplates. This includes all leads and package surfaces, even those coated, encapsulated, or otherwise not exposed. It applies to the outermost layer and underplates of electrical piece parts, mechanical piece parts, and boards.

FOREIGN OBJECT DEBRIS (FOD): Any object, particle, or substance that is not intended to be present on or in the product or environment with a potential to cause damage or failure.

GAP: Minimum line of sight distance between Pb-free tin-finished surface and the nearest adjacent conductor at a different electrical potential. It refers to any conductors (leads, pads, connectors, contacts, or others). Thus, the lead thickness and spacing need to be considered in the calculation. It may be determined by design drawings or physical measurement.

HIGH-PERFORMANCE SYSTEM OR PRODUCT: Requires continued high performance or performance on-demand, or equipment downtime cannot be tolerated, or end-use environment may be uncommonly harsh and the equipment must function when required, such as life support or other critical systems.

METAL VAPOR ARC: A low impedance plasma event between a metal surface and another surface potential. If the ions collide with the cathode with enough vigor, then substantial amounts of metal erupt from the cathode, as a gas, into the plasma, where this gas ionizes, thus sustaining the plasma.

MITIGATION: A method to reduce the risk or consequence of a failure. Mitigations do not drive risk to zero. It may impact either the risk or the consequence is reduced. It does not mean that the mitigation is effective permanently.

Pb-FREE TIN: Pure tin or any tin alloy with <3% Pb content by weight. This means that some Pb-free finishes other than pure tin, such as tin-bismuth and tin-copper, are considered to be "Pb-free tin" for the purposes of this standard. Many of these alloys have not been assessed for whiskering behavior. Note that this definition is different than the typical electronic industry definition of Pb-free, based on RoHS, which would require <0.01% Pb for RoHS compliance.

PIECE PART: An electronic component that is not normally disassembled without destruction. This includes electronic components (such as integrated circuits, capacitors, and connectors) and mechanical elements (such as washers, card guides, and shields).

PLASMA EVENT: An electrical event that creates an ionized (conductive) cloud emanating from a thermally hot source with a continuous electrical power source.

POTTING: A process that involves the surrounding of a component(s) or an assembly in a container with a liquid resin which is then cured in place. The container usually becomes an integral part of the system such that the critical property that needs to be maintained is the interfacial adhesion between the cured system and the container substrate and critical components for an optimum long-lasting and reliable package.

REWORK: The act of reprocessing non-complying articles through the use of original or equivalent processing in a manner that assures full compliance of the article with applicable drawings or specifications.

REPAIR: The act of restoring the functional capability of a defective article in a manner that precludes compliance of the article with applicable drawings or specifications.

RISK: Used with regard to the probability of a failure due to a tin whisker. It is not used with regard to the risk of the presence of a whisker or nodule.

SHALL: Indicates a mandatory requirement to be followed in order to conform to this standard.

SHOULD: Indicates that, among several possibilities, one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is discouraged but not prohibited.

SUBCONTRACTOR: An organization, within the given high-reliability industry, that supplies, maintains, repairs, or supports electronic systems and is not the direct supplier to the customer or user of those systems.

SUPPLIER: An entity or organization that designs, manufactures, repairs, or maintains a piece part, unit, or system. For example, this includes original equipment manufacturers (OEMs), repair facilities, subcontractors, and piece part manufacturers. In some cases, a single organization may be both a customer and a supplier. They should follow the requirements for suppliers when addressing their customer's contracts and should follow the requirements for customers when flowing down requirements to their lower-tier suppliers.

SYSTEM: One or more units that perform electrical function(s).

TIN WHISKER: A spontaneous crystal growth that emanates from a tin-rich finish. They may be cylindrical, kinked, or twisted. Typically, they have an aspect ratio (length/width) greater than two, with shorter growths referred to as nodules or odd-shaped eruptions.

UNIT: One or more assemblies within a chassis to perform electrical function(s).

XRF: X-ray fluorescence, a method for material composition analysis.

3. REQUIREMENTS

3.1 Control Level Selection

The requirements in this document are driven by a CCA's, module's, or assembly's tin whisker Control Level. It is important that the Control Level be evaluated for individual CCA, module, or assembly or particular class (such as by the module's criticality). The Control Level should be consistent with the overall risk strategy for that CCA, module, or assembly. See [3.1.1](#) for more information.

Higher Control Levels impose tighter controls and thereby reduce exposure to tin whisker risk. However, tin whisker risks are just one of many types of risks associated with component selection and assembly design. Controls imposed on tin whiskers should be commensurate with controls imposed to manage other risks. Decisions about Control Levels are cost-risk decisions that should be evaluated for each program and product.

Some questions to consider during Control Level selection are:

- What are the consequences of performance anomalies in the system?
- Is it anticipated that the tin whiskers will produce a plasma event?
- Do local anomalies affect top-level system performance?
- Could a whisker failure cause critical system level failure?
- Are anomalies detectable and repairable?

More information on how these questions can be used to select an appropriate Control Level is provided in Appendix A.

Overall, there are three approaches to tin whisker control:

- Whisker Risk Acceptance
- Whisker Risk Mitigation
- Whisker Avoidance by Tin Prohibitions

Different Control Levels represent different emphasis on each of these approaches.

- Control Level 1: Under Control Level 1, tin whisker risks are accepted. Those risks are managed by selecting and purchasing piece parts, CCAs, assemblies, and modules with best commercial practices for tin whisker control.
- Control Level 2: Under Control Level 2, Pb-free tin finishes are sometimes acceptable. Tin whisker risk is managed primarily by a combination of avoidance and mitigations, including design rules. For all Control Level 2 categories, it is expected that the supplier will actively apply mitigations. The level of validation will vary between Control Levels 2A, 2B, and 2C. If only Control Level 2, with no sub-level, is identified in a control document, the default Control Level is assumed to be Level 2A.
 - Control Level 2A: Under Control Level 2A, tin whisker risks are managed primarily through the acceptance of tin whisker risk and to a lesser extent upon the use of mitigations. At least one mitigation is required, but it has limited requirements on validating the quality and consistency of the mitigation.
 - Control Level 2B: Under Control Level 2B, tin whisker risks are managed primarily through the use of mitigations, including design rules, and to a lesser extent upon Pb-free tin finish avoidance. Validation of the quality of the mitigations is required with limited requirements for periodic inspection.
 - Control Level 2C: Under Control Level 2C, tin whisker risks are managed primarily by prohibiting Pb-free tin finishes, to a lesser extent through specific application of mitigations, and in exceptional cases by design rules. This level requires more rigorous validation of the mitigations to ensure they are effective.
- Control Level 3: Tin whisker risks are managed strictly by prohibiting Pb-free tin finishes. This Control Level is for CCAs, modules, and assemblies where failures cannot be tolerated and is most commonly used on systems that cannot be repaired in its final location or environment or in situations where a metal vapor arc or plasma event is likely if a whisker fuses.

The customer is responsible for determining the Control Level they are seeking and identifying the Control Level in their Request for Proposal (RFP) and/or contract when this standard is imposed. When bidding on a design, the supplier shall clearly state the Control Level(s) for the product in their response and LFCP (or other Parts, Materials, and Process [PMP] documentation if a full LFCP is not required). If a Control Level is not explicitly stated in the RFP or other customer requirements, approval of the supplier's LFCP and/or PMP document constitutes agreement of the customer to the Control Level documented by the supplier.

Many suppliers will have a baseline Control Level for their standard product and processes. This will be reflected in their LFCP.

Appendix A provides additional guidance on Control Level selection.

3.1.1 Control Levels and Levels of Integration

Control Levels were designed to be applied at the CCA, module, or assembly level. It is not uncommon for systems to have CCAs, modules, and assemblies at different Control Levels depending on their characteristics.

Customers may want to have an approach to Control Level selection at the subsystem, product, or system level. Some approaches at higher levels of integration and in system Pb-Free Control Plans (LFCPs) include:

- Define the criteria to be used to evaluate CCA, module, or assembly Control Levels, preferably with some general statements about expected baseline Control Levels.
- Define Control Levels based on CCA, module, or assembly criticality, function, or some other design rule.
- Define the system level Control Level based on the expected Control Level of most CCAs, modules, and assemblies and define when the program will require higher Control Levels. A discussion of this process for requiring higher or allowing lower Control Levels, with supporting data, should be included.

3.1.2 COTS and Control Level Selection

The imposition of Control Levels 2C or 3 will generally preclude the use of COTS assemblies. This is due to the difficulties in assuring that COTS assemblies will meet the rigorous requirements of Control Levels 2C and 3. Control Level 2B may also be challenging to implement if inspection of all assemblies in the COTS item is not possible. It should be recognized that:

- COTS assemblies do not allow the same control and visibility into the parts selection process or manufacturing process as non-COTS assemblies.
- COTS assembly manufacturers may make changes to their components, finishes, solders, and other manufacturing processes without notification to their customers.
- COTS require many other evaluations and mitigations beyond tin whisker mitigation (refer to EIA-933).

If COTS assemblies are used in a CCA, module, assembly, or system that requires Control Level 2C or 3, then at least one of the following **shall** be implemented:

- a. COTS assemblies can be identified as exceptions to the Control Level requirement.
- b. Execution of a comprehensive material control and analysis plan consistent with the Control Level of the program.
- c. Flowing down the Control Level requirements to a COTS supplier who is willing to modify their standard product.

For Control Levels 1, 2A, and 2B, it is possible that a COTS assembly may meet the requirements of the level. For example, if a COTS assembly is conformally coated by design but the quality of the conformal coat cannot be examined, it would likely only be able to meet the requirements of Control Level 2A but not 2B. The ability to determine if a COTS assembly can meet any Control Level in this standard is dependent on the amount of information available from the COTS supplier. If insufficient information is available to show that a COTS assembly or module meets any of the levels, it should be identified as not meeting the standards and treated as an exception to the requirement to use this standard.

COTS piece parts, as opposed to COTS assemblies, are likely to be acceptable for any Control Level but should be evaluated on a periodic basis. COTS suppliers have been known to change part finish without notification or a change in part number.

3.2 Requirements for Control Levels

If a program has a requirement to comply with this standard and cannot meet the minimum requirements for any Control Level, a nonconformance, deviation, or waiver (per program process) shall be required.

3.2.1 Control Level 1 Requirements

3.2.1.1 Control Level 1 Requirements for Documentation of Uses of Pb-Free Tin Finishes

No requirements.

3.2.1.2 Control Level 1 Requirements for Detecting and Controlling Pb-Free Tin Finish Introduction

No requirements.

3.2.1.3 Control Level 1 Requirements for Tin Whisker Risk Mitigation

The supplier **shall** apply at least one of these sets of mitigations to their CCA, module, or assembly complying with all elements of the selected set(s):

- a. All piece parts have passed JESD201. There is a minimum spacing of at least 6 mm between Pb-free tin-finished mechanical hardware and exposed electrical conductors. The design has been reviewed to confirm there is no use of Pb-free tin-finished, non-insulated (bare) bus bars.
- b. All electronic piece parts are installed using SnPb solder attached to printed wiring boards. There is a minimum spacing of at least 6 mm between Pb-free tin-finished mechanical hardware and exposed electrical conductors. The design has been reviewed to confirm that there is no use of Pb-free tin-finished, non-insulated (bare) bus bars.
- c. All electronics are conformally coated. The design has been reviewed to confirm there is no use of Pb-free tin-finished, non-insulated (bare) bus bars. (The difference between this option and Control Level 2A with conformal coat is that for Control Level 1 there is no requirement for analyzing or documenting the conformal coat process.)
- d. There is a reliability analysis based on warranty or other field data on the EXACT product that exceeds the reliability and lifetime requirements for the application. This analysis will be available to customers when requested.
- e. There is a reliability analysis based on warranty or other field data on SIMILAR product that exceeds the reliability and lifetime requirements for the application, and there is a minimum spacing of at least 6 mm between Pb-free tin-finished mechanical hardware and exposed electrical conductors. The analysis will be available to customers when requested. The design has been reviewed to confirm that there is no use of Pb-free tin-finished, non-insulated (bare) bus bars.
- f. There is an analysis showing that the impact of failure of the CCA, module, or assembly to the system and program is tolerable. This analysis will be available to customers when requested.
- g. Other tin whisker mitigation approaches as agreed to by the customer.

3.2.1.4 Control Level 1 Documentation Requirements

Process documentation is not required to be available. However, objective evidence of what mitigation from 3.2.1.3 was fulfilled shall be available when requested.

3.2.2 Control Level 2A Requirements

3.2.2.1 Control Level 2A Requirements for Documentation of Uses of Pb-Free Tin Finishes

The customer is responsible for listing any applications where Pb-free tin finishes are not allowed.

3.2.2.2 Control Level 2A Requirements for Detecting and Controlling Pb-Free Tin Finish Introduction

There are no detection or material analysis requirements for Control Level 2A.

3.2.2.3 Control Level 2A Requirements for Tin Whisker Risk Mitigation

The supplier **shall** ensure both design rules below are applied:

1. A minimum spacing of at least 6 mm between pure tin-finished mechanical hardware and exposed electrical conductors
2. A prohibition of Pb-free tin-finished, non-insulated (bare) bus bars

In addition, Control Level 2A CCAs, modules, and assemblies **shall** have at least one of the following mitigations:

- a. Hard potting or encapsulation (see 4.3.1)
- b. Physical barriers (see 4.3.2)
- c. Circuit design and analysis showing low impact of tin whisker short or FOD (see 4.3.6)
- d. Circuit design and analysis showing that areas sensitive to tin whisker shorts or FOD have at least a 1-cm gap (see 4.3.6)
- e. Use of conformal coat and SnPb soldering to achieve full coverage of the Pb-free tin by at least one method (no validation required) (see 4.3.5)
- f. Use of conformal coat with one-time nondestructive coverage validation (see [4.3.3](#))
- g. SnPb soldering process with one-time nondestructive XRF validation to confirm full coverage of the entire Pb-free tin surface (see [4.3.4](#))
- h. Piece parts that have passed JESD201 are used in an application that is conformally coated (without a required validation)
- i. Mitigation or combination of mitigations approved by the customer

If the application voltage is greater than 20 V, the piece part level current is greater than 1 A, and the application is not current limited, the risk of a metal vapor arc may be significant. It is recommended that Pb-free tin be refinished per GEIA-STD-0006 or equivalent. If the piece parts are not refinished, any use of mitigations under these high voltage conditions **shall** have a corresponding risk assessment approved by the customer (see Section F.4).

3.2.2.4 Control Level 2A Documentation Requirements

All processes used for tin whisker mitigation **shall** be controlled and documented and made available to the customer when requested (although nondisclosure agreements or limitation on how those processes are shared may be required).

3.2.2.5 Control Level 2A Exceptions

If specific piece parts, CCAs, soldered assemblies, modules, or applications not allowing tin are required to meet a higher Control Level, these requirements **shall** be specified in contractual and design documents.

3.2.3 Control Level 2B Requirements

3.2.3.1 Control Level 2B Requirements for Documentation of Uses of Pb-Free Tin Finishes

The supplier **shall** have a process by which they can identify all possible uses, including alternates, of Pb-free tin-finished parts, including the CCAs, modules, and assemblies where they are used and the mitigation applied, and provide that data upon request.

The customer is responsible for listing any applications where Pb-free tin finishes are not allowed.

3.2.3.2 Control Level 2B Requirements for Detecting and Controlling Pb-Free Tin Finish Introduction

The supplier **shall** perform part and material identification through XRF or other material analysis technique prior to assembly qualification or document that all parts (regardless of their finish) have mitigation applied at the assembly level, consistent with 3.2.3.3. Additional sample monitoring through a mixture of periodic material analyses and/or reviews of documentation by suppliers is recommended.

The supplier **shall** provide a plan for flowing the requirement to lower-tier suppliers in accordance with [4.1](#), if applicable.

3.2.3.3 Control Level 2B Requirements for Tin Whisker Risk Mitigation

The supplier **shall** ensure that both design rules below are applied:

1. A minimum spacing of at least 1 cm between pure tin-finished mechanical hardware and exposed electrical conductors
2. A prohibition of Pb-free tin-finished, non-insulated (bare) bus bars

In addition, Control Level 2B CCAs, modules, and assemblies **shall** have at least one of the following mitigations:

- a. Hard potting or encapsulation (see 4.3.1)
- b. Physical barriers (see 4.3.2)
- c. Circuit design and analysis showing low impact of tin whisker short or FOD (see 4.3.6)
- d. Circuit design and analysis showing that areas sensitive to tin whisker shorts or FOD have at least a 1-cm gap (see 4.3.6)
- e. Conformal coat with appropriate gap size with one-time destructive inspection and annual nondestructive inspection (see [4.3.3](#))¹
 1. Parylene conformal coating (type XY as per IPC-CC-830) requires worst-case (or sample-based measurements) gap size, before coating, greater than or equal to 150 µm (5.9 mil).
 2. Conformal coating of types AR, ER, SR, or UR (as per IPC-CC-830) requires worst-case (or sample-based measurements) gap size, before coating, greater than or equal to 250 µm (9.8 mil).
 3. Conformal coating of other types not listed above shall not be used for tin whisker mitigation.
- f. Pb-free tin electronic components with gaps greater than 2000 µm (78.7 mil) that have been installed with SnPb and are physically isolated from any Pb-free tin mechanical piece parts (see [4.3.4](#)).
- g. SnPb soldering process with one-time destructive and annual nondestructive inspection to confirm full coverage of the entire Pb-free tin surface (see [4.3.4](#)).
- h. SnPb soldering process and conformal coat with a one-time destructive inspection to confirm full coverage of the entire Pb-free tin surface by at least one method (see [4.3.5](#)).

NOTE: There are no gap size requirements when both mitigations are applied and no periodic nondestructive inspections so long as there is documentation of well-controlled processes for both SnPb soldering process and conformal coat.

- i. Mitigation or combination of mitigations approved by the customer.

If the application voltage is greater than 20 V, the piece part level current is greater than 1 A, and the application is not current limited, the risk of a metal vapor arc may be significant. It is recommended that Pb-free tin be refinished per GEIA-STD-0006 or equivalent. If the piece parts are not refinished, any use of mitigations under these high-voltage conditions shall have a corresponding risk assessment (see Section F.4).

¹ If the gap size is smaller than these requirements, a different mitigation method, such as option h, should be chosen, or the parts should be solder dipped consistent with GEIA-STD-0006.

3.2.3.4 Control Level 2B Process Documentation Requirements

All processes used for tin whisker mitigation **shall** be controlled and documented and made available to the customer when requested (although nondisclosure agreements or limitation on how those processes are shared are expected).

For mitigations requiring validation, test and analysis reports summarizing those validations **shall** be made available to the customer when requested, including documentation of both initial and periodic validations, consistent with the requirements in [Section 4](#).

If there are unmitigated finishes (because they are believed to not be Pb-free tin), see the requirement for detection of Pb-free tin in [3.2.3.2](#).

3.2.4 Control Level 2C Requirements

3.2.4.1 Control Level 2C Requirements for Documentation of Uses of Pb-Free Tin Finishes

For practical reasons, the supplier should avoid use of Pb-free tin finishes whenever possible.

The supplier **shall** have a process by which they can identify all possible uses, including alternates, of Pb-free tin-finished parts, including the CCAs, modules, and assemblies that are used and the mitigation applied, and provide that data upon request.

3.2.4.2 Control Level 2C Requirements for Detecting and Controlling Pb-Free Tin Finish Introduction

The supplier **shall** provide a plan for monitoring materials in their product in accordance with [4.2](#).

For critical piece parts, assemblies, or systems, the plan should include sampling at least one piece part per lot unless the applications have been approved to allow Pb-free finishes.

The supplier **shall** provide a plan for flowing the requirements to lower-tier suppliers in accordance with [4.1](#).

3.2.4.3 Control Level 2C Requirements for Tin Whisker Risk Mitigation

The supplier **shall** ensure that both design rules below are applied.

1. A prohibition on pure tin-finished mechanical hardware that are not physically isolated from exposed electronic hardware
2. A prohibition of Pb-free tin-finished, non-insulated (bare) bus bars

In addition, Control Level 2C CCAs, modules, and assemblies **shall** have at least one of the following mitigations:

- a. Hard potting or encapsulation (see [4.3.1](#))
- b. Physical barriers (see [4.3.2](#))
- c. Circuit design and analysis showing low impact of tin whisker short or FOD (see [4.3.6](#))
- d. Conformal coat with appropriate gap size with one-time destructive inspection and annual nondestructive inspection (see [4.3.3](#))
 1. Parylene conformal coating (type XY as per IPC-CC-830) requires worst-case (or sample-based measurements) gap size, before coating, greater than or equal to 150 µm (5.9 mil)
 2. Conformal coating of types AR, ER, SR, or UR (as per IPC-CC-830) require worst-case (or sample-based measurements) gap size, before coating, greater than or equal to 250 µm (9.8 mil).
 3. Conformal coating of other types not listed above shall not be used for tin whisker mitigation.

- e. SnPb soldering process with one-time destructive inspection and annual nondestructive inspection to confirm full coverage of the entire Pb-free tin surface (see [4.3.4](#)).
- f. SnPb soldering process and conformal coat with one-time destructive inspection and annual nondestructive inspection to confirm full coverage of the entire Pb-free tin surface (see [4.3.5](#)). For parts with gap size less than 250 µm, the one-time destructive inspection and annual nondestructive inspection shall show complete SnPb solder, regardless of conformal coat coverage.
- g. Mitigation or combination of mitigations approved by the customer

If the application voltage is greater than 20 V, the piece part level current is greater than 1 A, and the application is not current limited, the risk of a metal vapor arc may be significant. It is recommended that Pb-free tin be refinished per GEIA-STD-0006 or equivalent. If the piece parts are not refinished, any use of mitigations under these high-voltage conditions shall have a corresponding risk assessment (see Section F.4).

3.2.4.4 Control Level 2C Process Documentation Requirements

All processes used for tin whisker mitigation **shall** be controlled and documented and made available to the customer when requested (although nondisclosure agreements or limitation on how those processes are shared are expected).

For mitigations requiring validation, test and analysis reports summarizing those validations **shall** be made available to the customer when requested, including documentation of both initial and periodic validations, consistent with the requirements in [Section 4](#).

If there are unmitigated elements of the assembly, see the requirement for detection of Pb-free tin in [3.2.3.2](#).

3.2.5 Control Level 3 Requirements

3.2.5.1 Control Level 3 Requirements for Documentation of Uses of Pb-Free Tin Finishes

Pb-free tin finish shall not be allowed.

Any use of Pb-free tin finish would represent a violation of requirements, which would require a waiver process based on program requirements, including risk management requirements. No Pb-free tin finishes should be designed into the product or knowingly purchased without a plan to replace the finish. There will be cases where errors will be made in the finish determination or in the application of mitigation methods. Customers and suppliers should have processes in place to document and assess the impact of these errors. Already existing deviation or waiver processes may be acceptable when technical experts on tin whiskers are consulted.

3.2.5.2 Control Level 3 Requirements for Detecting and Controlling Pb-Free Tin Finish Introduction

The supplier **shall** monitor the material in their product per [4.2](#).

The supplier **shall** provide a plan for flowing the requirement to lower-tier suppliers per [4.1](#).

3.2.5.3 Control Level 3 Requirements for Mitigation of Tin Whisker Risk and Mitigation Effectiveness

Not applicable, as Pb-free tin finish is not allowed.

3.2.5.4 Control Level 3 Requirements for Parts Selection

Not applicable, as Pb-free tin finish is not allowed.

3.2.5.5 Control Level 3 Requirements for Assessment and Documentation of Risk and Mitigation Effectiveness

Not applicable, as Pb-free tin finish is not allowed.

If Pb-free tin finish is to be completely replaced through solder dipping or some other method, the process for qualifying and evaluating the replacement process and any secondary risks should be documented.

3.2.6 Requirements for Mitigating Tin Whisker Risk for Solder Joints

The majority of requirements in this standard apply to Pb-free tin finishes on piece parts, not Pb-free solders. Generally, the instance of tin whisker growing from solder joints is negligible. For Control Level 2, if the piece part being soldered does not require mitigation based on its finish, the use of Pb-free solder to attach the piece part to the printed wiring board does not introduce a requirement for mitigation.

For Control Level 3, all Pb-free solder joints **shall** be mitigated consistent with the mitigation requirements of Control Level 2B, regardless of the finishes on the piece parts. (Note that Pb-free part finishes are prohibited.)

The data on the dangers of tin whiskers growing from Pb-free *and* SnPb solders when there are rare earth elements (REE) present is sufficient to consider these solders a risk. For Control Levels 2 and 3, use of Pb-free or SnPb solder with intentionally alloyed REE, as discussed in J-STD-006, **shall** be disclosed to the customer and a risk assessment performed for tin whiskers.

Additional information and recommendations for preventing tin whiskers growing from Pb-free solder joints are presented in Appendix F.

4. IMPLEMENTATION METHODS

4.1 Flowing Requirements to Lower-Tier Suppliers (Applies to Control Level 2A, Control Level 2B, Control Level 2C, and Control Level 3)

Requirements for tin whisker control, analysis, and mitigation are applicable to all purchased and subcontracted elements and materials for the program. If Pb-free tin finishes are possible in the design, requirements for the Control Level **shall** be flowed to lower-tier suppliers or analysis **shall** be conducted on the purchased material to confirm that they will meet the Control Level applications after integration into the assembly.

4.2 Detecting and Controlling Pb-free Tin Finish Introduction

The use of screens to monitor Pb-free tin finish depends in part on the lot uniformity requirements. Many standard lot definitions do not address finishes, only internal features. The sampling or lot monitoring plan should take the finish uniformity requirements into consideration. When finish monitoring is required, it **shall** be applied to all piece parts, including electronic components (such as integrated circuits, capacitors, and connectors) as well as mechanical elements (such as washers, card guides, and shields) used within 6 mm of electrical conductors.

4.2.1 Sample Monitoring Plans (Applies to Control Level 2B and Control Level 2C)

A monitoring plan, including method of inspection, test, and sampling scheme, should be documented for Control Level 2B and **shall** be documented for Control Level 2C.

For Control Level 2B, the monitoring plan and sampling scheme should focus on critical hardware where Pb-free tin finish is not allowed.

For Control Level 2C critical hardware where approvals for use of Pb-free tin finish have not been obtained, the monitoring plan described in [4.2.2](#) should be used.

COTS piece parts may lack finish uniformity requirements and thus may require higher sample sizes during material identification testing.

If XRF is used for detection, the methods **shall** be consistent with JESD213 or MIL-STD-1580. Note that the two methods have different sample size and equipment requirements; either is acceptable. If EDS is used for detection, the methods **shall** be consistent with MIL-STD-1580. Other methods may be used with customer approval.

4.2.2 Lot Monitoring Requirements (Applies to Control Level 3)

The sample monitoring plan **shall** require testing each received lot or batch of items with metallic, unless otherwise specified by the customer. All tested finishes containing tin shall have minimum of 3% Pb by weight. The requirements for lot or batch uniformity should be documented to confirm that the monitoring plan is adequate. COTS piece parts may lack finish uniformity requirements and thus may require higher sample sizes during material identification testing. For hardware where the finish uniformity is not adequately addressed in lot or batch uniformity requirements, higher sample sizes should be required in the sample plan. The sample plan, and the finish uniformity requirements, **shall** be made available to the customer and should be agreed to by the supplier and the customer.

If XRF is used for detection, the methods **shall** be consistent with JESD213 or MIL-STD-1580. Note that the two methods have different sample size and equipment requirements, but either is acceptable. If EDS is used for detection, the methods **shall** be consistent with MIL-STD-1580. Other methods may be used with customer approval.

4.3 Methods for Mitigating Impact of Pb-Free Tin Finishes (Applies to Control Level 2A, Control Level 2B, and Control Level 2C)

Since the failure mechanisms for whisker growth are not fully understood, no single method is an assurance against whiskers in all applications, environments, and lifetimes. Mitigations, part selection, and analyses are all aspects of a general tin whisker risk mitigation system.

Mitigations selected for an application **shall** be reviewed to ensure that they do not cause secondary damage to the CCA, module, or assembly (e.g., reviewing coefficients of thermal expansion).

The following sections define the requirements for specific mitigations listed as options in [3.2.2.3](#), [3.2.3.3](#), and [3.2.4.3](#).

4.3.1 Hard Potting and Encapsulation

Potting and encapsulation can be a very effective means of reducing tin whisker risk. Materials used to meet the requirements of the hard potting and encapsulation mitigation **shall** be a material designed to be used as a potting or encapsulant (as opposed to be designed as a coating) and have at least one of the following:

- a. A filler (material, such as silica, to control thermal expansion and that also can serve as a barrier for tin whisker growth)
- b. An elastic modulus greater than 100 MPa after cure
- c. Hardness >75 durometer D
- d. Gap distance of at least 10 mil between the Pb-free tin surface and any other conductive surface (inside or outside encapsulant) using a material with hardness between 30 durometer A and 90 durometer A or between 10 durometer D and 75 durometer D
- e. Sufficient data or history to show affective coverage and whisker mitigation from delivered production hardware

For materials not meeting one of these requirements, see [4.3.3](#) on conformal coats.

For Level 2C, one-time validation of the potting and encapsulation process shall be performed on at least two representative pieces of hardware, showing both of the following:

- a. No voids greater than the minimum gaps size being mitigated by the potting or encapsulation, regardless of void location.
- b. No delamination between the potting material and surface or substrate allowed, including no evidence of either cohesive or adhesive separation.

This may be done using either acoustic microscopy, cross-sectioning, or other method shown to be effective for the application.

For potting or encapsulation to be effective, it needs to remain hard over the application temperature range and remain hard over the product life. Attention should be paid to the types of fillers, in addition to the matrix material. The process of forming the potting or encapsulation should ensure that it is unlikely to have voids or bubbles that would reduce its effectiveness at encapsulating whiskers. Issues such as induced stress, thermal mismatch, and outgassing should also be reviewed as part of a general design and risk review before taking this mitigation approach.

4.3.2 Physical Barriers

Placement of a physical barrier can prevent whiskers from growing from one conductive surface to another. For this standard, barriers are walls, cases, shields, or other hard material that whiskers will not penetrate. They are not the same as materials applied as a coating to the part. While a barrier may prevent a whisker growing from one conductive surface to another, it cannot mitigate the risks associated with free-floating whiskers unless a combination of barriers fully encase the Pb-free tin-finished area.

There **shall** be a documented process for reviewing the hardness of the barrier, examining the possibility and impact of whisker shorts within the enclosed area, and evaluating the risk and impact of free-floating whiskers escaping from the enclosed area.

4.3.3 Conformal and Other Coats as a Single Mitigation

Conformal coat **shall** be applied using a documented process meeting the applicable requirements of IPC-CC-830 and IPC-J-STD-001 for class 3 hardware.

Validation of conformal coat coverage shall be performed, if required by Control Level of the assembly, using either representative production hardware or a designated test vehicle processed in accordance with the documented production process.

Conformal coat materials **shall** conform to the categories in IPC-CC-830 with the exception of Types UT (Ultra-Thin) and SC (Styrene Block Copolymer), which are not allowed for tin whisker mitigation.

Thicknesses **shall** be per IPC-J-STD-001, section on “Coating, Encapsulation and Staking: Thickness.”

If deliverable production hardware was used in the original validation and the coating was found to be noncompliant, touch-up per IPC-J-STD-001, section on “Coating, Encapsulation and Staking: Rework or Touch-up” is allowed with assembly reinspection. However, only normal production touch-up may be done prior to the validation of the conformal coating process.

Gap size requirements are used in conjunction with conformal coat for mitigations to ensure there is an adequate air gap for whiskers to buckle upon contacting conformal coats on adjacent surfaces. The specific gap size requirement is given in [3.2.3.3](#) or [3.2.4.3](#).

Other aspects of conformal coat, such as possible stresses that may be induced by the coating or affect the curing requirements on the underlying hardware, should be addressed in the general engineering for the product.

4.3.3.1 Critical Conformal Coat Parameters

The critical parameters for process documentation and designing a representative validation sample are:

- Conformal coat type and product formulation. Include information about viscosity and solid content if applicable.
- For spray conformal coats: pressure, nozzle type, angles, number of passes, solid content, and drying time before cure.
- For manual spray conformal coats: flow rate, air assist pressure, speed, and hand angle (as per training).
- For dip conformal coats: immersion and withdrawal rates, dwell time, bath and assembly orientation, and drying time before cure.
- For brush conformal coats: type of brush(es) used, volume of conformal coat material being pushed with the brush, application technique (stroke pattern and motion, as per training).
- For vacuum deposition conformal coats: vacuum level, deposition length.
- For heat cures: temperatures and times.
- For humidity cures: relative humidity and times.
- For UV cures: wavelength and times.
- For IR cures: wavelength, temperature, and times.
- For air cures: temperature, humidity, and times.
- For all: surface preparation and cleanliness protocols.

4.3.3.2 Destructive Process Qualification (For Control Levels 2B and 2C)

The Process Qualification applies to all assemblies determined to be similar based on the requirements of **Error! Reference source not found.**

The sample size for destructive conformal coat process qualification shall be in accordance with [Table 1](#).

Table 1 - Conformal coat process qualification sample size

	# assemblies	Piece part types per assembly	# piece part per type	Total # piece parts across assemblies
Process Qualification	≥3 (test vehicles or identical or different samples from production)	Select representative package styles as necessary for future qualification by similarity purposes.	≥3	≥22

Samples of all external surfaces shall be inspected on the sample devices.

4.3.3.2.1 Conformal Coat Process Qualification Method for Control Levels 2B and 2C

Coating shall be inspected at 20X minimum (above IPC-J-STD-001 requirements), using ultraviolet light if the coating contains a fluorescing agent. There **shall** be no exposed conductors. This includes coating on all surfaces, regardless of whether they are Pb-free tin or not.

Coating shall be verified through either cross-section or coating peeling. Equivalent methods may be used with Technical Review Board (TRB) approval of equivalency. The components and their coating shall be photo-documented and coating thicknesses measured and recorded, if possible. Thickness measurements should be possible using cross section but may not be possible using peel. There shall be no exposed conductors.

If the cross-section method is used, component shall be removed by cutting around them. A method shall be employed that creates a visual boundary between the candidate coating and subsequent layers of overcoating or potting material. Cross-sectional analysis **shall** be conducted for both the end view and profile view of the component leads with an emphasis on component leads where a tin whisker short risk is present (see [Figure 1](#)).

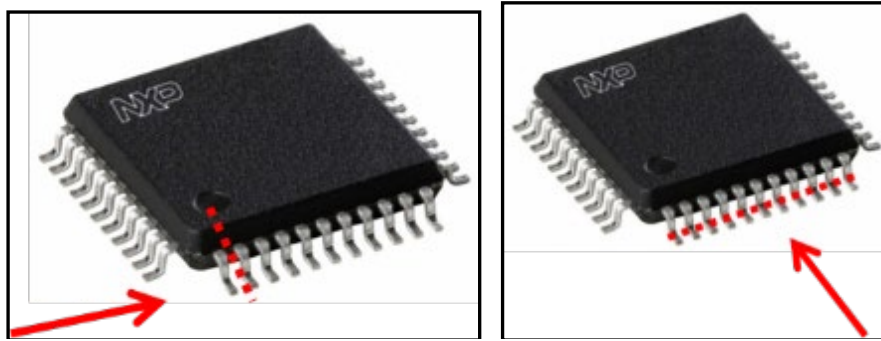


Figure 1 - Cross-section angles: profile (left) and end (right)

An alternative method for conformal coating assessment is the peel method. This method is suited for pliable conformal coatings such as silicones or acrylics and may not be applicable to rigid conformal coatings such as epoxies or urethanes. The peel method is generally considered a destructive test due to the risk of causing laminate damage.

4.3.3.2.1.1 Example Cross-Sectional Analysis Flow

1. Identify the designated sample components and cut the assembly around the components for removal. Handle the sample in a manner to prevent any damage to the conformal coating, keep any evidence intact, and maintain traceability of the component and location from which it was removed. Carefully clean off any remaining debris from cutting such that the conformal coating is not altered.
2. Using a vacuum chamber gold sputtering system, deposit a thin layer of gold over each designated component, specifically the areas to be analyzed. The thin layer of gold provides a visual boundary between the candidate coating and subsequent layers of overcoating or potting material.
3. Overcoat each specimen with a harder material to prevent tear-out of softer coatings during grinding and polishing operations used during the cross-sectioning.
4. Cross-section grind and polish in an orientation to measure and analyze the conformal coating in crevices and corners and for subsequent photo-documentation.
5. Photo-document conformal coating thickness and uniformity data.
6. Measure conformal coating thickness for each designated component using the metallographic microscope measurement system.

4.3.3.2.1.2 Example Peel Analysis Flow

The peel method procedure is:

1. Using a dull knife blade, slit the conformal coating near the component of interest and peel onto the component.
2. Carefully lift and peel the conformal coating from the component.
3. Confirm presence of conformal coat.

In some cases, the piece part will need to be removed from the assembly by clipping the termination in order to peel the coating on the backside of the lead.

4.3.3.3 Nondestructive Inspection (Qualification for Control Level 2A, Recurring for Control Levels 2B and 2C)

For nondestructive inspection, coating shall be inspected at 20X minimum, using ultraviolet light if the coating contains a fluorescing agent. There **shall** be no exposed conductors. This includes coating on all surfaces, regardless of whether they are Pb-free tin or not.

NOTE: These are not the same inspection requirements as J-STD-0001.

For formed leads and other surfaces with corners, special attention **shall** be paid to thin or missing coating due to sharp edges where exposed metal is more likely. If it is too difficult to ascertain whether conformal coating is present or not, additional inspections at higher magnifications, other lighting conditions, or angles shall be used to prove the presence of the coating.

NOTE: Printed wiring board outer layer conductors covered by solder mask are not exposed conductors.

Visual criteria from IPC-J-STD-001, section on “Coating, Encapsulation and Staking,” **shall** be applied. This includes requirements for uniformity, bubbles, delamination, FOD, and other inspectable conditions.

Photo documentation shall be performed, including areas where coverage is not clearly discernable and example photographs of typical coverage. Any areas where coverage is not clearly discernable shall be dispositioned by an engineering review board or equivalent.

The sample size shall be in accordance with [Table 2](#).

Table 2 - Conformal coat recurring validation sample size

	# assemblies	Piece part types per assembly	# piece part per type	Min total # piece parts across assemblies
Recurring inspection	≥1	Consistent with part types on initial qualification	≥3	≥22

For Control Level 2B, the requirement for recurring nondestructive inspection may be waived if process consistency can be established and validated some other way. Some examples of alternate approaches to process consistency validation are provided in Appendix C.

Control Level 2C requires annual nondestructive inspection. This requirement may be waived if process consistency is established and the inspection removal is approved by the customer.

NOTE: Flat coupon verification of conformal coating is insufficient for establishing process consistency for the purposes of tin whisker mitigation. Part geometry as described in this section is critical.

4.3.3.4 Qualification by Similarity (Compared to Nondestructive Results for Control Level 2A and Destructive Results for Control Levels 2B and 2C)

The expectation is that the process qualification will be applicable to multiple designs. There are two aspects to be considered when determining if a new product can be considered to be qualified by similarity to previous process qualification: process similarity and assembly design similarity.

The process shall be considered similar so long as there have been no major changes per IPC-J-STD-001 and there have been no changes to the following:

- Conformal coat material
- Conformal coat application equipment
- Changes in application process parameters (such as those in [4.3.3.1](#))
- Method of cure
- Changes in location of conformal coating process (i.e., address change)

Assembly design **shall** be considered similar to the process verification samples if the following can be shown to be the same:

- a. Gap size (smaller than or equal gap size, for both between leads and between components, to the planned application)
- b. Piece part type and shape (package styles and sizes are comparable)
- c. Likelihood of shadowing (for spray conformal coats)

The similarity shall be established and documented by a manufacturing or engineering review board.

4.3.3.5 Verification Artifacts for Conformal Coat

The verification artifacts **shall** be made available to the customer when requested.

- a. Description of conformal coat process (at a minimum addressing the information in [4.3.3.1](#))
- b. Description of test assembly
- c. Discussion of the test assembly was determined to be representative (including gap size, shape and piece part type, and shadowing, if applicable)
- d. Results of the destructive inspection, including the test report, quantitative results, and photographs
- e. Dates and description of the last periodic nondestructive inspection, including number of piece parts and description of package styles
- f. Objective evidence used to establish process consistency (and waive recurring inspection) for Control Level 2B, if applicable

It is understood that sharing the actual documents may require an NDA and hard and electronic copies may not always be sent to the customer, but an option to review the document in some way if requested is required.

4.3.3.6 Small Batch Processing

It is understood that, in some cases, the number of assemblies using this mitigation method may be small, and performing a process qualification may not be cost-effective. For Levels 2B or 2C where conformal coat is used as a single mitigator, 100% nondestructive inspection (of all devices on all assemblies) consistent with [4.3.3.3](#) may be allowed as an alternate to process qualification with customer approval. Particular attention shall be paid to conductive surfaces at different potential from the Pb-free tin surface within 1 mm from the Pb-free tin surface, noting that these surfaces may be on neighboring parts.

4.3.4 SnPb Soldering Process with Validated Coverage as a Single Mitigation

This section applies to Pb-free tin piece parts installed with SnPb solder for mitigation and cases where Pb-free finished tin piece parts have been reworked with solder dipping but not to the requirements of GEIA-STD-0006. As stated in the definition, if all Pb-free tin finishes on the device have been replaced through replating or solder-dipping, following GEIA-STD-0006 or equivalent, then the device is no longer considered to be Pb-free tin finished.

The SnPb soldering process shall use a documented process meeting the requirements of IPC-J-STD-001 for Class 3 hardware.

Validation of SnPb solder coverage shall be performed using either representative production hardware or a designated test vehicle processed in accordance with the documented production process.

4.3.4.1 Piece Part Level Verification

Piece parts that have been dipped per GEIA-STD-0006 or equivalent no longer have Pb-free tin finish and no additional actions are needed. Piece parts that have been dipped, but not per GEIA-STD-0006 or equivalent, such as with manual dipping, may be evaluated at the piece part level before installation.

For piece part level dip process mitigations, the following **shall** be true:

- a. Use Sn63Pb37, Sn60Pb40, or Sn62Pb38 for the dip.
- b. ESD procedures per ANSI/ESD S20.20 are in place if the piece part is ESD sensitive. This includes validating the grounding of the solder pot.
- c. There is a process for monitoring and removing dross and surface residue consistent with those in GEIA-STD-0006.
- d. Components are evaluated for the necessity of preheating before dipping (for thermal shock and moisture sensitivity).
- e. Piece parts may be dipped a maximum of three times with cooldown between attempts.
- f. Piece parts are cleaned to remove the flux within 1 hour of cooldown.
- g. Piece parts are 100% inspected under at least 40X magnification for complete coverage of the tin surfaces and no delamination or other damage.

Because of the potential for non-visible damage to piece parts during solder dipping, it is recommended that complex piece parts receive electrical testing as a first article check. For many piece parts, more extensive electrical testing can be accomplished at first electrical test at the assembly or module level. For cavity piece parts, great care needs to be taken. It is recommended that hermetic testing be performed on piece parts where hermeticity was initially required. For non-hermetic piece parts, samples should be checked for flux contamination inside the cavity.