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Performance Testing for Aerospace and High Performance Electronic
Interconnects Containing Pb-free Solder and Finishes

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Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes

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December 2012



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(Formulated under the cognizance of the TechAmerica (APMC) Avionics Process Management Committee. This document was prepared by the LEAP working group, a multi-association group consisting of the AIA, TechAmerica, and the AMC.)

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Performance Testing for Aerospace and High Performance Electronic Interconnects Containing Pb-free Solder and Finishes

GEIA-STD-0005-3-REV A

Revision	Description of change	Date
-	Initial Release	Jun 2008
A	Updates and corrections to the body of the text Removed Appendix B – Material Properties of Pb-free Solder Materials Added new Appendix B – Bulk Material Testing Added Appendix D – Illustrative Examples of Failure Mechanisms in Thermally Aged Pb-free Interconnects	Dec 2012

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The success of this standard is a tribute to the effort put forth by these individuals as well as those who contributed toward Revision A of this standard (Ken Bowden of New Mexico Institute of Mining and Technology, John Biel of GE Aviation, Gary Latta of NSWC-Crane, Jeffrey Suhling of CAVE-Auburn University, and Paul Vianco of Sandia National Laboratories). Their knowledge, experience, creativeness, and open-minded view produced a document that will benefit all engineers in understanding the performance characteristics of Pb-free technology such that reliable products can continue to support the military and aerospace user community. Appreciation is also extended to the Aerospace Industries Association (AIA) Pb-free Electronics Risk Mitigation (PERM) consortium who supported Revision A of this document.

Anthony J. Rafanelli, Ph.D., P.E.
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Forward

The implementation of Pb-free (lead-free) interconnection technology into electronics has resulted in a variety of reactions by designers, manufacturers, and users. While the prime motivation for Pb-free technology was to address the social concern of improving the environment by limiting the amount of toxic and dangerous substances used in products, the ramifications of this initiative have provided a state of uncertainty regarding the performance* of aerospace and defense systems. For over fifty years, SnPb (tin-lead) solder was the benchmark for electronics assembly and generations of research baselined its performance under a variety of operating conditions including the harsh settings of aerospace and defense equipment. However, with the integration of Pb-free technology, aerospace and defense companies are faced with questions as to whether these new materials will provide, as a minimum, the same degree of confidence during the life cycle of critical systems and products.

In evaluating performance, two approaches are used: analysis/modeling and test. This document addresses the latter providing guidance and direction in the development and execution of performance tests for Pb-free electronic interconnections. The user of this document needs to be aware of the following: This document does not give answers as to how to perform a specific test. Products and systems applications vary immensely so designers need to understand use conditions and the entire life cycle. Once this is understood, then this document can be used to give designers an understanding of how to develop a suitable test, e.g., ascertaining the type of platform in which a product will be used, comprehending all the environmental effects on the platform, and learning about why material characterization is key to deciding upon test parameters, etc.

Sound engineering knowledge and judgment will be required for the successful use of this document.

*In this context, performance is defined as operation and reliability, i.e., the expected life cycle of a product.

Introduction

The global transition to Pb-free electronics has a significant impact on the electronics industry; and it is especially disruptive to aerospace and other industries that produce electronic equipment for high performance applications. These applications, hereinafter described as AHP (Aerospace and High Performance), are characterized by severe or harsh operating environments, long service lifetimes, and high consequences of failure. In many cases, AHP electronics must be repairable at the soldered assembly level. Typically, AHP industry production volumes may be low and, due to low market share, they may not be able to resist the change to Pb-free. Furthermore, the reliability tests conducted by suppliers of solder materials, components, and sub-assemblies cannot be assumed to assure reliability in AHP applications. This document provides guidance (and in some cases direction) to designers, manufacturers, and maintainers of AHP electronics in assessing performance of Pb-free interconnections.

Over the past several decades, electronics manufacturers have developed methods to conduct and interpret results from reliability tests for lead-bearing solder alloys. Since these alloys have been used almost universally in all segments of the electronics industry, and since a large body of data, knowledge, and experience has been assembled, the reliability tests for Pb-bearing solder alloys are well-understood and widely accepted.

When it became apparent that the use of Pb-bearing alloys would decline rapidly, programs were implemented to evaluate the reliability of the Pb-free replacement alloys. Those programs have generated a considerable database. To date, however, there is no reliability test method that is widely accepted in the AHP industries. Reasons for this include:

1. No single Pb-free solder alloy has emerged as a replacement for lead-bearing alloys; instead, a number of alloys are being used in various segments of the electronics industry.
2. The physical, chemical, and metallurgical properties of the various Pb-free replacement alloys vary significantly.
3. Due to the many sources of solder alloys used in electronic component termination materials or finishes, assembly processes, and repair processes; the potential number of combinations of alloy compositions is nearly unlimited. It is an enormous task to collect data for all these combinations.
4. The test methods developed by other segments (References [1] and [2]) are directed toward shorter service lives and more benign environments. Also, there is still a question of suitable dwell times and acceleration factors. (However, the intent of this document is to provide a means of coordinating the information from References [1] and [2] into a basic approach for AHP suppliers.)
5. The data from reliability tests that have been conducted are subject to a variety of interpretations.

In view of the above facts, it would be desirable for high-reliability users of Pb-free solder alloys to wait until a larger body of data has been collected, and methods for conducting reliability tests and interpreting the results have gained wide acceptance for high-reliability products. In the long run, this will indeed occur. However, the transition to Pb-free solder is well under way and there is an urgent need for a reliability test method, or set of methods, based on industry consensus. While acknowledging the uncertainties mentioned above, this document provides necessary information for designing and conducting performance tests for aerospace products. In addition, when developing test approaches, the material in question needs to be suitably characterized. Such material properties as ultimate tensile strength, yield strength, Poisson's ratio, creep rate, and stress relaxation have been shown to be key attributes in evaluating fatigue characteristics of Pb-free solders.

Because of the dynamic nature of the transition to Pb-free electronics, this and other similar documents must be considered provisional. While this document is based on the best information and expertise available, it must be updated as future knowledge and data are obtained.

The intent of the document is not to prescribe a certain method, but to aid avionics/defense suppliers in satisfying the reliability and/or performance requirements of GEIA-STD-0005-1 [5] as well as support the expectations in GEIA-HB-0005-1 [6]. Accordingly, it includes:

1. A default method for those companies that require a pre-defined approach and
2. A protocol for those companies that wish to develop their own test methods.

Also, this document will focus on testing the Pb-free interconnections, i.e., the “system” comprised of the solder alloy as well as the component and board finishes. While the bulk of this introduction has discussed reliability testing of Pb-free assemblies, this document will direct attention to test guidelines to evaluate the performance of the Pb-free interconnection. The guidelines presented in this document do not suggest methods for reliability testing of product. That is left to each individual user. What the document does is provide insight as to what approaches should be used as part of a performance test when Pb-free interconnection is of prime interest. Given the current state of the industry, gaps do exist in the knowledge base especially in some recently disclosed phenomenon such as effects of room temperature aging as well as issues in COTS testing and accelerated test. Subsequently, the user is advised to corroborate/validate information provided in the associated references.

In summary, the purpose of this document is threefold:

1. It is meant to provide a means to acquire sound, accurate data regarding the performance of a Pb-free interconnection under harsh conditions (aerospace, military, medical, etc.,)
2. It is usable for further design assessment and operation of a product, and
3. It is usable as part of a process development study.

Finally, any portion of this document may be used to develop a Pb-free assembly test program, i.e., THIS DOCUMENT IS TAILORABLE and provides room for flexibility. For those situations in which results are used for reliability, verification, or qualification, it is strongly recommended that stakeholder concurrence be sought and documented so that expectations are understood and concerns are addressed.

1.0 SCOPE

This document defines:

1. A default method for those companies that require a pre-defined approach and
2. A protocol for those companies that wish to develop their own test methods.

The default method ([Section 4](#) of the document) is intended for use by electronic equipment manufacturers, repair facilities, or programs which, for a variety of reasons, may be unable to develop methods specific to their own products and applications. It is to be used when little or no other information is available to define, conduct, and interpret results from reliability, qualification, or other tests for electronic equipment containing Pb-free solder. The default method is intended to be conservative, i.e., it is biased toward minimizing the risk to users of AHP electronic equipment.

The protocol ([Section 5](#) of the document) is intended for use by manufacturers or repair facilities which have the necessary resources to design and conduct reliability, qualification, or process development tests that are specific to their products, their operating conditions, and their applications. Users of the protocol will have the necessary knowledge, experience, and data to customize their own methods for designing, conducting, and interpreting results from the data. Key to developing a protocol is a firm understanding of all material properties for the Pb-free material in question as well as knowledge of package- and board-level attributes as described in [Section 4.1.1](#). As an example, research has shown that the mechanisms for creep are very different between SnPb and Tin-Silver-Copper (SAC) solders. Understanding these mechanisms is key to determining critical test parameters such as dwell time for thermal cycling. The protocol portion of this document provides guidance on performing sufficient characterization of new materials in order to accurately define test parameters.

Use of the protocol is encouraged, since it is likely to yield more accurate results. Reference [\[7\]](#) provides a comprehensive overview of those technical considerations necessary in implementing a test protocol.

This document addresses the evaluation of failure mechanisms, through performance testing, expected in electronic products containing Pb-free solder. One failure mode, fatigue-failure through the solder-joint, is considered a primary failure mode in AHP electronics and can be understood in terms of physics-of-failure and life-projections. Understanding the all potential failure modes caused by Pb-free solder of AHP electronics is a critical element in defining early field-failures/reliability issues. Grouping of different failure modes may result in incorrect and/or misleading test conclusions. Failure analysis efforts should be conducted to insure that individual failure modes are identified enabling the correct application of reliability assessments and life-projection efforts.

When properly used, the methods or protocol defined in this document may be used along with the processes documented in compliance to Reference [\[3\]](#), to satisfy, at least in part, the reliability requirements of References [\[3\]](#) and [\[4\]](#).

This document may be used for products in all stages of the transition to Pb-free solder, including:

- Products that have been designed and qualified with traditional SnPb electronic components, materials, and assembly processes, and are being re-qualified with use of Pb-free components
- Products with SnPb designs transitioning to Pb-free solder; and
- Products newly-designed with Pb-free solder.

For programs that were designed with SnPb solder, and are currently not using any Pb-free solder, the traditional methods may be used. It is important, however, for those programs to have processes in place to maintain the SnPb configuration including those outsourced or manufactured by subcontractors.

With respect to products as mentioned above, the methods presented in this document are intended to be applied at the level of assembly at which soldering occurs, i.e., circuit-card assembly level. For those users interested in COTS (commercial-off-the-shelf) testing, some guidance at box-level (e.g., power suppliers, module assemblies, etc.) is provided in [Section 6.0](#).

IMPORTANT TO NOTE: This standard does not apply to space flight hardware. Applications that do not permit the use of Pb-free soldering for circuit board assembly, such as electronic hardware for space flight, are outside the scope of this document.

The demonstration of successful performance or acceptable reliability of hardware through a test program consistent with this Standard may be application-specific, and should not be construed as demonstrating qualification of the same hardware for a different application where Pb-free solder and finishes have been prohibited.

2.0 REFERENCES

These references represent a combination of refereed/controlled documents as well as briefings used to support informational items discussed throughout the standard. The user is encouraged to use additional references, as necessary, to better clarify test objectives and design.

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These references represent a combination of refereed/controlled documents as well as briefings used to support informational items discussed throughout the standard. The user is encouraged to use additional references, as necessary, to better clarify test objectives and design.

3.0 TERMS AND DEFINITIONS

AHP – Aerospace and High Performance referring to a generalized level of equipment use in harsh and stringent operating conditions.

CCA – circuit card assembly

Coupon – a test sample representing a scaled-down or proportional version of an actual product or higher level test vehicle.

DSC – Differential Scanning Calorimeter.

LEAP – Pb-free Electronics in Aerospace Project supported by the Aerospace Industries Association (AIA), TechAmericas, and the Avionics Maintenance Conference (AMC).

JCAA – Joint Council on Aging Aircraft.

JG-PP – Joint Group on Pollution Prevention referring to the Department of Defense initiative that sponsored a project to obtain design data from testing Pb-free assemblies under a series of military environments.

Lead – Term associated with the termination of an electronic component, i.e. the structure that makes electrical contact with a printed wiring board.

PERM – Pb-free Electronics Risk Management consortium which is the successor to the LEAP (see above) group. The PERM is supported by the Aerospace Industries Association (AIA).

Pb-Free - meaning that the content of the element lead is $< 0.1\%$ by weight. [The chemical symbol for the element is used so as to not confuse the reader when the term “lead”, meaning the electrical connection of a component, is used.]

PSD – Power Spectral Density; describes how the power of a signal or time series is distributed with frequency.

RoHS – Restriction on Hazardous Substances (DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment).

SnPb – Solder bearing the elements tin and lead, respectively, in the by-weight amounts of 63-37 unless otherwise specified.

Vehicle – A test sample such as a populated circuit card assembly.

4.0 DEFAULT TEST METHODS

Use of the default method *shall* be limited to traditional (mature design) circuit-card assemblies (CCA). Also, the use of test coupons may also be used provided the concerns listed in Section 4.1.1 are considered.

4.1 Test Vehicles

4.1.1 Test Vehicle type

Test vehicles used in testing of electronic systems containing Pb-free solder *shall* consist of soldered assemblies that are representative of the materials and processes used in the assembly and/or repair procedures used by the AHP manufacturer or repair facility. Characterization and documentation of the test vehicle attributes (both design and manufacturing) is recommended. Test vehicle attribute documentation *shall* include, at a minimum, the following data:

- Board type, material, size, finish, thickness, Copper content
- Piece-part material, package size, package type, termination finish
- Assembly solder alloy
- Assembly processes including fluxes and cleaners
- Thermal management materials
- Underfill and staking materials
- Other mechanically attached structures
- Environmental coatings
- Repair history/process (including solder alloys)

The utilization of electrically functional assemblies/units or representative test vehicles is permitted provided full characterization of the electronic assembly materials, test vehicle configuration, and assembly processes are documented. The IPC-9701A specification (Section 4.2) contains additional guidance on the characterization and documentation for test vehicles [1].

The use of test coupons may be used but the user is cautioned that various attributes of concern can be different at coupon level, i.e., cool down rates, metallurgy, pitch, others. If the use of coupons is desired, the user *shall* perform an analysis to determine if such attribute differences exist. If differences are determined, the user *shall* mitigate associated risks. Be aware that results are based upon the processes used and that complete documentation of the processes is necessary if this document is being used to evaluate the processes.

4.1.2 Sample size

The number of test vehicles *shall* be based on a statistically based sample size and analysis plan. Accordingly, several options are available. IPC-9701A specifies a minimum number of 33 test