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SAE J1850 Verification Test Procedures

RATIONALE

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1. Scope

- 1.1 Purpose**—This SAE Recommended Practice recommends test methods, test procedures, and specific test parameters to help verify that vehicles and test tools can communicate using the SAE J1850. This document only verifies the portion of SAE J1850 that is used for OBD-II communications. The term “test tool” is synonymous with OBD-II Scan tool.
- 1.2 Application**—The procedures, methods, and parameters contained in this document apply to vehicles and test tools which support OBD-II messages, as outlined in SAE J1979. SAE J1699 is intended primarily for use as a design verification aid.
- 1.3 Rationale**—This document has been reaffirmed to comply with the SAE 5-Year Review policy.

2. References

- 2.1 Applicable Publications**—The following publications form a part of this specification to the extent specified herein. Unless otherwise specified, the latest issue of SAE publications shall apply.

- 2.1.1 SAE PUBLICATIONS—Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or 724-776-4970 (outside USA), www.sae.org.

SAE J1699-2—OBD-II Related SAE Specification Verification Test Procedures
SAE J1850 MAY2001—Class B Data Communication Network Interface
SAE J1962 FEB98—Diagnostic Connector
SAE J1978 FEB98—OBD-II Scan Tool
SAE J1979 SEP97—E/E Diagnostic Test Modes

- 2.2 Related Publications**—The following publications are provided for information purposes only and are not a required part of this specification.

- 2.2.1 SAE PUBLICATIONS—Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or 724-776-4970 (outside USA), www.sae.org.

SAE J1213-1 SEP97—Glossary of Vehicle Networks for Multiplexing and Data Communications
SAE J1930 MAY98—Electrical/Electronic Systems Diagnostic Terms, Definitions, Abbreviations, & Acronyms
SAE J2178-1 MAR99—Class B Data Communication Network Messages

3. Definitions

- 3.1 Active State**—The state of a bus wire that results when one or more nodes have “turned on” their physical layer circuitry. This is V_{oh} volts for Bus + (PWM and VPW) and V_{ol} volts for Bus - (PWM only). Refer to Table 4 (PWM DC Parameters) and Table 6 (VPW DC Parameters) in SAE J1850 for the values of V_{oh} and V_{ol} . The active state voltage level is determined by the source voltage of the physical layer drive circuitry.
- 3.2 Arbitration**—The process of resolving which frame, or In-Frame Response data, continues to be transmitted when two or more nodes begin transmitting frames, or In-Frame Response data, simultaneously.
- 3.3 Dominant Bit**—A bit which wins arbitration when contending for the bus. For SAE J1850, a logic “0” is the dominant bit.

- 3.4 Dual Wire**—Two wires that are routed adjacently throughout the vehicle and can be either a twisted or a parallel pair of wires.
- 3.5 Fault Tolerance**—The ability of a system to survive a certain number of failures with allowance for possible down-graded performance while maintaining message transmission capability at the specified data rate.
- 3.6 Frame**—One complete transmission of information, which may or may not include an “in-frame response.” For this network, each frame contains one and only one message. A frame is delineated by the Start of Frame (SOF) and End of Frame (EOF) symbols.
- 3.7 Maximum OBD-II Scan Tool Load**—The maximum electrical load that the OBD-II Scan tool may have. $C_{load\ max}$ is 500 pF and $R_{load\ min}$ is 10.6 k Ω .
- 3.8 Maximum Vehicle Load**—The maximum electrical load that the vehicle network may have. Refer to SAE J1850 for the values of $C_{load\ max}$ and $R_{load\ min}$. The electrical load of the OBD-II Scan Tool must be subtracted from $C_{load\ max}$ and $R_{load\ min}$.
- 3.9 Minimum Vehicle Load**—The minimum electrical load that the vehicle network may have. Refer to SAE J1850 for the values of $C_{load\ min}$ and $R_{load\ max}$. The electrical load of the OBD-II Scan Tool must be subtracted from $C_{load\ min}$ and $R_{load\ max}$.
- 3.10 Message**—All of the data bytes contained in a frame. The message is what remains after the frame symbols have been removed from the frame. As such, the message is the sequence of bytes contained in the frame.
- 3.11 Passive State**—The state of a bus wire which results when all nodes have “turned off” their physical layer circuitry. This is V_{ol} volts for Bus + (PWM and VPW) and V_{oh} volts for Bus - (PWM only). Refer to Table 4 (PWM DC Parameters) and Table 6 (VPW DC Parameters) of SAE J1850 for the values of V_{oh} and V_{ol} . The passive state voltage level is determined by the reference voltage of the bus wire termination resistor(s).
- 3.12 Pulse Width Modulation (PWM)**—A data bit format, where the width of a pulse of constant voltage or current determines the value (typically one or zero) of the data transmitted.
- 3.13 Recessive Bit**—A bit which loses arbitration when contending for the bus with a dominant bit. For SAE J1850, a logic “1” is the recessive bit.
- 3.14 Variable Pulse Width (VPW) Modulation**—A method of using both the state of the bus and the width of the pulse to encode bit information. This encoding technique is used to reduce the number of bus transitions for a given bit rate. One embodiment would define a “ONE” (1) as a short active pulse or a long passive pulse while a “ZERO” (0) would be defined as a long active pulse or a short passive pulse. Since a frame is comprised of random 1's and 0's, general byte or frame times cannot be predicted in advance.
- 3.15 Unit Load**—The electrical loading effect of each device connected to the network will be measured in terms of unit loads. A unit load is a nominal value which, if all nodes correspond to one unit load, will allow the maximum specified number of nodes to be connected to the network. There is no requirement that a given node must be equal to a standard unit load, but the combination of all load values must not exceed the limits for any given system.

4. Abbreviations and Acronyms

CRC	Cyclic Redundancy Check
DUT	Device Under Test (either the OBD-II Scan Tool or the Vehicle)
EOD	End of Data
EOF	End of Frame
IFR	In-Frame Response (Byte/Bytes)
IFS	Inter-Frame Separation
NAD	Network Access Device
OBD-II	On-Board Diagnostics version two
PWM	Pulse Width Modulation
PID	Parameter ID
SOF	Start of Frame
VPW	Variable Pulse Width

5. General Information

5.1 Test Procedure Overview—The procedures contained in this document are intended to test a subset of the SAE J1850 specification. The following is a short synopsis of the purpose of each of the tests.

- 5.1.1 **INVALID CRC TEST**—Verifies that the module under test generates correct CRCs. Also, verifies that the module discards any message sent to it with an incorrect CRC.
- 5.1.2 **MESSAGE STRUCTURE TEST**—Verifies that the DUT uses all required frame elements in the proper order, and that it is capable of recognizing and responding to network traffic.
- 5.1.3 **BUS ARBITRATION TEST**—This test confirms the DUT arbitrates for bus control during message header transmission.
- 5.1.4 **BUS FAULT TEST**—Verifies that the DUT meets all failure modes specified by SAE J1850 as required modes and optional modes (if applicable).
- 5.1.5 **SYMBOL PARAMETER LIMITS**—Verifies that the DUT shall receive and transmit symbols within specified SAE J1850 limits.

5.2 Generic Test Conditions—The tests shall be performed under conditions considered to be a typical garage environment. The environment shall not exceed the temperature extremes of either the device under test or any of the pieces of test instrumentation. Test personnel may want to record the temperature and humidity the test procedures were performed under. The test sequence is arbitrary.

5.2.1 DIGITAL SCOPE REQUIREMENTS

- a. Record 20 ms of network traffic
- b. 20 pF (max)
- c. 1 M Ω (min)
- d. 2 channel 100 MHz digital storage scope (min)
- e. Pre-trigger input
- f. Hewlett-Packard 54600B or equivalent

5.2.2 POWER SUPPLY REQUIREMENTS—All power supplies specified in this document are industry standard.

5.2.2.1 PS#1—The power supply shall be capable of supplying 0 to 24 V DC at 5 A or HP 6543A equivalent.

5.2.2.2 PS# 2—Refer to the Voltage Ground Offset device description for power supply requirements or HP 6023A equivalent.

5.2.2.3 PS#3—The power supply shall be capable of supplying 0 to 12 V DC at 0.5 A or HP 6543A equivalent.

5.2.2.4 PS#4—Refer to the Small Signal Voltage Ground Offset device description for power supply requirements or HP 6543A equivalent.

5.2.3 DIGITAL VOLT OHM METER (DVOM) REQUIREMENTS—Industry standard DVOM or Fluke 87 equivalent.

5.2.4 GROUND OFFSET VOLTAGE DEVICE—The Ground Offset Voltage device, shown in Figure 1, introduces a voltage offset in the test fixtures. PS #2 provides current in the $0.1\ \Omega$ resistor thereby producing a voltage rise from point (+) to point (–).

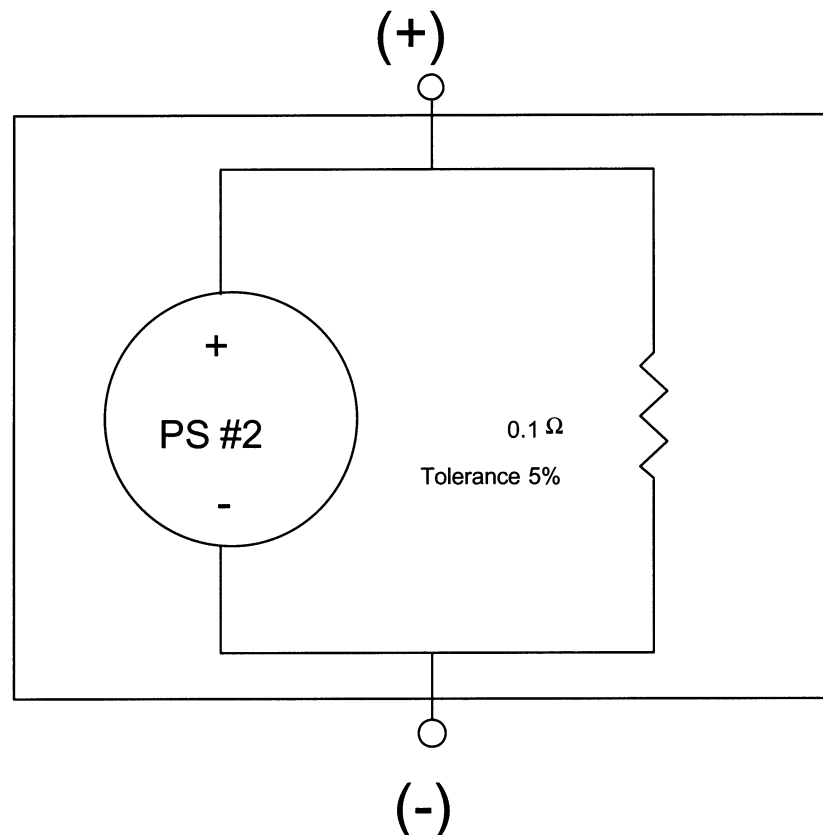


FIGURE 1—GROUND OFFSET VOLTAGE DEVICE

The Ground Offset Voltage device must be able to achieve a maximum of 1.9 V. The current calculation follows in Equation 1:

$$\text{Current} = \frac{\text{Voltage}}{\text{Resistance}} = \frac{1.9}{0.1\Omega} = 19\text{A} \quad (\text{Eq. 1})$$

PS #2 must be capable of supplying 20 A at 1.9 V. The power rating for the resistor is determined by Equation 2:

$$\text{Watts} = \text{Volts} \times \text{Current} = 1.9\text{V} \times 19\text{A} = 36.1\text{W} \quad (\text{Eq. 2})$$

The wattage rating on the resistor should be at least 50 W to account for temperature increases.

If the Ground Offset Voltage needs to be zero, remove the Ground Offset Voltage Device and short the (+) and (–) point together in the test fixture.

- 5.2.5 SMALL SIGNAL GROUND OFFSET VOLTAGE DEVICE—The Small Signal Ground Offset Voltage device, shown in Figure 2, introduces a voltage offset in PWM signal. PS #4 provides current in the 1.0 Ω resistor thereby producing a voltage rise from point (+) to point (–).

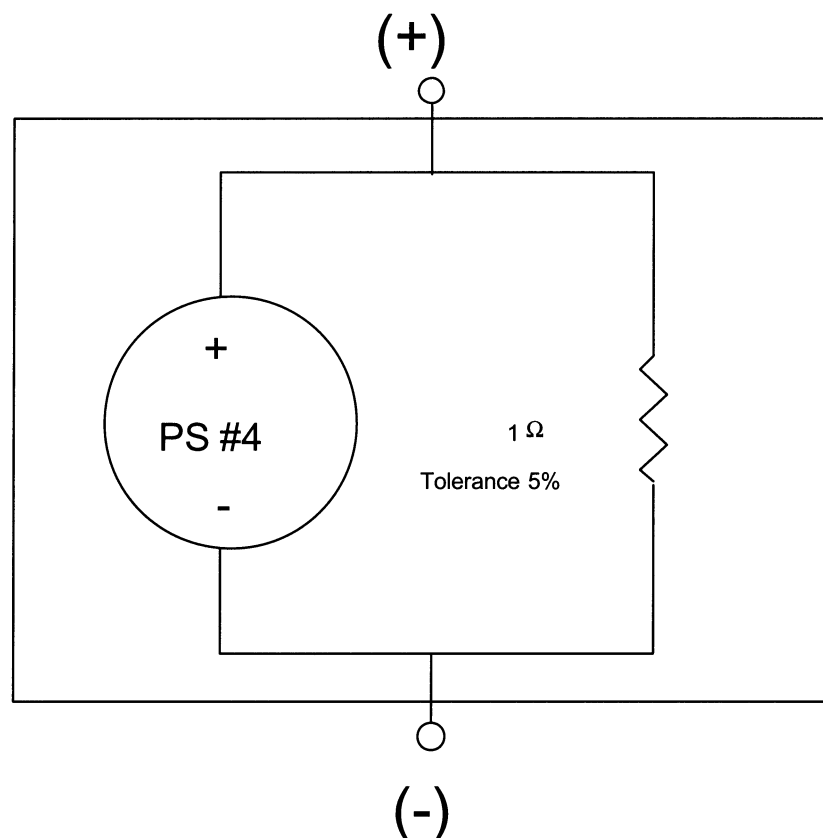


FIGURE 2—SMALL SIGNAL GROUND OFFSET VOLTAGE DEVICE

The Small Signal Ground Offset Voltage device must be be able to achieve a maximum of 4.0 V. The current calculation follows in Equation 3:

$$\text{Current} = \frac{\text{Voltage}}{\text{Resistance}} = \frac{4.0}{1.0\Omega} = 4\text{A} \quad (\text{Eq. 3})$$

PS #4 must be capable of supplying 4.0 A at 4.0 V. The power rating for the resistor is determined by Equation 4:

$$\text{Watts} = \text{Volts} \times \text{Current} = 4.0\text{V} \times 4.0\text{A} = 16.0\text{W} \quad (\text{Eq. 4})$$

The wattage rating on the resistor should be at least 20 W to account for temperature increases.

If the Small Signal Ground Offset Voltage needs to be zero, remove the Ground Offset Voltage Device and short the (+) and (–) point together in the test fixture.

- 5.2.6 VPW BUS RX/TX CIRCUIT—Figure 3 shows the schematic for the VPW Bus Transceiver. This circuit is not representative of a vehicle module physical layer. Resistors are 5% tolerant and 1/2 W unless otherwise specified.

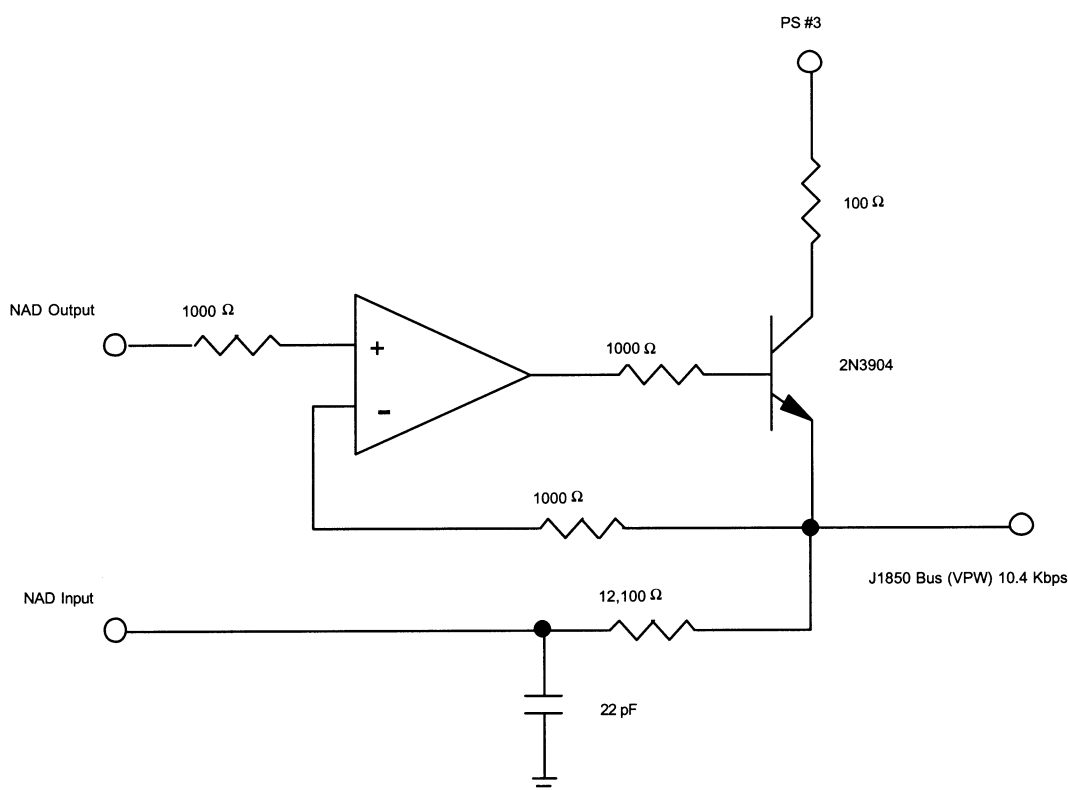


FIGURE 3—VPW BUS RX/TX CIRCUIT