



SURFACE VEHICLE RECOMMENDED PRACTICE

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(R) Handbook for Robustness Validation of Semiconductor Devices
in Automotive Applications

RATIONALE

Error and issue corrections with latest state of art updates.

FOREWORD

The quality of the vehicles we buy and the competitiveness of the automotive industry depend on being able to make quality and reliability predictions. Qualification measures must provide useful and accurate data to provide added value. Increasingly, manufacturers of semiconductor components must be able to show that they are producing meaningful results for the reliability of their products under defined mission profiles from the whole supply chain.

Reliability is the probability that a semiconductor component will perform in accordance with expectations for a predetermined period of time in a given environment. To be efficient reliability testing has to compress this time scale by accelerated stresses to generate knowledge on the time to fail. To meet any reliability objective requires comprehensive knowledge of the interaction of failure modes, failure mechanisms, the mission profile and the design of the product 10 years ago you could read: "Qualification tests of prototypes must ensure that quality and reliability targets have been reached".

This approach is no longer sufficient to guarantee robust electronic products for a failure free life of the car, which is the intention of the Zero-Defect-Approach. The emphasis has now shifted from merely the detection of failures to their prevention.

We started this way by introducing screening methods after the product had been produced after product has successfully survived a standard qualification. Then the focus shifted to reliability methodologies applied on technology level during development.

Now product qualification again changes from the detection of defects based on predefined sample sizes towards the generation of knowledge by generating failure mechanisms specific data, combined with the knowledge from the technology field. Now we can generate real knowledge on the robustness of products.

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Qualification focuses on intrinsic topics of products and technologies, requiring only small sample sizes. Defectivity issues now put a big load on monitoring measures, which are now needed to demonstrate manufacturability and the control of extrinsic defects.

This handbook should give guidance to engineers how to apply robustness validation during development and qualification of semiconductor components. It was made possible because many companies, semiconductor manufacturers, component manufacturers (Tier1) and car manufacturers (OEMs) worked together in a joint working group to bring in the knowledge of the complete supply chain.

I would like to thank all teams, organizations and colleagues for actively supporting the robustness validation approach.

Andreas Preussger
Core Team Leader RV Group
Editor in Chief 1st revision

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ZVEI Robustness Validation Committee Chairman

Helmut Keller, Keller Consulting Engineering Services

SAE Automotive Reliability Committee Chairman

Jack Stein, Transportation

Robustness Validation Core Team

Andreas Preussger (Team Leader), Infineon Technologies
Colman Byrne, Kostal Ireland GmbH
Werner Kanert, Infineon Technologies and AEC Member
Ole Mende, Audi AG Roger Rickey, R.E. Rickey & Associates Inc.

Representative of ZVEI

Rolf Winter, ZVEI e.V.

Representative of SAE

Caroline Michaels, SAE International

Representative of JSAE

Tadashi Wakiya, Tokai Rika Co., Ltd

Team Members of Working Groups

Boettger Eckart, Continental Automotive System
Clarac Jean, Siemens VDO and AEC Member
Craggs Dennis, Daimler Chrysler Corp
Enser Bernd, Sanmina-SCI
Giroux Francois, ST Microelectronics
Gehnen Erwin, Hella KGaA Hueck & Co
Hodgson Keith, Ford Motor Co.
Hrassky Petr, ST Microelectronics
Ishikawa Makato, Hitachi Ltd.
Ito Masuo, Nissan Motor Company Ltd
Jendro Brian, Siemens VDO and AEC Member
Kanekawa Nobuyasu, Hitachi Ltd.
Kanemaru Kenji, Tokai Rika Co Ltd.
Klaue Martin, Renesas Technology
Knoell Bob, Visteon Corporation and AEC Member
Koch Herbert, Robert Bosch GmbH
Liang Zhongning, NXP and AEC Member
Lycoudes Nick, Freescale Semiconductor and AEC Member

Maier Reinhold, BMW AG
Mori Satoshi, Tokai Rika Co Ltd.
Nakaguro Kunio, Nissan Motor Co., Ltd.
Narumi Kenji, TRAM Inc.
Petersen Frank, Elmos Semiconductor AG
Schilde Bernd, Brose Fahrzeugteile GmbH & Co
Schmidt Ernst, BMW AG
Senske Wilhelm, Daimler Chrysler Corporation
Takasu Yuji, Tokai Rika Co Ltd.
Unger Walter, Daimler Chrysler Corporation
Vanzeveren Vincent, Melexis
Wilson Peter, On Semiconductor
Wulfert Friedrich-W., Freescale Semiconductor

EDITORIAL TEAM 2ND EDITION

Andreas Preussger (Team Leader), Infineon Technologies
Jörg Breibach, Robert BOSCH GmbH
Bob Knoell, NXP and SAE Interface
Liang Zhongning, NXP and AEC Member
Wilhelm Binder, Atmel Automotive GmbH
Werner Kanert, Infineon Technologies and AEC Member
Vasquez-Borucki Infineon Technologies

We would like to thank the other members of the RV-Forum for their contributions to the 2nd edition

Representative of ZVEI
Rolf Winter, ZVEI e.V.

Boettger Eckart, Continental Automotive System
Enser Bernd, Sanmina-SCI
Unger Walter, Daimler Chrysler Corporation
Wulfert Friedrich-W., Freescale Semiconductor

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1. INTRODUCTION

In 2006 members of SAE International Automotive Electronic Systems Reliability Standards Committee, ZVEI (German Electrical and Electronic Manufacturers` Association), AEC (Automotive Electronics Council) and JSAE (Japanese Society of Automotive Engineers) formed a joint task force and published the first version of the Robustness Validation Handbook (RVHB) together with an update of the corresponding SAE document (SAE Recommended Practice J1879, General Qualification and Production Acceptance Criteria for Integrated Circuits in Automotive Applications), which was a content copy of the RVHB.

The RVHB was based on information from a wide number of sources including international Automotive OEMs and their full supply chain, engineering societies, and other related organizations.

This Robustness Validation Handbook provides the automotive electronics community with a common qualification methodology to demonstrate acceptable reliability. The Robustness Validation approach requires testing the component to failure, or end-of-life (EOL), avoiding invalid failure mechanisms, and evaluation of the Robustness Margin between the outer limits of the customer specification and the actual performance of the component.

Since then the principles defined in this handbook have been applied in modules, systems and other application areas. For details see section 19.

2. SCOPE

This document will primarily address intrinsic reliability of electronic components for use in automotive electronics. Where practical, methods of extrinsic reliability detection and prevention will also be addressed. The current handbook primarily focuses on integrated circuit subjects, but can easily be adapted for use in discrete or passive device qualification with the generation of a list of failure mechanisms relevant to those components. Semiconductor device qualification is the main scope of the current handbook.

Other procedures addressing extrinsic defects are particularly mentioned in the monitoring chapter. Striving for the target of Zero Defects in component manufacturing and product use it is strongly recommended to apply this handbook. If it gets adopted as a standard, the term "shall" will represent a binding requirement.

This document does not relieve the supplier of the responsibility to assure that a product meets the complete set of its requirements.

3. TERMS, DEFINITIONS AND ABBREVIATIONS

3.1 Terms and Definitions

3.1.1 Accelerated Test

A test using test conditions that are more severe than usual operating conditions.

3.1.2 Acceleration Factor

The ratio between the times necessary to obtain the same portion of failure in two equal samples under two different sets of stress conditions, involving the same failure modes and mechanisms.

3.1.3 Commodity Product

A product for which there is a demand without qualitative differentiation across a market. It is produced for a group of customers or one or several markets or application segments e.g., Standard Logic IC's or small signal transistors. For details see RVManual.

3.1.4 Component (general)

A constituent part.

NOTE 1: Examples include source and drain regions as components of transistors, lead frames and dies as components of packaged integrated circuits, resistors and integrated circuits as components of printed circuit boards, motherboards as components of computers, LCD screens as components of monitors, ac and dc components of complex waveforms, and loops and algorithms as components of software programs.

NOTE 2: Unless the context identifies the thing of which a component is a part, a descriptive prepositional phrase identifying the thing should follow the word "component".

3.1.5 Defect

A deviation in an item from some ideal state. The ideal state is usually given in a formal specification.

3.1.6 Degradation

A gradual deterioration in performance as a function of time.

3.1.7 De-rating

The intentional reduction of stress/strength ratio in the application of an item, usually for the purpose of reducing the occurrence of stress related failures.

3.1.8 Device

A piece of equipment, a mechanism, or another entity designed to serve a special purpose or perform a special function.

3.1.9 Electronic Component

A self-contained combination of electronic parts, subassemblies, or assemblies that perform an electronic function in the overall operation of equipment.

3.1.10 Extrinsic Reliability

The reliability not related to intrinsic failure mechanisms; but to process induced deviations, being random in nature.

3.1.11 Failure Mechanism

The physical, chemical or other process that results in a failure. A failure mechanism describes how a degradation process precedes, e.g., oxidation, cracking. If the driving forces are known, e.g., electric field, current density, temperature, an empirical or theoretically based acceleration model can be proposed or derived that allows for failure rate modeling.

3.1.12 Failure Mode

The effect or manner by which a failure is observed to occur. It is the effect of the failure mechanism.

3.1.13 FMEA

Failure Mode and Effects Analysis. A systematized group of activities intended to recognize, evaluate, and prioritize the potential failure of a product or process and its effects, and to identify actions that could eliminate or reduce the chance of the potential failure occurring, listed in the order of effect on the customer.

3.1.14 Go, No-Go

Attribute data, which is data that results from counting items or classifying items into distinct non-overlapping categories; in this case, pass/fail data.

3.1.15 Intrinsic Reliability

The reliability related to the inherent material properties or design, being systematic in nature.

3.1.16 Component Life Cycle

Time period between the completion of the manufacturing process of the semiconductor component and the end of life of the vehicle.

3.1.17 Life Cycle

The time span between the beginning of development (specification) and the end of production (withdrawal from the market).

3.1.18 Lifetime

The time span between initial operation and failure.

3.1.19 Matrix Lot

A wafer lot manufactured in such a way that groups of wafers are intentionally processed to create high and low extremes in several parameters important to yield, functionality and/or reliability. Examples include transistor threshold voltage, effective channel length, conductor sheet resistance and transistor beta.

3.1.20 Matrix Lot Plan

A description of the parameters and extremes of the matrix lot per wafer.

3.1.21 Mission Profile

The simplified representation of all of the relevant conditions to which the devices will be exposed in all of its intended application throughout the full life time covering production, handling, storage and transportation.

3.1.22 Operating Conditions

The conditions of environmental parameters, voltage bias, and other electrical parameters whose limits are defined in the datasheet and within which the device is expected to operate reliable.

3.1.23 Product Robustness

The ability of a product to remain in control and capable within the expected variations of inputs (application, manufacturing, transport and storage conditions).

3.1.24 Qualification

The entire process by which products or production technologies are obtained, examined and tested, and then identified as qualified.

3.1.25 Reliability Characteristic

A parameter that characterizes the probability that a device will function without failure over a specified time period or amount of use at stated conditions.

3.1.26 Reliability Characterization

The process that characterizes the probability that a device will function without failure over a specified time period or amount of usage at stated conditions.

3.1.27 Reliability Parameter

See reliability characteristic.

3.1.28 Robust Condition

A condition at which the product remains in control and capable within the expected variations of inputs (application, manufacturing, transport and storage conditions).

3.1.29 Robustness Target Value

Target of the robustness validation process.

3.1.30 Robustness Validation

The process to demonstrate the robustness of a device under a defined mission profile.

3.1.31 Safe Operating Area

The process, product, and environmental characteristics within whose limits in extremes the component is expected to operate to maintain functionality and reliability (distinguish from SOA for power transistors).

3.1.32 Semiconductor Component

Synonym for solid-state component.

3.1.33 Solid-State Component

A solid-state device that is a constituent part of a higher order assembly.

NOTE: Examples of solid-state components include DRAMs as parts of memory modules and microprocessors as parts of motherboards.

3.1.34 Solid-State Device

An electronic device whose operation depends on the properties of the integral solid semiconductor materials.

NOTE 1: Examples of solid-state devices include transistors, thyristors, transient voltage suppressors, semiconductor pressure sensors, integrated circuits, modules consisting mainly of integrated circuits such as multichips and hybrids, and memory modules such as DIMMs and SIMMs.

NOTE 2: Electromechanical devices, e.g., solenoids, breakers, wire relays, are not considered to be solid-state devices.

3.1.35 Test Vehicle

Device used for evaluating a specific failure mechanism.

3.1.36 Use Condition

Operating or environmental condition during the use time of a device.

3.1.37 Use Time

Time the product is used in the field.

3.2 Abbreviations

AEC	Automotive Electronics Council
APQP	Advanced Product Quality Planning
ASIC	Application-Specific IC
DFMEA	Design Failure Mode and Effects Analysis
DOE	Design of Experiments
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EM	Electro Migration
EOS	Electrical Overstress
FLL	Frequency Locked Loop
FMEA	Failure Mode and Effects Analysis
IC	Integrated Circuit
JSAE	Society of Automotive Engineers of Japan
OEM	Original Equipment Manufacturer (e.g., car makers are called OEMs)
PAT	Part Average Testing
PFA	Physical Failure Analysis
PFMEA	Process Failure Mode and Effects Analysis
PLL	Phase-Locked Loop
POR	Process of Record
RIF	Robustness Indicator Figure
SAE	Society of Automotive Engineers
SBA	Statistical Bin Analysis
SOA	safe operating area
TC	Temperature Cycling
TDDB	Time-Dependent Dielectric Breakdown
TTF	Time to Failure
ZVEI	Zentralverband Elektrotechnik- und Elektronikindustrie e.V. (German Electrical and Electronic Manufacturers' Association)

3.3 Definition of Robustness Validation

Robustness Validation is a process by which to demonstrate the robustness of a semiconductor component under a defined mission profile. Robustness Validation represents an approach to qualification and validation that is based on knowledge of failure mechanisms and relates to specific Mission Profiles. The knowledge gained by applying this approach leads to improvement that extends beyond the component and its manufacturing process under consideration. RV contains great potential for re-use, which contributes in its entirety to a significant increase in quality and reliability, time to market and reduction of costs. Last but not least, this will result in improvement of the competitiveness of all involved participants from the value adding chain.

A mission profile defines the conditions of use for the component in the intended application (see section 5). The mission profile establishes the basis for the Robustness Validation approach, providing necessary additional information that is not described in the datasheet. Experience shows that a simple passing on of specifications down the supply chain is inadequate for and incapable of capturing the necessary information. Rather, an interactive process including the entire value chain is needed to achieve a common understanding of and a mutual agreement on the requirements, which is a key factor for success of a project. This interactive process has to be started in the early concept and definition phase of the project. Cross-functional and inter-company communication across the entire value chain shall, therefore, be established as good practice.

TABLE 3.1 - ILLUSTRATES THE MEANING OF ROBUSTNESS VALIDATION BY CONTRASTING POSITIVE (IS) AND NEGATIVE (IS NOT) STATEMENTS

Robustness Validation IS	Robustness Validation IS NOT
A methodology	A regulation or specification
A test to failure process or end-of-life process	A test to pass/limit process
Validation of "fit for use"	Validation of "fit to standard"
An iterative process	A one off process
A process to gain knowledge of the failure mechanisms of a semiconductor component	A process to gain knowledge of where the part is functional
A measurement of product lifetime	A go/no go (attribute) measurement

4. ROBUSTNESS VALIDATION BASICS

4.1 Robustness Validation Summary

Robustness is the capability of functioning correctly or not failing under varying application and production conditions. Robustness Validation relies heavily on expertise and knowledge, and, therefore, requires detailed explanation and intensive communication among the specialists of the participants along the entire value adding chain.

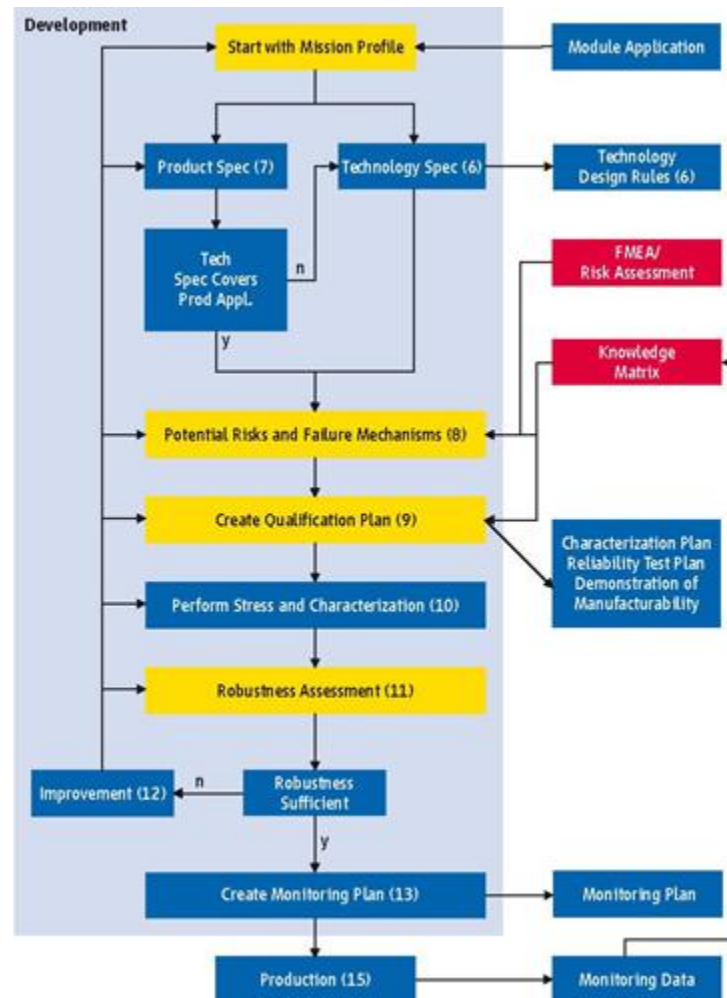
This methodology is based on three key components:

- Knowledge of the conditions of use (mission profile, see section 5)
- Knowledge of the failure mechanisms and failure modes and the possible interactions between different failure mechanisms
- Knowledge of acceleration models for the failure mechanisms needed to define and assess accelerated tests.

Robustness Validation is a knowledge-based approach [1,7,8] utilizing stress tests that are defined to address dedicated failure mechanisms using suitable test vehicles (e.g., wafer test structures, packaged parts) and specific stress conditions. If accurately applied this approach results in a product being qualified as "fit for use", and not "fit for standard" only.

4.2 Robustness Validation Flow

The Robustness Validation flow (Figure 4.1) is part of the development process. It starts with the transfer of the mission profile from the module level to the level of the semiconductor component. For details of this transfer, see Section 5. The process ends with release for mass production and definition of the related monitoring plan.



The numbers in the figure refer to sections of this document.

FIGURE 4.1 - RV QUALIFICATION PROCESS FLOW

4.3 Robustness Diagrams

Results of Robustness Validation can be represented by the use of Robustness Diagrams.

The Commodity Component Robustness Diagram, shown in figure 4.2, represents the first use of a robustness diagram, and is initiated at the conclusion of the finalization of the Mission Profile. At this point, the Semiconductor Component Supplier investigates whether the mission profile requirement can be achieved by using the relevant commodity device.

Figure 4.2 provides such a pictorial representation for two parameters, A and B, which have a certain relationship, such as voltage and temperature. Many parameters may be simple enough to plot one-dimensionally. The red box represents the area of the application's specification, which the commodity component must meet or exceed. The light blue area represents the commodity components actual performance. The Robustness Margin is the distance between any point of application specification and the point of failure of the commodity component, taking into account all variations of the product and the application's environment. The failure could result in different failure modes X, Y, Z, depending on the values of the parameters A and B. A robust component is a component that is able to maintain all the required characteristics under the conditions of use over the lifecycle without degradation to out-of-spec-values.

The Commodity Component Robustness Diagram should be reviewed with the customer to demonstrate the actual robustness of the component when developing the application FMEA.

The Application-Specific Component Robustness Diagram, shown in figure 4.3, represents the second use of a robustness diagram and is initiated at the conclusion of the Robustness Validation Stress Test. At this point, the Component Supplier demonstrates to his customer the robustness of the semiconductor component to exceed the application specification requirement.

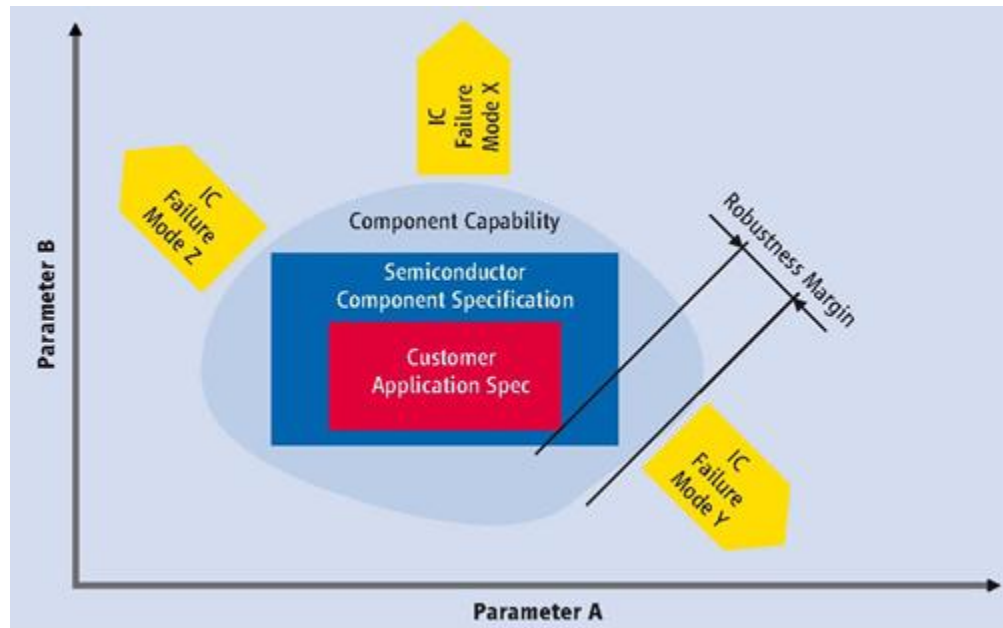


FIGURE 4.2 - ROBUSTNESS DIAGRAM FOR A COMMODITY SEMICONDUCTOR COMPONENT

The IC specification for parameters A and B can be represented by a box (in blue) that displays the minimum and maximum allowed values. Naturally, the range of parameter values for a certain application must lie within this box. However, the specification limit does not imply that the product will fail at this point. Robustness Validation identifies the point of failure for the values of (A, B). The line connecting all points of failure gives the component capability as shown by the light blue area. When any point (A_i, B_j) lies outside the component capability a failure criterion related to A, B or both parameters is violated and the semiconductor component fails. The type of failure mechanism that causes the failure depends on the parameter values and can vary along this component capability curve. Examples for parameters A and B are given in Table 4.2.

TABLE 4.2 - EXAMPLES OF PARAMETERS OF A TWO-DIMENSIONAL ROBUSTNESS DIAGRAM

Parameter A	Parameter B
Lifetime	gate oxide area
Lifetime	supply voltage
Maximum current density	junction temperature (max)
Lifetime	number of temperature cycles
Supply voltage	ambient temperature (min)
Number of temperature cycles	temperature range of cycles (T _{max} – T _{min})
Number of critical vias	lifetime

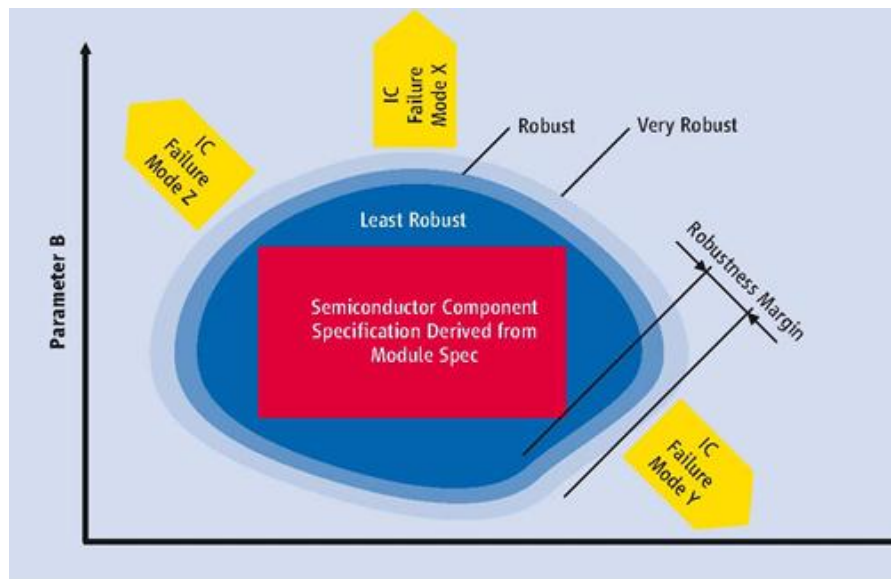


FIGURE 4.3 - APPLICATION-SPECIFIC COMPONENT ROBUSTNESS DIAGRAM.

4.4 Difference between Robustness Validation Approach and Stress Test Driven Qualification Standards

The stresses address multiple failure mechanisms and the test itself being considered pass when NO stress relevant failure occurs. Particular business fields usually require specific stress recipes, prescribed by standards specific to each of them, promoting in the most cases single failures with extrinsic defect nature. At the end these are almost neither systematic, nor relevant for the real application, and only very few intrinsic defects being triggered with relevance to the actual service life of the component. Investigations of the failures triggered by these generic tests usually require substantial effort on failure analysis and to yields almost in root cause information with less or no importance for component's actual service life. Both, effectiveness and efficiency of the stress test driven qualification may be therefore questionable.

On the other hand, the Robustness Validation approach requires the institution of wear out studies on particularly chosen tests promoting specific intrinsic failure modes and provides significant amounts of failure mechanism specific information. Detailed studies on the accordingly triggered failure mechanisms and activation energies will successfully yield in accumulation of valuable knowledge on relevant failures. This represents in consequence the basis for the Robustness Assessment and supports the calculation of the actual Robustness Margin relevant to the component application specific Mission Profile.

Thus, all the accumulated knowledge generated through testing, requested by Robustness Validation, represents is added value and the owning organization being invited to re-use it as often as requested.

In stress-based standards, all tests have fixed stress conditions over a predefined period of time (5). Only a few of the stress tests really focus on single failure mechanisms. The sample sizes are selected as a compromise between failure mechanism detection and the economies of testing and material sets. Stress time is typically chosen to address the anticipated design life of the part based on acceleration models for temperature, voltage, and humidity using mean acceleration factors. As an example, temperature acceleration is typically addressed by "average" activation energy of 0.7 eV, while the spectrum of failure mechanisms ranges from -0.2 eV to 3.3 eV. Depending on the dominating failure mechanism, the use of average values for E_a could result in misleading interpretations of stress test results. The information gleaned from these tests, while comforting when detecting zero defects, may be misleading to the customer. This is caused by the fact, that if no failures are generated:

- The actual robustness of the product being NOT known
- Acceleration factors are NOT measured
- There is no proof that the intended failure mechanisms have been triggered
- The dominant failure mechanism may not be sufficiently accelerated to demonstrate the life in the requirements.

In the past, this approach helped the customer to compare products from different suppliers and to generate a large database of stress test results performed under identical conditions. As the robustness was not known, the quality, reliability and robustness margins could not be improved effectively, or may even have been unintentionally reduced. Some examples for which traditional stress-test methodologies have been unable to detect subsequent field issues are described in section 15.1.

Development activity is now required to generate a failure mechanism risk assessment and a stress methodology that is able to characterize the failure mechanisms.

Failure Mechanism

Reliability physics differentiates between intrinsic and extrinsic failure mechanisms. The intrinsic failures can be characterized by a small sample of test devices stressed to failure, because they can be considered as physical properties of the materials used.

Extrinsic failures, on the other hand, are random in nature and a large sample size is needed to characterize the critical part of the distribution.

Defect density related failures are typical examples for the last group. Therefore, the sample size must be chosen depending on the type of failure to be addressed by a specific test and the failure rate target to be demonstrated. Extrinsic failures are mainly dominated by manufacturing performance issues and not by the product itself. Therefore, in most of the cases, a complex component like an IC does not necessarily the best vehicle to characterize or measure extrinsic kinds of failures.

On the other hand it is the main task of the IC design to ensure the expected semiconductor robustness by addressing all known intrinsic failure mechanisms and where ever possible the particular manufacturing process disturbances, too, through the accurate application of accordingly developed and engineered design rules and simulation tools integrated in the design flow.

Intrinsic failure	Extrinsic failure
Related to the inherent material properties or design	Related to process induced deviations
Systematic	Random
Wearout	Early life failures
Small sample sizes sufficient	Large sample sizes needed

Acceptance criteria

Acceptance criteria of stress-test-driven approaches are typically “test to pass”, which means that the value of the qualification statement is completely dependent on the validity of the model parameters, because quality and the reliability are not really measured. Therefore, the robustness of the product is actually not known after performing this kind of qualification. The result evaluation being of qualitative nature, as the relationship between the applied stress during the stress-test-driven qualification conditions and lifetime at conditions of use are usually not established. The sensitivity of stress-test-driven methods with respect to new or changed materials or technologies being insufficient to demonstrate robustness of a component in the harsh automotive environment.

5. MISSION PROFILE/VEHICLE REQUIREMENTS

As mentioned in the previous section, the knowledge on the actual conditions of use in the overall system of the semiconductor device under investigation represents one of the key components of Robustness Validation. The Robustness Validation process for any relevant component shall start always with the generation of the Mission Profile based on its actual conditions of use in the environment of the current, and next higher level of the component hierarchy. The supplier of the semiconductor component will develop a set of profile assumptions based on market research and/or interactions with customers to capture the majority of user application scenarios. The generation process of the Mission Profile for the component in question represents a detailed, back and forward oriented communication process across the entire value adding chain on each detail of the actual Conditions of Use in the chosen application. The primary and

overarching objective is to ensure the requested/expected quality and reliability over the entire service life of the final product of the OEM. Therefore the BEST known PRACTICE to mutually conclude in good faith for the actual realization on the best technical, reliable and cost saving trade off shall be established in order to ensure competitiveness and the necessary margin to each of the involved partners.

The ideal flow for the generation of these conditions of use is illustrated in Figure 5.1. Starting from the mission profile for the vehicle (such as a car or truck), the corresponding high-level requirements are defined. These requirements are then transferred from the different system levels, module level, and electronic control unit to the level of the semiconductor component (see Figure 5.1).

As mentioned before this shall not represent a one-direction process along the chain, but rather an interactive, iterative agile communication, up and down the entire supply chain, as specification development proceeds. Thereby the requirements become step by step more clear and shall be finally and mutually concluded by all involved parties at the point of freezing of the specification. This is still valid for the mission profile, too.

Examples of the contents of a mission profile on ECU level can be found in the paper “Automotive Application Questionnaire for Electronic Control Units and Sensors”, published by ZVEI (9).

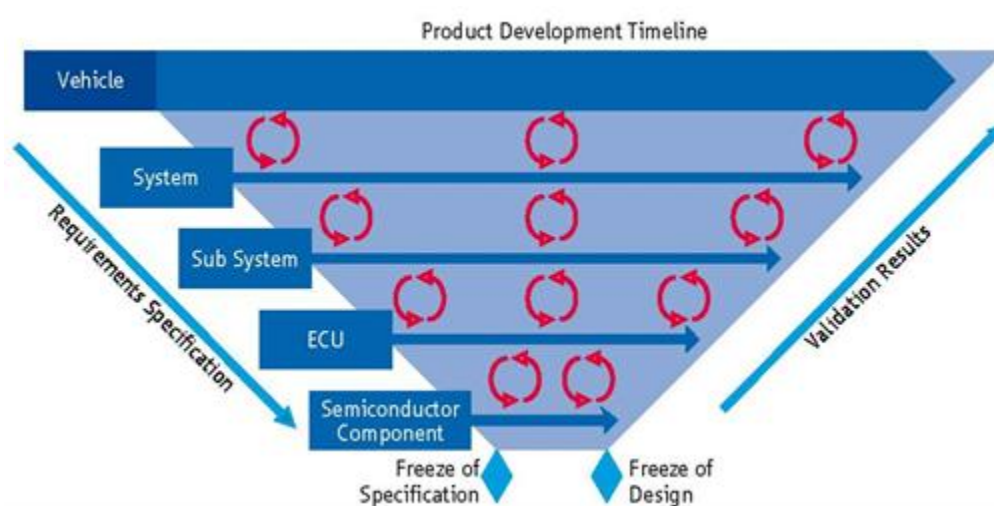


FIGURE 5.1 - PRODUCT DEVELOPMENT PROCESS

The mission profile represents the collection of all relevant environmental load/stress and conditions of use to which a component will be exposed during its full life cycle.

Life cycle is defined as the time period between the completion of the manufacturing process of the semiconductor component and the end of life of the vehicle.

The mission profile includes:

- Transport
- Storage
- Processing
- Operations in the intended application

Each of the profile items listed above can occur more than once. It is not state-of-the-art methodology to replace field application conditions by specific stress conditions. A stress test plan cannot replace the mission profile. A specific example of lifetime prediction that could be made based on mission profile is shown in reference 13.

Commodity Products vs. ASICs

In the case of commodity products, these mission profiles are usually defined without a specific user (as in the case of an ASIC), based on the intended customer base and applications. This case is similar to the case of an ASIC; the difference being that the input does not come directly from the customer but instead from internal sources (such as marketing and product definition). The definition of mission profiles for commodity products requires information and experience by the semiconductor supplier for certain applications. Contents of the mission profile shall be documented for communication to users.

Conditions of Use

The conditions of use are affected by various parameters, such as service life or mounting location. The following section provides an overview of the conditions of use and the corresponding requirements.

In the same way, a new evaluation is required if the conditions of use change for a current component; for instance, if this component shall be used in a new application.

In the following text, aspects of the mission profile are discussed in more detail.

Vehicle Service Life

The most general data concerns the vehicle service life. This comprises information on

- **Service Lifetime**

The total lifetime of the car

- **Mileage**

The total number of miles/kilometers that the car is assumed to be driven during its service life

- **Engine On Time**

The amount of time that the engine and component is switched on (key-on time) and operational during the service lifetime

- **Engine Off Time**

The amount of time that the engine is switched off while several applications are running (such as the radio on)

- **Non-operating time**

The amount of time remaining by subtracting engine-on and engine-off time from the total service lifetime

An example of this kind of data is given in Table 5.1 below.

TABLE 5.1 - EXAMPLE OF OEM VEHICLE MISSION PROFILE PARAMETERS – (HIGH-LEVEL)

Service Lifetime	Mileage	Engine On Time	Engine Off Time	Non-operating Time	Engine On/Off Cycles
15 years	600,000 km	12,000 h	3,000 h	116,400 h	50k (w/o start-stop) > 300 k (w start-stop)

NOTE: There are applications that operate continuously during, non-operating" time (such as, theft protection, alarm system)

Environmental Conditions and Stress/Load Factors

The environmental conditions can be classified into four main categories as listed below:

Thermal Conditions

- Seasonal/daily variation of outside temperature and extremes
- Ambient temperature inside ECU
- Junction temperature

Electrical Conditions

- Voltage
- Current
- Energy (transients)
- Electric field
- Magnetic field

Mechanical Conditions

- Vibration
- Shock
- External load, such as pressure or tensile forces

Other Conditions

- Chemical reactions
- Humidity
- Radiation
- Electromagnetic radiation
- Particle radiation

NOTE: All load factors can be static or dynamic and can have spatial gradients that must be taken into account.

Thermal Conditions

The various levels of component integration require a clear understanding and definition of the meaning of the temperature under consideration. Figure 5.2 indicates the locations of different possible points for temperature measurement for different levels of integration.

The temperature measurement locations at the points defined in the Figure 5.2 can be used to describe the thermal conditions in the ECU and the semiconductor components. The temperatures are defined as follows:

T_{Vehicle Mounting Location Ambient}:

Temperature at 1 cm distance from the ECU package.