



SURFACE VEHICLE RECOMMENDED PRACTICE

J1939™-11

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Superseding J1939-11 SEP2012

Physical Layer, 250 Kbps, Twisted Shielded Pair

RATIONALE

Document is revised to allow additional color combinations to denote SAE J1939 networks, to clarify connector pin labeling, and update references and terminology for consistency with ISO 11898-1:2015.

FOREWORD

The set of SAE J1939 Recommended Practice documents define a high speed ISO 11898 CAN protocol based communications network that can support real-time closed loop control functions, simple information exchanges, and diagnostic data exchanges between Electronic Control Units (ECUs) physically distributed throughout the vehicle.

The SAE J1939 communications network is developed for use in heavy-duty environments and suitable for use in horizontally integrated vehicle industries. The physical layer aspects of SAE J1939 reflect its design goal for use in heavy-duty environments. Horizontally integrated vehicles involve the integration of different combinations of loose package components, such as engines and transmissions, which are sourced from many different component suppliers. The SAE J1939 common communication architecture strives to offer an open interconnect system that allows the ECUs associated with different component manufacturers to communicate with each other.

The SAE J1939 communications network is intended for light-duty, medium-duty, and heavy-duty vehicles used on-road or off-road, and for appropriate stationary applications which use vehicle derived components (e.g., generator sets). Vehicles of interest include, but are not limited to, on-highway and off-highway trucks and their trailers, construction equipment, and agricultural equipment and implements.

This set of SAE Recommended Practices has been developed by the SAE Truck and Bus Control and Communications Network Committee of the SAE Truck and Bus Electrical and Electronics Steering Committee. The SAE J1939 communications network is defined using a collection of individual SAE J1939 documents based upon the layers of the Open System Interconnect (OSI) model for computer communications architecture. These SAE J1939 documents are intended as a guide toward standard practice and are subject to change to keep pace with experience and technical advances.

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1. SCOPE

This document defines a physical layer having a robust immunity to EMI and physical properties suitable for harsh environments.

CAN controllers are available which support the CAN Flexible Data Rate Frame Format. These controllers, when used on SAE J1939-11 networks, must be restricted to use only the Classical Frame Format compliant to ISO 11898-1:2015.

These SAE Recommended Practices are intended for light- and heavy-duty vehicles on- or off-road as well as appropriate stationary applications which use vehicle derived components (e.g., generator sets). Vehicles of interest include but are not limited to: on- and off-highway trucks and their trailers; construction equipment; and agricultural equipment and implements.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of SAE publications shall apply.

2.1.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or +1 724-776-4970 (outside USA), www.sae.org.

SAE J1113-13 Electromagnetic Compatibility Measurement Procedure for Vehicle Components -Part 13: Immunity to Electrostatic Discharge

SAE J1128 Low Voltage Primary Cable

SAE J1939 Serial Control and Communications Heavy Duty Vehicle Network - Top Level Document

SAE J1939-13 Off-Board Diagnostic Connector

SAE J1939-16 Automatic Baud Rate Detection

SAE AS85485 Cable, Electric, Filter Line, Radio Frequency Absorptive

2.1.2 ISO Publications

Copies of these documents are available online at <http://webstore.ansi.org/>

ISO 11898-1:2015 Road vehicles -- Controller area network (CAN) -- Part 1: Data link layer and physical signalling

ISO 11898-2:2016 Road vehicles - Controller area network (CAN) - Part 2: High-speed medium access unit.

ISO 6722-1 Road vehicles - 60 V and 600 V single-core cables - Part 1: Dimensions, test methods and requirements for copper conductor cables

3. NETWORK PHYSICAL DESCRIPTION

3.1 Physical Layer

The physical layer is a realization of an electrical connection of a number of ECUs (Electronic Control Units) to a network. The total number of ECUs will be limited by electrical loads on the bus line. This maximum number of ECUs is fixed to 30, on a given segment, due to the definition of the electrical parameters given in the present specification

3.2 Physical Media

This document defines a physical media of shielded twisted pair. These 2 wires have a characteristic impedance of 120 Ω and are symmetrically driven with respect to the electrical currents. The designations of the individual wires are CAN_H and CAN_L. The names of the corresponding pins of the ECUs are also denoted by CAN_H and CAN_L, respectively. The third connection for the termination of the shield is denoted by CAN_SHLD.

3.3 Differential Voltage

The voltages of CAN_H and CAN_L relative to ground of each individual ECU are denoted by V_{CAN_H} and V_{CAN_L} . The differential voltage between V_{CAN_H} and V_{CAN_L} is defined by Equation 1:

$$V_{diff} = V_{CAN_H} - V_{CAN_L} \quad (\text{Eq. 1})$$

3.4 Bus Levels

The bus lines can have one of the two logical states, recessive or dominant (see Figure 1). In the recessive state, V_{CAN_H} and V_{CAN_L} are fixed to a mean voltage level. V_{diff} is approximately zero on a terminated bus. The recessive state is transmitted during bus idle or a recessive bit.

The dominant state is represented by a differential voltage greater than a minimum threshold. The dominant state overwrites the recessive state and is transmitted during a dominant bit.

3.5 Bus Levels During Arbitration

A dominant and recessive bit imposed on the bus lines during a given bit time by two different ECUs will result in a dominant bit.

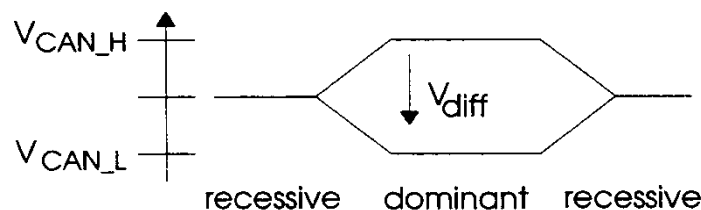


Figure 1 - Physical bit representation

3.6 Common Mode Bus Voltage Range

The common mode bus voltage is defined as the boundary voltage levels of CAN_H and CAN_L, measured with respect to the individual ground of each ECU, for which proper operation is guaranteed when all ECUs are connected to the bus line.

3.7 Bus Termination

The bus line is electrically terminated at each end with a load resistor denoted by R_L (see Figure 2). Type I ECUs shall not contain the bus termination resistor R_L . Type II ECUs shall contain the bus termination resistor or split termination, and if used shall be located only at one or both ends of a network. Type II ECUs shall be clearly marked as specified in Section 5.2.5. (Also see 5.2.3 for resistor characteristics.)

3.8 Internal Resistance

The internal resistance, R_{in} , of an ECU is defined as the resistance between CAN_H (or CAN_L) and ground during the recessive state, with the ECU disconnected from the bus line (see Figure 3).

3.9 Differential Internal Resistance

The differential internal resistance, R_{diff} , is defined as the resistance between CAN_H and CAN_L during the recessive state, with the ECU disconnected from the bus line (see Figure 4).

3.10 Internal Capacitance

The internal capacitance, C_{in} , of an ECU is defined as the capacitance between CAN_H (or CAN_L) and ground during the recessive state, with the ECU disconnected from the bus line (see Figure 3).

3.11 Differential Internal Capacitance

The differential internal capacitance, C_{diff} , of an ECU is defined as the capacitance between CAN_H and CAN_L during the recessive state, with the ECU disconnected from the bus line (see Figure 4).

3.12 Bit Time

The nominal bit time, t_B , (duration of one bit in the arbitration phase) and data bit time, t_D , (duration of one bit in the data phase) for this document is 4 microseconds corresponding to 250 kbps. Bus management functions executed within this bit time, such as ECU synchronization behavior, network transmission delay compensation, and sample point positioning, are defined by the programmable bit timing logic of the CAN protocol IC (Integrated Circuit). See Figure 5.

Various names for the bit segments are used by suppliers of CAN protocol ICs and it is possible that two bit segments are defined as one.

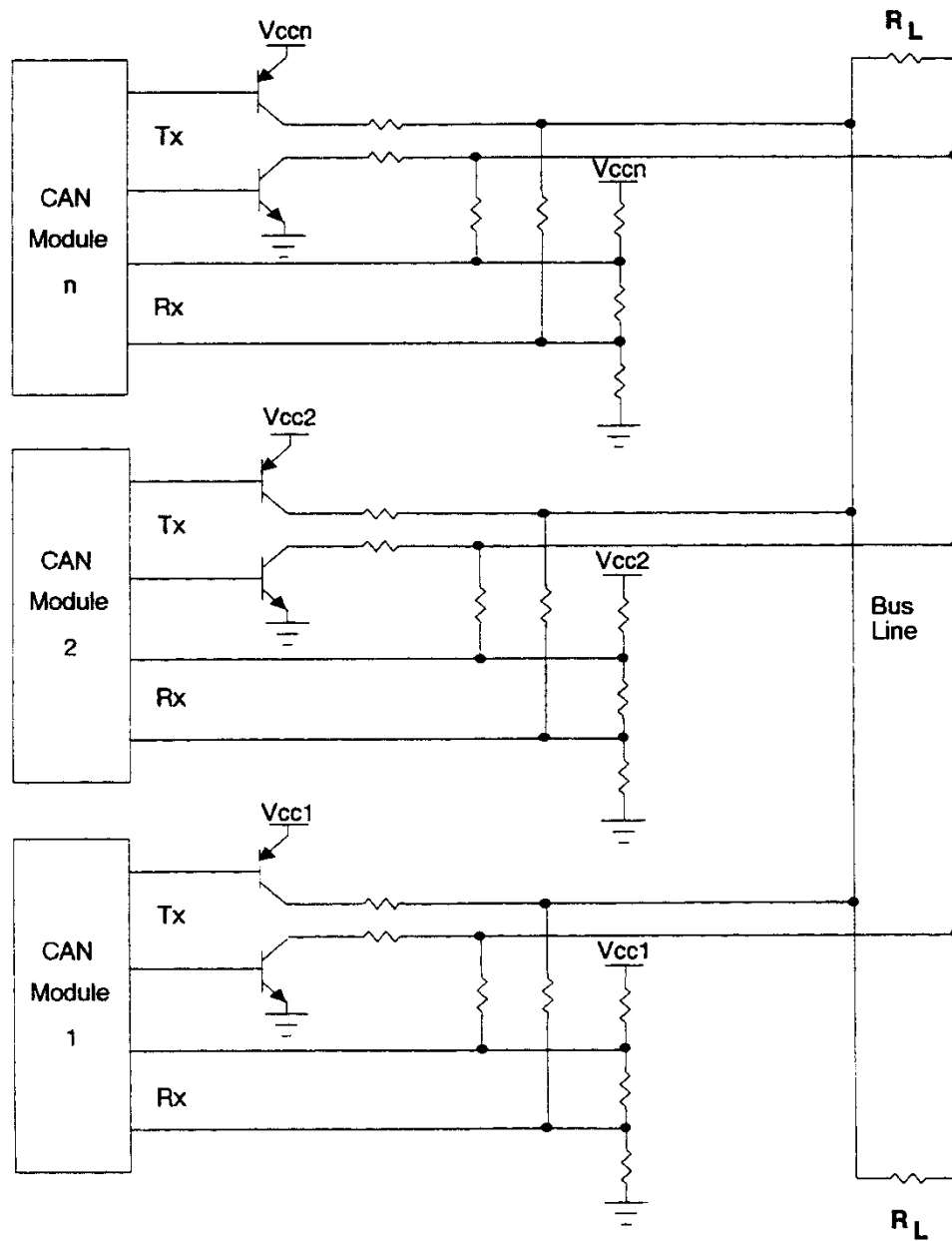


Figure 2 - Physical layer functional

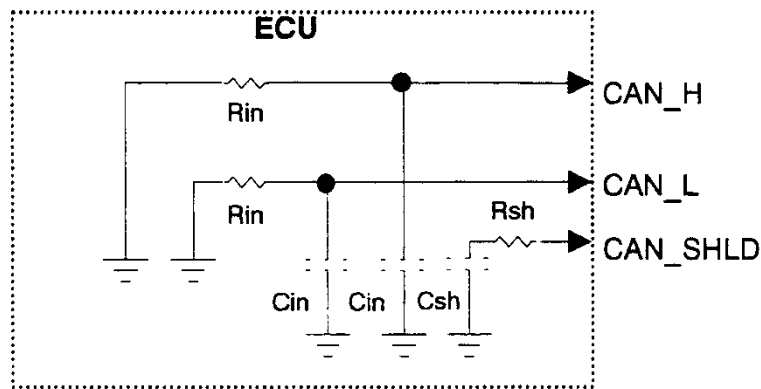


Figure 3 - Illustration of internal capacitance and resistance of an ECU in the recessive state

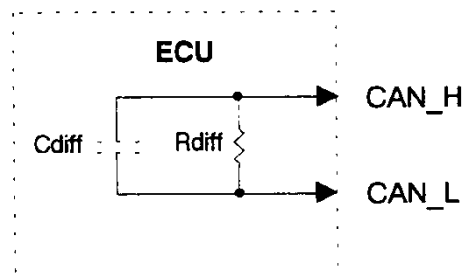


Figure 4 - Illustration of differential internal capacitance and resistance of an ECU in the recessive state

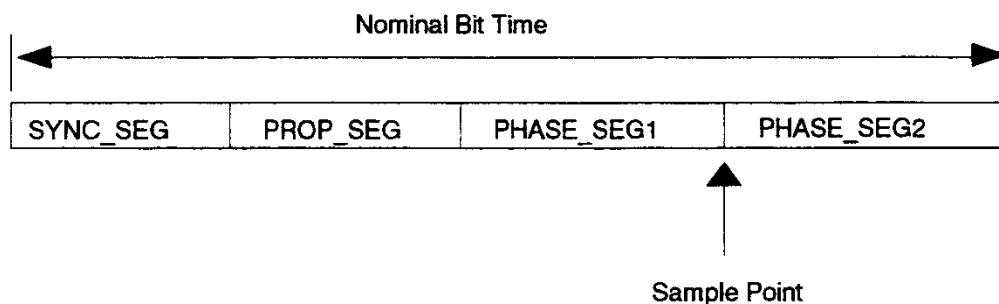


Figure 5 - Partition of the bit

- SYNC SEG - This part of the bit time is used to synchronize the various ECUs on the bus. An edge is expected within this bit segment.
- PROP SEG - This part of the bit time is used to compensate for the physical delay times within the network. These delay times are caused by the propagation time of the bus line and the internal delay time of the ECUs.
- PHASE SEG1, PHASE SEG2 - These Phase-Buffer-Segments are used to compensate for phase-errors and can be lengthened or shortened by resynchronization.
- Sample-Point - The Sample-Point is the point of time at which the bus level is read and interpreted as the value of that respective bit. Its location is at the end of PHASE_SEG1.

3.13 Internal Delay Time

The internal delay time of an ECU, t_{ECU} , is defined as the sum of all asynchronous delays that occur along the transmission and reception path of the individual ECUs, relative to the bit timing logic unit of the protocol IC.

- a. Synchronization - Hard Synchronization and Resynchronization are the two forms of synchronization. They obey the following rules:
 1. Only one Synchronization within one bit time is allowed.
 2. An edge will be used for Synchronization only if the value detected at the previous Sample Point (previously read bus value) differs from the bus value immediately after the edge.
 3. Hard Synchronization is performed during said edge whenever there is a 'recessive' to 'dominant' edge.
 4. All other 'recessive' to 'dominant' edges fulfilling rules 1 and 2 will be used for Resynchronization with the exception that a transmitter will not perform Resynchronization as a result of a 'recessive' to 'dominant' edge with a positive Phase Error if only 'recessive' to 'dominant' edges are used for Resynchronization.
- b. Synchronization Jump Width (SJW) - As a result of Synchronization PHASE_SEG1 may be lengthened or PHASE_SEG2 may be shortened. The amount of lengthening or shortening of the Phase Buffer bit Segments has an upper bound given by the Synchronization Jump Width. The Synchronization Jump Width is less than or equal to PHASE_SEG1.

3.14 CAN Bit Timing Requirements

It is necessary to ensure that a reliable network can be constructed with components from multiple suppliers. Without any bit timing restrictions, different devices may not be able to properly receive and interpret valid messages. Under certain network conditions it may also be possible for a particular device to have unfair access to the network. In addition, it makes network management (system diagnostics) much more difficult. CAN chip suppliers also recommend that all devices on a given network be programmed with the same bit timing values.

All CAN ICs divide the bit time into smaller sections defined as T_q (time quantum). For many CAN ICs 1 T_q = 250 ns (with a 16 MHz clock) (determined by oscillator frequency and baud rate prescaler).

Therefore specific values for the bit timing registers need to be defined to ensure that a reliable network exists for all nodes based on the best tradeoffs between propagation delay and clock tolerance. Note that there are some differences in bit segment definition between manufacturers of CAN devices.

It is recommended that a t_q be selected which permits the sample point (see Figure 5) to be located as close to but not later than 7/8 of a bit time (0.875×4 microseconds = 3.5 microseconds). This provides the best tradeoff between propagation delay and clock tolerance.

The following values are recommended for typical controller ICs running at standard clock frequencies. At other frequencies, different values may have to be selected to maintain the sample point as close as possible but not later than the preferred time.

Table 1 – Example bit timing parameters

Oscillator (MHz)	NQ (T_q /bit)	T_q (ns)	Sync_Seg (T_q)	SJW (T_q)	TSEG1 (T_q)	TSEG2 (T_q)	Sample Point
16	16	250	1	1	13	2	87.5%
20	20	200	1	1	16	3	85.0%
40	20	200	1	1	16	3	85.0%
80	20	200	1	1	16	3	85.0%

The bit timing values for the 40 and 80 MHz example are the same as the 20 MHz example. The number of time quanta is limited by the controller and is usually between 8 and 25. The baud rate prescaler is used to divide the oscillator frequency such the number of time quanta adding up to the bit time is within this range.

$SJW = 1 \text{ tq}$ (SJW is a part of TSEG1 and TSEG2)

Total Bit Time = TSEG1 + TSEG2 + Tsyncseg = 13 + 2 + 1 = 16 tq = 4 microseconds

(Example for 16 MHz clock)

PROP_SEG + PHASE_SEG1 = TSEG1

PHASE_SEG2 = TSEG2,

SYNC_SEG = SYNC_SEG

This selection for the bit timing registers generally requires the use of crystal oscillators at all nodes so that the clock tolerance given in Table 2 can be achieved.

Table 2 - AC parameters of an ECU disconnected from the bus line

Parameter	Symbol	Min.	Nom	Max.	Unit	Conditions
Bit time ⁽¹⁾	t_B	3.998	4.000	4.002	μs	250 Kbps
Data bit time ⁽¹⁾	t_D	3.998	4.000	4.002	μs	250 Kbps
Internal Delay Time ⁽²⁾	t_{ECU}	0.0		0.7	μs	
Internal Capacitance ⁽³⁾	C_{in}	0	50	100	pF	250 Kbps for CAN_H and CAN_L relative to Ground
Differential Internal Capacitance ⁽³⁾	C_{diff}	0	25	50	pF	
Available Time ⁽⁴⁾	t_{avail}	2.5			μs	40 m bus length
Signal Rise, Fall Time ⁽⁵⁾	t_R, t_F	200		500	ns	measured from 10% to 90% of the signal
Signal Rise, Fall Time ⁽⁵⁾	t_R, t_F	200		500	ns	measured from 10% to 90% of the signal

1. Including initial tolerance, temperature, aging, etc.
2. The value of t_{ECU} has to be guaranteed for a differential voltage of $V_{\text{diff}} = 1.0 \text{ V}$ for a transition from recessive to dominant and of $V_{\text{diff}} = 0.5 \text{ V}$ for a transition from dominant to recessive. With the bit timing from the example of note 1, a CAN-Interface delay of 500 ns is possible (controller not included) with a reserve of about 300 ns. This allows slower slopes (R1 in Figure A.1) and input filtering. It is recommended to use this feature due to EMC.
The minimal internal delay time may be zero. The maximum tolerable value is determined by the bit timing and the bus delay time.
3. In addition to the internal capacitance restrictions a bus connection should also have an inductance as low as possible. The minimum values of C_{in} and C_{diff} may be 0, the maximum tolerable values are determined by the bit timing and the network topology parameters l and d (see Table 9). Proper functionality is guaranteed if occurring cable resonant waves do not suppress the dominant differential voltage level below $V_{\text{diff}} = 1 \text{ V}$ and do not increase the recessive differential voltage level above $V_{\text{diff}} = 0.5 \text{ V}$ at each individual ECU (see Tables 4 and 5).
4. The available time results from the bit timing unit of the protocol IC. For example, this time in most controller ICs corresponds to TSEG1. Due to mis-synchronization it is possible to lose the length of SJW. So the available time (t_{avail}) with one mis-synchronization is TSEG1-SJW ms. A tq time of 250 ns and SJW = 1 tq, TSEG1 = 13 tq, TSEG2 = 2tq results in $t_{\text{avail}} = 3.00 \mu\text{s}$.
5. The load on the ECU for the purpose of this parameter should be 60 Ω between CAN_H and CAN_L in parallel with 200 pf of capacitance