

SURFACE VEHICLE RECOMMENDED PRACTICE

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Universal Interface for OBD II Scan

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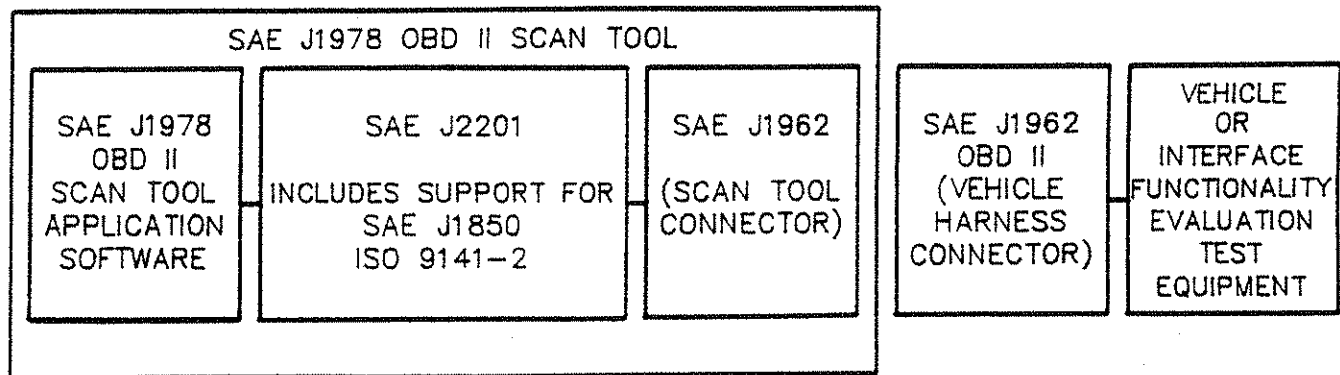
1. **Scope**—SAE J1978 defines the requirements of the OBD II scan tool. SAE J2201 defines the minimum requirements of the vehicle communications interface for the SAE J1978 OBD II scan tool. This interface connects the SAE J1962 test equipment connector to the hardware/software of the SAE J1978 OBD II scan tool that will use this interface to communicate with vehicles for the purpose of accessing required OBD II functions.

Included in this SAE Recommended Practice are several definitions relating to the interface, and interface functionality evaluation.

Appendix A - Examples include several example interface circuit implementations, which are believed to meet the requirements of this document and of SAE J1978. These examples are NOT requirements of this document. They are provided to assist circuit designers in developing interface circuits.

Appendix B - Supporting Documents includes a list of supporting documents for the examples shown in Appendix A.

- 1.1 **SAE Document Interrelationships**—Figure 1 shows the interrelationships between SAE J1978, SAE J1962, and this document.



NOTE—See SAE J1962 Diagnostic Connector for pin assignments.

FIGURE 1—SAE DOCUMENT INTERRELATIONSHIPS

Where any conflict may exist between the requirements contained in SAE J1978 and this document, SAE J1978 is the overriding document.

2. References

2.1 Applicable Publications—The terms, definitions, abbreviations, and acronyms contained in SAE J1930 are included by reference.

The following publications form a part of this specification to the extent specified herein. The latest issue of SAE publications shall apply.

2.1.1 SAE PUBLICATIONS—Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

SAE J1850—Class B Data Communication Network Interface
 SAE J1930—Electrical/Electronic Terms, Definitions, Abbreviations, and Acronyms
 SAE J1962—Diagnostic Connector
 SAE J1978—OBD II Scan Tool
 SAE J1979—Diagnostic Test Modes
 SAE J2205—Expanded Diagnostic Protocol

2.1.2 CALIFORNIA AIR RESOURCE BOARD PUBLICATIONS—Available from California Air Resource Board Documents

California Code of Regulation, Title 13, 1968.1—Malfunction and Diagnostic System Requirements - 1994 and Subsequent Model-Year Passenger Cars, Light-Duty Trucks, and Medium-Duty Vehicles With Feedback Fuel Control Systems

2.1.3 EPA REGULATIONS—Available from EPA

Federal Register Tuesday September 24, 1991, Part II Environmental Protection Agency 40 CFR Part 86—Air Pollution Control; New Motor Vehicles and Engines: On-Board Diagnostic Systems on 1994 and Later Model Year Light-Duty Vehicles and Light-Duty Trucks; Proposed Rule

2.1.4 ISO PUBLICATIONS—Available from ANSI, 11 West 42nd Street, New York, NY 10036-8002.

ISO 9141-2—Road vehicles—Diagnostic systems—CARB requirements for interchange of digital information ISO/TC 22/SC 3/WG 1 - N 425 E/REV April 1991

3. Definitions

- 3.1 **Application Software**—As used in this document, this term refers to the microprocessor programming that controls the external equipment/scan tool hardware so as to perform required SAE J1978 OBD II Scan Tool functions.
- 3.2 **DLCS**—(Data Link Controller Serial) refers to the integrated circuit family developed by General Motors that supports SAE J1850 10.4 Kbps VPW CRC communication.
- 3.3 **HBCC**—(Hosted Bus Controller Circuit) refers to the integrated circuit developed by Ford Motor Co. that supports SAE J1850 41.6 Kbps PWM CRC communication.
- 3.4 **OBD II**—(On Board Diagnostics II) common term that refers to the requirements of the California legislation-California Code of Regulation, Title 13, 1968.1.
- 3.5 **PCI**—(Programmable Communications Interface) refers to a set of integrated circuits which includes a control microcomputer, the Symbol Encoder Decoder (SED) and the Integrated Driver Receiver (IDR). The PCI was developed by Chrysler Corporation and supports SAE J1850 10.4 VPW communication with both CRC and Checksum error techniques.
- 3.6 **JCI**—(SAE J1850 Communications Interface) refers to an integrated circuit manufactured by Motorola which supports both SAE J1850 10.4 VPW with CRC and SAE J1850 41.6 PWM with CRC communication.

4. Acronyms and Abbreviations

CRC - Cyclic Redundancy Check
CS - Checksum
EDP - Enhanced Diagnostic Protocol (SAE J2205)
IBS - Inter-Byte Separation
IFR - In-Frame Response
NRZ - Non Return to Zero
PWM - Pulse Width Modulation
SCI - Serial Communications Interface
SPI - Serial Peripheral Interface
UART - Universal Asynchronous Receiver/Transmitter
VDD - 5.0 VDC from Regulated Power Supply
VPW - Variable Pulse Width Modulation
"~" - Indicates Active Low Signals

5. **Requirements**—This section defines the required message structure support, signal ground, chassis ground, minimum scan tool connector cable length, and other requirements for the interface to be used by an SAE J1978 OBD II scan tool.

- 5.1 **Interface and Message Protocol Support**—The interface defined in this document must support the interface requirements and message protocol requirements of SAE J1978.
- 5.2 **In-Frame Response**—When a single byte in-frame response (IFR) is required during the reception of a 41.6 Kbps PWM SAE J1979 message, the interface will support the transmission of the node address as a single byte IFR.

5.3 Signal Ground—The Signal Ground pin of the scan tool side of the SAE J1962 diagnostic connector must be used as the signal ground reference for all interface transceivers required by this document.

5.4 Maximum Voltage Differentials—The interface described in this document includes any required interface transceivers and the cabling connecting the interface transceivers to the scan tool side of the SAE J1962 connector. Any interface connected to a vehicle through the SAE J1962 diagnostic connector is considered a part of the vehicle network and must operate within the limits of that network, which are described in SAE J1850 and ISO 9141-2.

The maximum voltage differential, e.g., due to load current, noise, etc., between any two nodes of a vehicle data communication network, where the interface described in this document is considered as a node on the vehicle network when connected to the vehicle, must be less than the limits specified in SAE J1850 and ISO 9141-2.

The following are maximum voltage differential values for the interface described in this document (as measured between the signal ground connection of all interface transceivers and the Signal Ground pin on the vehicle side of the SAE J1962 diagnostic connector) are:

0.25 V peak noise
0.1 VDC offset

5.5 Chassis Ground—The Chassis Ground pin of the scan tool side of the SAE J1962 diagnostic connector is available for any use, with the exception that the minimum DC impedance between the Chassis Ground and the Signal Ground is 1 M Ω .

5.6 Minimum Connector Cable Length—The minimum length between the ground reference connection of each interface transceiver and the Signal Ground connection of the vehicle side of the SAE J1962 diagnostic connector is 2 m.

5.7 Other Requirements—The interface must support the requirements of SAE J1850, SAE J1962, SAE J1978, SAE J1979, SAE J2205, and ISO 9141-2.

6. Interface Functionality Evaluations—The functionality of any proposed interface implementations must be evaluated by either of the following:

- a. The use of multiplex bus interface equipment from I + ME, or equivalent equipment, that with appropriate software simulates vehicles that use the required implementations of SAE J1850 and ISO 9141-2, or
- b. The use of representative vehicles of motor vehicle manufacturers that use the required implementations of SAE J1850 and ISO 9141-2.

PREPARED BY THE SAE VEHICLE E/E SYSTEM DIAGNOSTICS STANDARDS COMMITTEE

APPENDIX A

EXAMPLES

A.1 General Example Information—This section shows example interface implementations that are believed to meet the requirements of this document.

These examples are NOT requirements of this document. These examples are intended as an assist to interface circuit designers.

Table A1 illustrates a summary of some of the capabilities available with these examples that are over and above the requirements of this document and some that are required.

TABLE A1—SUMMARY OF CAPABILITIES FOR THE FOLLOWING EXAMPLES

	DLCS & HBCC Section A.2	PCI & HBCC Section A.3	ST9 Section A.4	F690 & F691 Section A.5	JCI Section A.6
Error Checking	CRC	CS & CRC	CS & CRC	CS & CRC	CRC
Comprehends IBS ⁽¹⁾	No	Yes	Yes	Yes	No
Header Bytes	3	1 & 3	1 & 3	1 & 3	3
Generate Break	Yes	Yes	Yes	Yes	Yes
Control Function ⁽²⁾	No	Yes	Yes	No	No
Host Required	Yes	Optional ⁽³⁾	Optional ⁽³⁾	Yes	Yes

1. IBS is part of only 10.4 Kbps VPW networks. It is not a part of 41.6 Kbps PWM networks, nor a part of ISO 9141–2 networks.

2. Control Function refers to parts of an interface that are implemented in software and executed by some form of microcomputer.

3. Host Required refers to the need for a host microcomputer to perform the functionality of SAE J1978. Some interface implementations include a microcomputer as a part of the interface. In some of these implementations, this microcomputer may have enough excess capability so as to also be able to perform "host microcomputer" functions.

Error checking (CS or CRC), IBS, header bytes, and the Break signal are defined in SAE J1850.

A.1.1 Transient Protection—While some of the examples may show transient protection, this document does not specify or require transient protection.

A.1.2 Host Support Not Included—The examples shown here support a nominal type of host interface and are not meant to be directly applicable to any particular host microprocessor, host interface, and/or host software. The host application software (e.g., interface drivers, message building routines, message processing routines, etc.) and/or additional hardware (e.g., signal buffers, signal inverters, clock synchronization circuits, etc.) required to complete the interface to the example circuits shown in this document is the responsibility of the designer/implementer and is not shown here.

A.1.3 Supporting Documents—Appendix B - Supporting Documents identifies documentation that may be used to aid in the understanding of the examples shown in this document.

A.1.4 Common ISO 9141-2 Support—Many of the examples include a common implementation for ISO 9141-2. This common implementation is described here (see Figure 2-D ISO 9141-2).

The ISO 9141-2 document describes the requirements of the ISO 9141-2 interface. This interface is an asynchronous serial communication link using NRZ bit encoding. A 5 bps bit rate is used during module communication initialization and a 10.4 Kbps bit rate is used for all further communications.

This interface includes a K line which is bidirectional and used for all communication phases, and a L line which is output only from the scan tool and is only used during the 5 bps module communication initialization phase. When used to transmit data to a vehicle, both the L and K lines are driven to either ground or battery level, through a 510 Ω resistor, depending on the data value. When used to receive data from a vehicle, the K line is referenced to 1/2 the battery voltage, with a small amount of hysteresis for noise immunity, to determine the logic value of the data being transmitted by a vehicle module.

In all of the examples, the L and K lines are connected to the SCI port of either the host or a control microprocessor. A select signal from the host/control microprocessor is used to enable the L line when necessary.

A.1.5 Electromagnetic Compatibility—The Electromagnetic Compatibility (EMC) characteristics of these examples have not been investigated nor estimated. The ability of the examples to meet EMC or noise radiation requirements is unknown.

A.1.6 No Responsibility Assumed by Contributors—No responsibility is assumed by Chrysler Corporation, Ford Motor Co., General Motors Corporation, Delco Electronics Corporation, SAE, SGS-Thomson, Silicon Systems, Motorola, or any other company for use of any of the examples or products shown in this document nor for any infringements of patents and trademarks or other rights of other parties resulting from the use of these examples or products. No license is granted under any patents, patent rights, or trademarks of the previously named parties.

A.1.7 Additional Capabilities of Examples—Many of the examples support capabilities beyond the requirements of this document. Such capabilities are discussed in a separate section of each example.

A.2 DLCS, HBCC, and ISO 9141-2 Interface Example—This example (see Figure A1a) combines the use of the Data Link Controller Serial (DLCS) integrated circuit developed by Delco Electronics, the Hosted Bus Controller Circuit (HBCC) integrated circuit developed by Ford, a discrete 41.6 Kbps transmit driver, and the common ISO 9141-2 interface to provide the required interface support. (Figure A1b shows the detail of the DLCS, Figure A1c shows the detail of the HBCC with its Transmit Driver, and Figure A1d shows the detail for the common ISO 9141-2.)

The DLCS and HBCC communicate with the host through the host's SPI port, while the ISO 9141-2 interface communicates with the host through the host's SCI port. Separate logic interface lines are used by the host to individually select communication between the host and either the DLCS and HBCC, and to enable the L line.

A.2.1 General Overview—The DLCS and HBCC perform as communication peripheral integrated circuits. Following initialization, they isolate the host from bus communications tasks and are only serviced by the host when the host is loading a message for transmission or unloading a received message. The host receives an interrupt when a received message is available and when message transmission is completed. The host only handles communications as full messages. Several control and status registers are available in both the DLCS and HBCC to control their operation and indicate the status of their communications tasks.

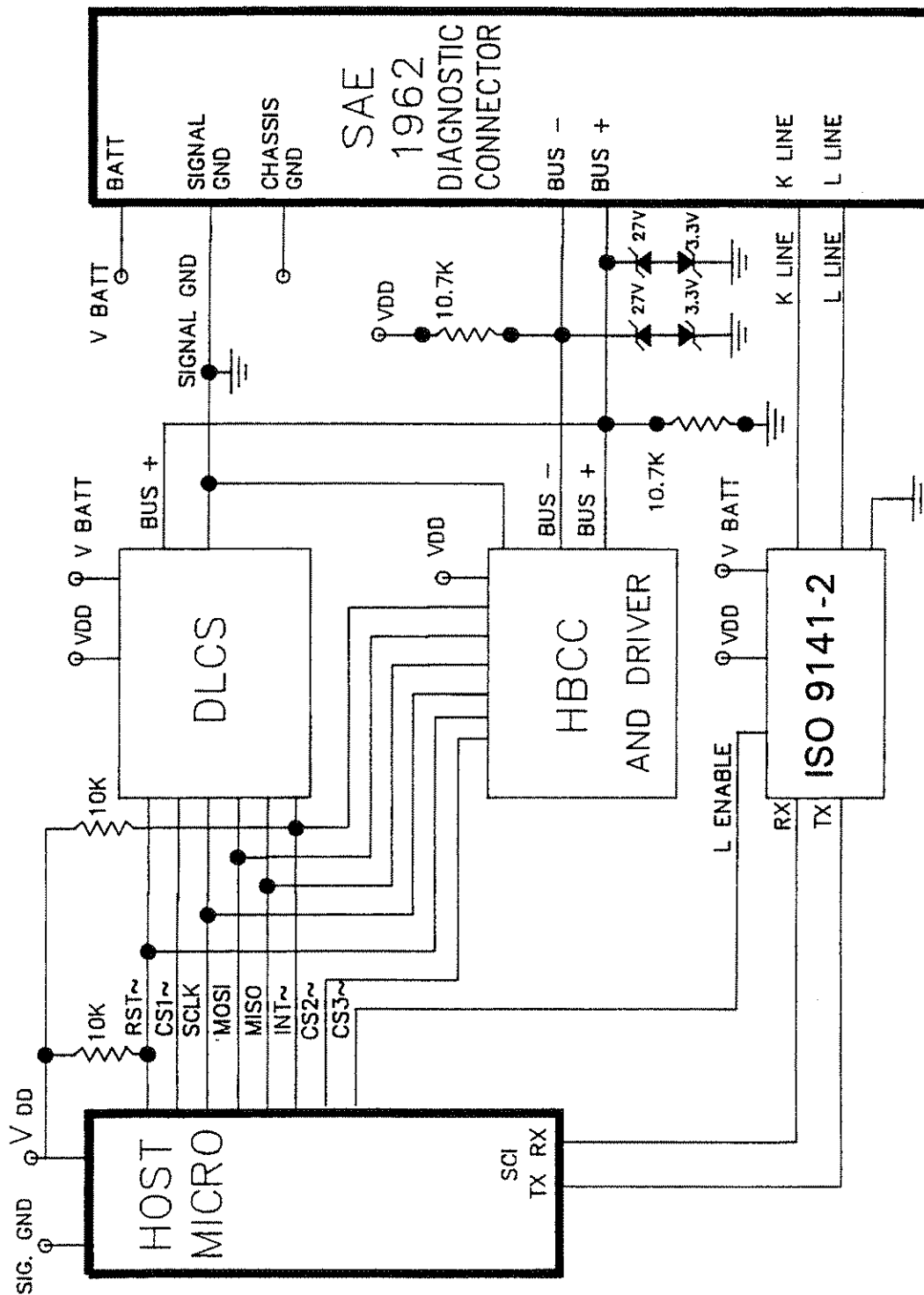


FIGURE A1A—DLCS, HBCC, AND ISO 9141-2 EXAMPLE

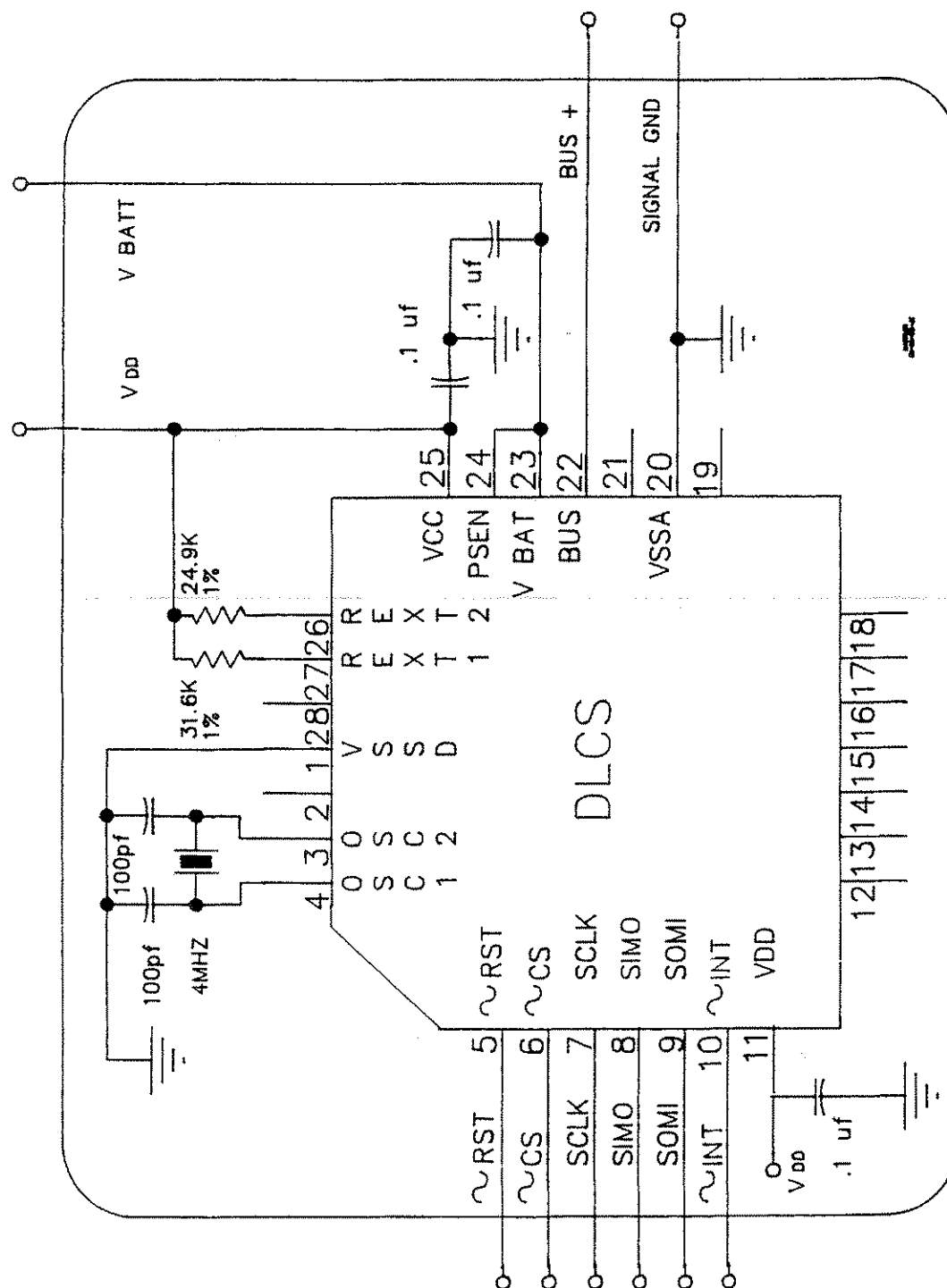


FIGURE A1B—DLCS DETAIL

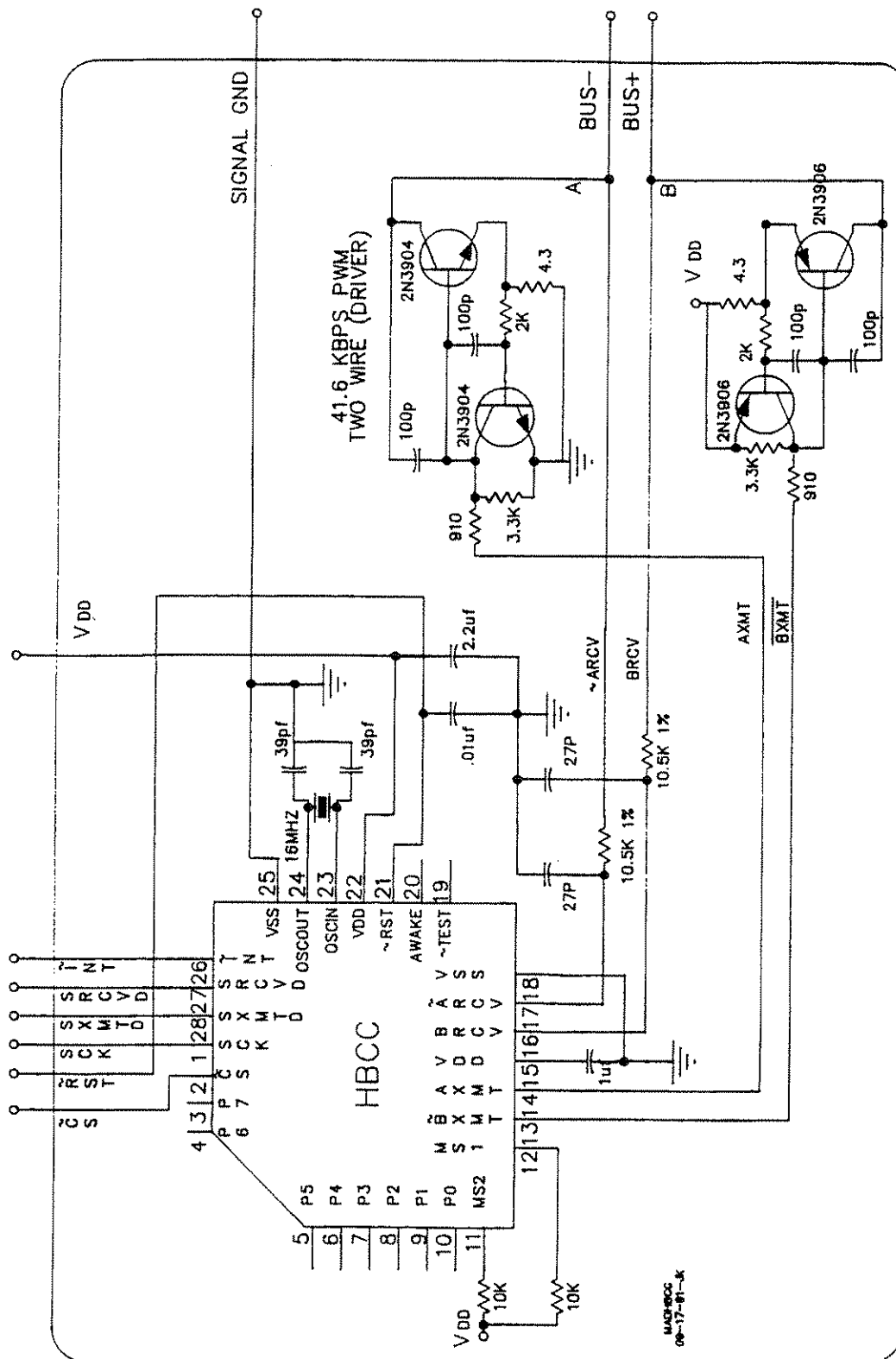
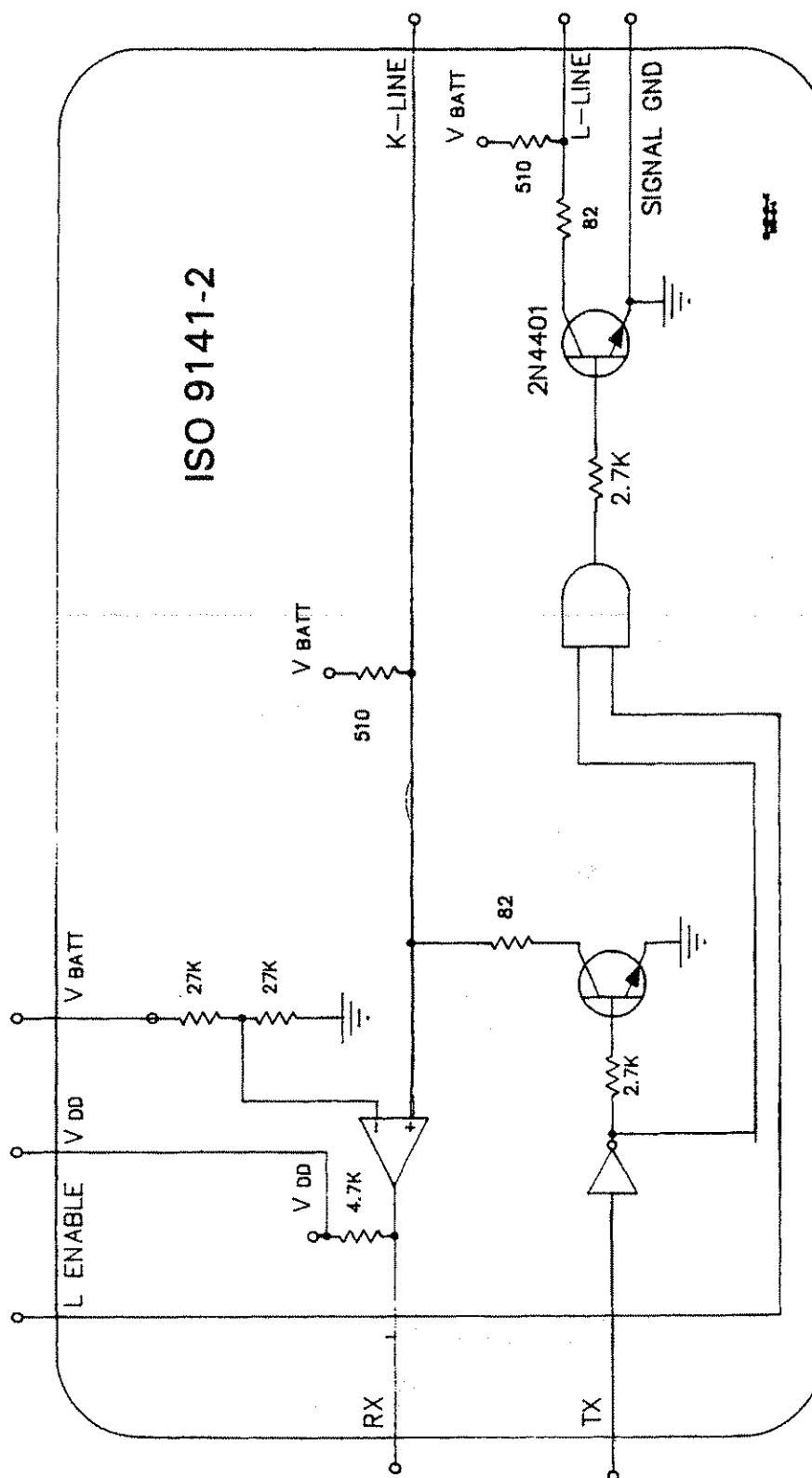


FIGURE A1C—HBCC AND TRANSMIT DRIVER DETAIL



This example uses chip select lines from the host to select which peripheral the host wishes to communicate with. Control data from the host enables and disables the DLCS and HBCC interfaces.

Because these devices are available from semiconductor suppliers who are also supplying them to major automotive manufacturers for use in production vehicles, compatibility with those vehicles should be readily verifiable.

The ISO 9141-2 interface is as described in A.1.4. The host uses its SCI interface to communicate with a vehicle through the ISO 9141-2 interface. A logic line is used by the host to enable the L line when necessary.

A.2.2 DLCS Operation—The DLCS contains a logic section and an analog section in a single integrated circuit. The logic section includes the SPI interface to the host, a transmit buffer, a receive buffer, status and control registers, bit timing, and symbol encoding and decoding logic. The analog section includes the transceiver circuitry. Data transfer between the host and the DLCS is done with two byte SPI transfers. The host sends to the DLCS a command byte and a data byte, while the DLCS sends to the host a status byte and a data byte. The content of the data bytes is dependent on the command.

a. Commands sent to the DLCS include:

1. General commands (e.g., send break, go to sleep, terminate transmit retry, load configuration data)
2. Transmit commands (e.g., load transmit data, transmit message)
3. Receive commands (e.g., unload receive data, flush byte, flush message)

b. Status data send from the DLCS indicate the following:

1. Receive status (e.g., buffer contains bytes or messages)
2. Transmit status (e.g., buffer contains bytes or messages)
3. Data link status (e.g., data link shorted)

Operation of the DLCS consists primarily of three functions: initialization, transmission of a message, and reception of a message. Each of these will be discussed in more detail as follows:

A.2.2.1 INITIALIZATION—Initialization is accomplished by sending the DLCS a command byte to load the accompanying data from the host as configuration data. The DLCS can be configured to enable or disable it to interrupt the host, thereby allowing either polling or interrupt based signalling schemes to be used, and to configure the oscillator divisor. Once the DLCS is initialized, normal transmission and reception can begin.

A.2.2.2 MESSAGE TRANSMISSION—Loading a message from the host to the DLCS for transmission on the bus is done by several 2 byte SPI transfers. Each transfer contains a command byte to load the accompanying data as transmit data. Loading the first and last byte of the message must be done with specific command bytes. Once the command to load the accompanying data as the last transmit data byte is received by the DLCS, the DLCS will begin an attempt to transmit the message on the bus. With each 2 byte SPI transfer with the DLCS, a status byte and data byte will be transferred to the host. The status byte is used to determine the status of the transmit buffer, i.e., empty, contains some bytes, full, etc. The status byte also contains receive status. When loading a transmit message into the DLCS, the data bytes returned by the DLCS to the host are ignored.

The DLCS handles all data link access responsibilities, i.e., idle bus detection, arbitration, automatic retry (if enabled), etc.

A.2.2.3 MESSAGE RECEPTION—The DLCS on its own receives and buffers a complete message from the bus, checks the received CRC, sets a status flag indicating a message has been received and if any errors occurred and, if enabled, interrupts the host. Retrieving a message received by the DLCS is done first by either polling the DLCS to determine if a message has been received, or by servicing an enabled interrupt that occurs upon reception of a message. (The remainder of this discussion assumes the interrupt method is used.)

Upon receiving an interrupt, performing a 2 byte SPI transfer with the DLCS will result in the transfer of status and data to the host. The status byte is used to determine if the receive buffer contains any bytes of a message or a complete message(s), and the status of the transmit buffer. Once all the bytes of a message have been received by the DLCS an indicator will be set in the status byte and, if enabled, an interrupt will be generated for the host. The status byte will also indicate whether the message was received correctly or that an error occurred, i.e., CRC error, incomplete byte, and bit timing error. If the message unloaded from the DLCS was received while the DLCS was attempting to transmit a message, the status byte will also indicate transmission status values such as overrun or underrun and whether bus arbitration was won or lost.

A.2.3 DLCS Pin Names and Descriptions—The names and descriptions of the pins of the DLCS are shown in Table A2.

TABLE A2—DLCS PIN NAMES AND DESCRIPTIONS

Pin Number	Pin Name	Description
1	Vssd	Digital Ground
2	LOTI	Logic Out Transmitter In (Test)
3	OSC2	Oscillator 2
4	OSC1	Oscillator 1
5	RST~	Reset~ (Active Low)
6	CS~	Chip Select ~ (Active Low)
7	SCLK	SPI Serial Clock
8	SIMO	SPI Slave In Master Out
9	SOMI	SPI Slave Out Master In
10	INT~	Interrupt~ (Active Low)
11	Vdd	Digital Voltage Supply (+5 V)
12	N/A	Not Used
13	N/A	Not Used
14	N/A	Not Used
15	N/A	Not Used
16	N/A	Not Used
17	N/A	Not Used
18	N/A	Not Used
19	N/A	Not Used
20	Vssa	Analog Ground
21	LOAD	Bus Load
22	BUS	Bus Output
23	Vbatt	Battery Voltage
24	PSEN	Power Supply Enable
25	Vcc	Analog Voltage Supply (+5 V)
26	REXT2	External Resistor 2
27	REXT1	External Resistor 1
28	LITO	Login In Transmitter Out (Test)