

# SURFACE VEHICLE RECOMMENDED PRACTICE

**SAE** J2411

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## Single Wire CAN Network for Vehicle Applications

**Foreword**—The objective of this SAE Standard is to define a level of standardization in the implementation of low speed vehicle serial data network communications using the Controller Area Network (CAN) protocol. This low speed implementation of CAN is intended to provide a lower cost complement to the SAE J2284 High Speed CAN standard.

The goal of this document is to define a serial data physical layer, data link layer and media design criteria to be installed in various automotive Electronic Control Units (ECU). This document will allow ECU and tool manufacturers to satisfy the needs of multiple end users with minimum modifications to the basic design. This document will benefit vehicle Original Equipment Manufacturers by achieving lower ECU costs due to higher industry volumes of the basic design.

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1. **Scope**—This SAE Recommended Practice defines the Physical Layer and portions of the Data Link Layer of the OSI model for data communications. In particular, this document specifies the physical layer requirements for any Carrier Sense Multiple Access/Collision Resolution (CSMA/CR) data link which operates on a single wire medium to communicate among Electronic Control Units (ECU) on road vehicles.

Requirements stated in this document will provide a minimum standard level of performance to which all compatible ECUs and media shall be designed. This will assure full serial data communication among all connected devices regardless of supplier.

This document is to be referenced by the particular vehicle OEM Component Technical Specification which describes any given ECU in which the single wire data link controller and physical layer interface is located. Primarily, the performance of the physical layer is specified in this document. ECU environmental and other requirements when provided in the Component Technical Specification, shall supercede the requirements of this document.

The intended audience includes, but is not limited to, ECU suppliers, CAN controller suppliers, CAN transceiver suppliers, component release engineers, and vehicle system engineers.

- 1.1 **Mission/Theme**—This specification describes the physical layer requirements for a single wire data link capable of operating with various CSMA/CR protocols such as the Bosch Controller Area Network (CAN) version 2.0. This serial data link network is intended for use in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor and/or dedicated logic devices which use the network.

## 2. References

- 2.1 **Applicable Publications**—The following publications form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest version of SAE publications shall apply.

- 2.1.1 SAE PUBLICATIONS—Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

SAE J551—All parts—Performance Levels and Methods of Measurement of Electromagnetic Compatibility for Vehicles and Devices  
SAE J1113—All parts—Electromagnetic Compatibility Measurement Procedures for Vehicle Components  
SAE J1213-1—Glossary of Vehicle Networks for Multiplexing and Data Communications  
SAE J1930—Electrical/Electronic Systems Diagnostic Terms, Definitions, Abbreviations and Acronyms  
SAE J2284—High Speed CAN (HSC) for Vehicle Applications at 500 KBPS  
SAE 970295—Optimization of CAN Bit Timing Parameters

- 2.1.2 ISO DOCUMENTS—Available from ANSI, 11 West 42nd Street, New York, NY 10036-8002.

ISO 7498—Data processing systems—Open systems interconnection standard reference mode  
ISO 7637—Road vehicles—Electrical interference by conduction and coupling—Parts 1 and 2

- 2.1.3 SUPPLIER PUBLICATIONS

Delphi - Delco Electronics Automotive Systems - DK166153 - Single Wire CAN Transceiver  
Philips - AU5790 - Single Wire CAN Transceiver  
Infineon - TLE 6255 - Single Wire CAN Transceiver

#### 2.1.4 OTHER PUBLICATIONS

Bosch Controller Area Network 2.0 specification  
CISPR 25 - Limits & Methods of Measurement of Radio Disturbance Characteristics for the Protection of Receivers used on board vehicles.

### 3. Definitions

- 3.1 Data Link Layer**—This provides for the reliable transfer of information across the physical layer. It includes the message structure, framing, and error control.
- 3.2 Dominant Signal**—The driven and high voltage state of the single wire bus. If multiple devices access the bus, this state dominates the recessive or non-driven state.
- 3.3 Media**—The physical entity which conveys the electrical (or equivalent means of communication) signal transmission among ECUs on the network. For Single Wire CAN, this media consists of a single random laid wire.
- 3.4 Physical Layer**—This ISO 7498 subsection consists of the media, mechanical interconnections, and transceivers which provide the network with access and interconnection among all ECU nodes.
- 3.5 Protocol**—The formal set of conventions or rules for the exchange of information among the ECUs. This includes the specification of the signal frame administration, frame transfer, and physical layer.
- 3.6 Radiated Emissions**—This is the energy that radiates from the CAN physical layer.
- 3.7 Radiated Immunity**—This is the level of susceptibility of physical layer components to communication errors in the presence of high energy electromagnetic fields.
- 3.8 Recessive Signal**—The undriven and low voltage state of the single wire bus. If multiple devices access the bus, this state is overridden by the dominant state.

### 4. Acronyms, Abbreviations, and Symbols

CAN - Controller Area Network  
CSMA/CR - Carrier Sense Multiple Access/Collision Resolution  
ECU - Electronic Control Unit  
EMC - Electromagnetic Compatibility  
ESD - Electrostatic Discharge  
ISO - International Organization for Standardization  
Kbits/s - Thousands of data bits per second  
SAE - Society of Automotive Engineers  
SWC - Single Wire CAN  
DLC - Diagnostic Link Connector

- 5. Single Wire CAN System Requirements**—The physical layer is responsible for providing a method of transferring digital data symbols (1's and 0's) to the communication medium. The physical layer interface is a single wire, vehicle ground referenced bus with high side voltage drive.

#### 5.1 Physical and Data Link Layer Characteristics

- a. Carrier Sense Multiple Access/Collision Resolution (CSMA/CR) bus access and arbitration with dominant high and recessive low signal voltages.
- b. Capable of operating with CAN 2.0 messages with either 11-bit or 29-bit identifier.

**5.2 Message Format**—All ECU Single Wire CAN interfaces shall conform to the Bosch “CAN Specification 2.0” of September 1991. Either the 11- or the 29-bit frame identifier mode may be used.

The encoding of the 11-bit identifier field shall be vehicle manufacturer specific. The CAN requirement that the “seven most significant bits (ID10-ID4) shall not all be recessive” shall not be enforced in SAE J2411 hardware.

### 5.3 Bus Operation

**5.3.1 NORMAL COMMUNICATION MODE**—Transmission bit rate in the normal communication mode speed is 33.333 Kbits/s. The normal transmission mode shall use transmitters with controlled waveform rise and overshoot times. Waveform trailing edge control is required to assure that high frequency components are minimized at the beginning of the downward voltage slope. The remaining fall time occurs after the bus is inactive with drivers off and is determined by the RC time constant of the total bus load.

**5.3.2 HIGH SPEED COMMUNICATION MODE**—The high speed mode is used for data download when the on-board network is attached to an off-board tester ECU. The assembly line data download transmission bit rate in high speed communication is up to 83.333 Kbits/s depending on the number of connected bus nodes (which affect the network time constant) - see Appendix C and/or specific vehicle specifications. If a variable assembly line download bit rate method is used, the tester shall be able to communicate the intended bit rate to all participating nodes prior to the switch into the high speed mode.

The service tools may be designed so that the service download high speed bit rate shall always operate at the fixed bit rate of 83.333 Kbits/s to limit the service test tool complexity. See Appendix C.

The test tool must connect Rtool to the bus before transmitting any high speed messages. Rtool shall be connected directly to ground on the ECU. Rtool shall never be connected to the Load pin of the transceiver. The Load pin is not designed to handle the high level of current through Rtool.

High speed transmission mode allows shortened total bit time and shortened waveform rise and fall times (rise or fall times shall be less than 25% of the total bit time as measured at the normal receiver threshold voltage levels  $V_{ih}$ ). Radiated EMC requirements in 5.5 are waived while in this mode. Bus transmitter drive circuits for those nodes which are required to communicate in high speed mode shall be able to drive reduced bus resistance when in this mode (to reduce the RC time constant - see Table 1). High speed communications shall utilize the normal mode signal voltage levels as specified in Table 1.

All nodes shall be able to operate at the High Speed mode CAN frame timing and shall enter this mode when they have been commanded by the download system manager. The normal sequence of entering and leaving high speed mode is shown as follows as commanded by the download system manager:

- a. All nodes are awakened at normal bus speed
- b. Nodes are commanded to remain awake or go to sleep mode
- c. Nodes designated as sleepers go to sleep mode
- d. The download tool switches the bus circuit to the lower tool bus resistance
- e. Awake nodes are commanded to go to high speed mode
- f. High speed traffic is completed
- g. Awake nodes are commanded to go to normal speed mode
 

NOTE—In case of system errors, all nodes which enter the High Speed mode shall return to the normal speed mode after a system specified time delay
- h. The download tool switches the tool bus resistance out of the bus circuit
- i. All sleeping nodes are awakened and shall then operate at normal bus speed

Nodes shall initialize in the normal speed mode after a power up, CAN error passive, CAN Busoff, or running reset.

TABLE 1—SINGLE WIRE CAN BUS SIGNALS AND LOADING REQUIREMENTS

| Parameter                                                                                | Symbol           | Min              | Typical | Max               | Units    |
|------------------------------------------------------------------------------------------|------------------|------------------|---------|-------------------|----------|
| ECU Battery Voltage Input <sup>(1)</sup>                                                 | $V_{batt}$       | 6.5              |         | 16                | V        |
| Offset Wakeup Input High Voltage Threshold <sup>(2)(3)</sup>                             | $V_{ihWuOffset}$ | $V_{batt} - 4.3$ |         | $V_{batt} - 3.25$ | V        |
| Offset Wakeup Output High Voltage <sup>(4)</sup>                                         | $V_{ohWuOffset}$ | $V_{batt} - 1.6$ |         | $V_{batt}$        | V        |
| Fixed Wakeup Input High Voltage Threshold <sup>(2)(3)</sup>                              | $V_{ihWuFixed}$  | 6.15             |         | 8.1               | V        |
| Fixed Wakeup Output High Voltage <sup>(5)</sup>                                          | $V_{ohWuFixed}$  | 9.7              |         | 12                | V        |
| High Speed and Normal Mode Output High Voltage <sup>(6)</sup>                            | $V_{oh}$         | 3.5              |         | 4.55              | V        |
| High Speed and Normal Mode Input High Voltage Input Threshold                            | $V_{ih}$         | 1.8              |         | 2.2               | V        |
| Normal Bus recessive or passive state low voltage <sup>(5)</sup>                         | $V_{leaknorm}$   | 0.0              |         | 0.25              | V        |
| LOG condition Bus recessive or passive state low voltage <sup>(5)</sup>                  | $V_{leak LOG}$   | 0.0              |         | 0.5               | V        |
| Ground Offset Voltage                                                                    | $V_{g off}$      | —                |         | 0.8               | V        |
| Battery ECU Offset Voltage                                                               | $V_{b off}$      | —                |         | 1.0               | V        |
| EMC Inductor inductance (if required to meet EMC)                                        | $L_{ul}$         |                  | 47      |                   | $\mu H$  |
| EMC Inductor DC resistance                                                               | $R_L$            |                  |         | 2.25              | $\Omega$ |
| EMC Inductor voltage drop                                                                | $V_{ind}$        |                  |         | 0.3               | V        |
| Network Total Resistance <sup>(7)(8)</sup>                                               | $R_{tl}$         | 270              |         | 4596              | $\Omega$ |
| Device Capacitance (unit load)                                                           | $C_{ul}$         | 198              | 220     | 242               | pF       |
| Network Total Capacitance <sup>(7)(8)(9)</sup>                                           | $C_{tl}$         | 396              |         | 13,700            | pF       |
| Network Time Constant <sup>(10)</sup>                                                    | $t_{network}$    | 1.0              |         | 4.3               | $\mu s$  |
| High Speed Mode Network Resistance to GND                                                | $R_{load}$       | 100              |         |                   | $\Omega$ |
| High Speed Mode Tool Resistance to GND                                                   | $R_{tool}$       | 171              | 180     | 189               | $\Omega$ |
| Device Resistance (unit load)                                                            | $R_{ul}$         | 9009             | 9090    | 9191              | $\Omega$ |
| Device Resistance (min load)                                                             | $R_{min}$        | 2000             |         |                   | $\Omega$ |
| Normal mode signal transition time - TxD to $V_{ih max} + V_{g off}$ <sup>(11)</sup>     | $T_{t norm}$     | 3.0              |         | 6.3               | $\mu s$  |
| High speed mode signal transition time - TxD to $V_{ih max} + V_{g off}$ <sup>(12)</sup> | $T_{t hs}$       | 0.2              |         | 1.5               | $\mu s$  |
| High voltage mode signal transition time - TxD to $V_{ih min} - V_{g off}$               | $T_{t hv}$       |                  |         | 12.4              | $\mu s$  |
| Device Leakage Current to bus with no loss of ground                                     | $I_{leak}$       | —                |         | 10                | $\mu A$  |
| Device Leakage Current to bus with loss of ground                                        | $I_{leak LOG}$   | —                |         | 50                | $\mu A$  |
| Device Series Inductor Resistance ( if required )                                        | $R_{ind}$        | —                |         | 2.3               | $\Omega$ |
| Network distance between any two ECU nodes                                               | bus length       | —                |         | 60                | m        |
| Number of system nodes including off vehicle test tool                                   |                  | 2                |         | 32                |          |

1.  $V_{batt}$  is measured at the ECU input power pins. All voltages are referenced to the local ECU ground.
2. The minimum transceiver input wakeup voltage level shall be the smaller of  $V_{ihWuFixed}$  minimum or  $V_{ihWuOffset}$  minimum.
3. The maximum transceiver input wakeup voltage level shall be the smaller of  $V_{ohWuFixed}$  minimum or  $V_{ohWuOffset}$  minimum.
4. The minimum transceiver output wakeup voltage level shall be the smaller of  $V_{ohWuFixed}$  minimum or  $V_{ohWuOffset}$  minimum.
5. The bus recessive state low voltage is the offset due to the ECU high side driver leakage current ( $I_{leak}$ ) and does not include the ground offset voltage ( $V_{g off}$ ). This leakage current limitation shall be in effect over the  $6.5 < V_{batt} < 26.5$  V range (see 5.8 and 5.3.5.4.)
6. The  $V_{ohwu}$  value is measured at the ECU bus pin. It includes an allowance for the voltage drop across the inductor DC resistance (see 5.4.2.3).
7. The minimum Network Time Constant and Signal Transition Time are determined by the EMC requirements. If these values are set too low, the ECU will not pass the required EMC tests. See 6.1.9, items, a and b for wave-shaping requirements.
8. The signal transition time must be maintained regardless of bus RC distribution.
9. The Network total capacitance includes the capacitors placed on the ECUs as well as the capacitance of the bus wires.
10. The network time constant incorporates the bus wiring capacitance. The minimum value is selected to limit radiated emissions. The maximum value is selected to ensure proper communication under all communication modes and is the absolute maximum allowed under normal operating conditions. The system should be designed to have a time constant no larger than  $5.3 \mu s$  under an error condition. This should be considered when determining the fusing for the vehicle. Not all combinations of R and C are possible. Only those combinations of R and C, and the bus length, and PCB trace capacitance, etc., are possible that meet the specified network time constant.
11. Signal delay time is measured from  $V_{il}$  on the TxD input pin to the  $V_{ihMax}$  level on the Bus Input/Output pin. It includes both the internal transceiver propagation delay and the waveform rise time.
12. Signal delay time is measured from  $V_{il}$  on the TxD input pin to the  $V_{ihMax}$  level on the Bus Input/Output pin with  $R_{tool}$  present. It includes both the internal transceiver propagation delay and the waveform rise time.

- 5.3.3 ECU SELECTIVE AWAKE—This bus includes a selective node wakeup capability which allows normal communication to take place among some nodes while leaving the other nodes in an undisturbed sleep state. This is accomplished by controlling the signal voltages such that all nodes must wake up when they receive a higher voltage message signal waveform. The communication system communicates to the nodes information as to which nodes are to stay operational (awake) and which nodes are to put themselves into a non communicating low power “sleep” state. Communication at the lower, normal voltage levels shall not disturb the sleeping nodes. The recommended method of power moding of serial communications nodes shall be by use of the network sleep mode.

The High Speed and High Voltage wakeup features shall not be active at the same time. This requires that the bus be awakened only when in the normal speed mode.

- 5.3.4 CAN CONTROLLER CLOCK TOLERANCE—All nodes which operate on the Single Wire CAN bus shall utilize a CAN controller with a bit timing clock tolerance of  $\pm 0.35\%$  to ensure that the CAN bit timing synchronization shall not be affected by the waveform rise and fall times. See Appendix A for bit timing analysis.
- 5.3.5 BUS ELECTRICAL PARAMETERS—This section describes two possible modes of the bus electrical voltage level parameters required by devices which drive and receive signals on the single wire bus. They are the normal and the wakeup communications signal levels. See Table 1. The high level signals ( $V_{oh}$ ,  $V_{ih}$ ,  $V_{oh\ wu}$ , and  $V_{ih\ wu}$ ) of Table 1 are considered to be the dominant or driven-to-high-voltage bus states.

- 5.3.5.1 *Normal Mode Transmit and Receive Voltage Thresholds for Data Communication*—Serial communication shall operate with normal signal voltage levels indicated in Table 1 without generating a wakeup interrupt to the ECU's controller.

- 5.3.5.2 *High Speed Mode Transmit and Receive Signal Voltages*—The high speed input threshold and output signal voltages are the same as the normal mode signals. See Table 1.

The High Speed and High Voltage Wakeup bus signals shall not be active at the same time.

High speed operation dominant bus symbols shall not exceed the transceiver duty cycles, operating voltage, and temperature requirements as specified in Section 5. (See 5.1.11.)

- 5.3.5.3 *Wakeup Signal Voltage Levels*—A special higher voltage communication waveform using higher signal voltages shall be used to transmit wakeup message frames (see Figure 1). ECUs which detect that the signal voltage level has exceeded the wake up threshold for the wakeup filter time (see  $T_{wuDelay}$  in Table 4) shall enable the Rx/D signal to its ECU. The CAN wakeup frame shall provide at least three consecutive standard speed dominant bit times either in the Identifier or in the data fields. The wakeup frame shall not be sent when in the high speed mode (see 5.3.2). While  $V_{batt}$  is greater than 11.65 V, messages which are transmitted at the normal voltage levels shall not wake up any receiving ECUs.

Messages which are transmitted at the higher wakeup voltage levels shall meet normal bit timing rules so as to reach  $V_{oh}$  at the same time as when transmitting a normal mode recessive-to-dominant voltage signal. The dominant-to-recessive transition  $T_{thv}$  may be extended to the value shown in Table 1 due to the undriven trailing edge and the network time constant. The normal input threshold voltages  $V_{ih}$  and  $V_{il}$  shall remain the same in normal and in wakeup modes so as to be interpreted as normal data and when the  $V_{oh\ wu}$  level is reached, as wakeup commands. See Table 1.

Serial communication when not in wakeup mode shall operate with normal signal voltage levels indicated in Table 1 without generating a wakeup signal or interrupt to the ECU's controller. See Table 1.

ECUs which receive a wakeup signal shall become ready to receive data link frames within a time to be specified by the vehicle system engineer.

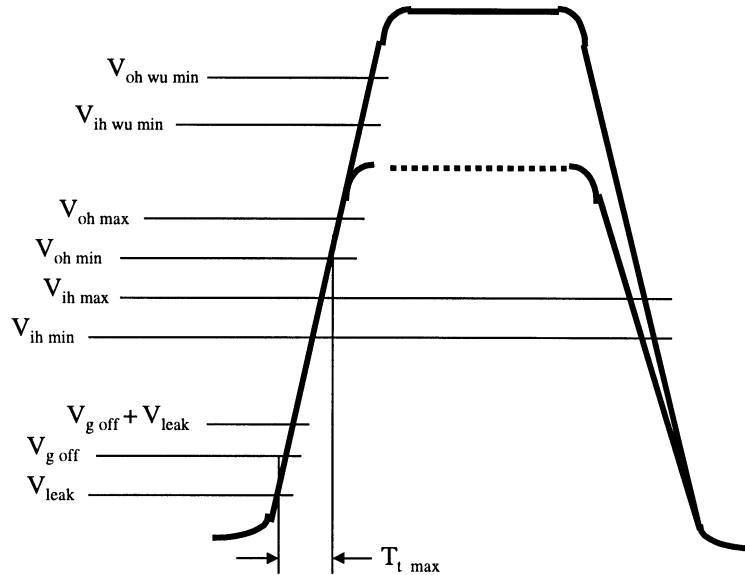


FIGURE 1—SINGLE WIRE DOMINANT BIT WAVEFORM

Single wire data link voltage levels and trip points:

- a.  $V_{oh\_wu\_min}$ —Wakeup Output High Voltage—The minimum guaranteed output voltage high level when commanding all nodes to wake up from sleep mode.
- b.  $V_{ih\_wu\_min}$ —Wakeup Input High Voltage—The minimum guaranteed input voltage high level which will cause the receiving node to wake up from sleep mode.
- c.  $V_{oh\_max}$ —Normal Mode Maximum Output High Voltage—The guaranteed maximum output voltage. This will assure that sleeping nodes will not be awakened by normal data voltage levels.
- d.  $V_{oh\_min}$ —Normal Mode Minimum Output High Voltage—The guaranteed minimum output voltage to assure that receiving nodes will decode a dominant data link symbol.
- e.  $V_{ih\_min}$ —Normal Mode Input High Voltage—The minimum input voltage that will be interpreted as a dominant data link symbol.
- f.  $V_{leak\_max}$ —Bus Passive State Low Voltage—The maximum bus voltage due to transceiver bus out pin leakage when in the off state.
- g.  $V_{g\_off\_max}$ —The maximum bus offset voltage due to ground wire variations among ECUs.
- h.  $T_{t\_max}$ —Signal Transition Time—The rise or fall time of the data link waveform.

5.3.5.4 **Bus Passive State Voltage Offset ( $V_{leak}$ )**—The bus input/output circuit shall operate under the following limitations:

NOTE—This circuit shall only source current to the bus.

- a. When a node is awake and the bus is in the recessive state, the absolute maximum value of  $V_{leak}$  which may be provided by the node output current shall be as shown in Table 1 over the bus load resistance range  $100 < R_L < 9.19\text{ k}\Omega$
- b. In the sleep mode without a loss of ground, the node leakage current shall be as shown in Table 1.
- c. In any node or bus state, the contribution to bus leakage current by any node which has a loss of ground condition, shall be as specified in Table 1.

## 5.4 Network Topology

5.4.1 LOSS OF ECU GROUND—The loss of ground by any single ECU, with or without an accompanying loss of  $V_{batt}$ , shall not cause any bus voltage offset that will disable normal communications (See Table 1).

5.4.1.1 *Preferred Loss of Ground Protection Method*—This shall be accomplished by including a loss of ground protection circuit in each ECU which will disconnect the path from the bus to  $V_{batt}$  when a loss of ground occurs.

This is the preferred method of loss of ground protection. The Single Wire CAN transceivers as specified in this document shall provide the ground path interrupt circuit.

This method consists of a provision of a circuit within the ECU which will open the ECU ground path to the bus in the event of a loss of ground condition in the ECU. See Figures 2 and 3. The circuit shall not allow the ECU to exceed the maximum ECU bus leakage current ( $V_{leak}$ ) when in the loss of ground failure condition. Since this circuit will contribute a bus offset in the normal or non-failed mode, it shall be capable of sinking the maximum load current allowed by the bus load resistor selected for that ECU without causing the bus voltage to increase to more than the maximum allowed bus offset voltage when there is no loss of ground.

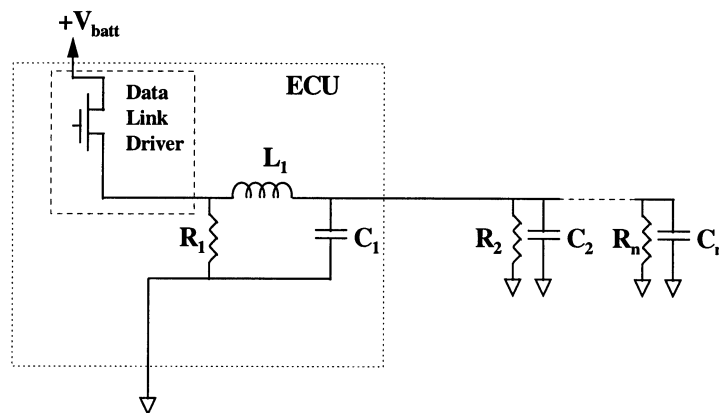


FIGURE 2—SINGLE WIRE DATA LINK PHYSICAL LAYER

- ECU disconnects from bus if LOG condition
- Internal LOG switch allows add/delete ECUs
- Leakage increased when LOG condition

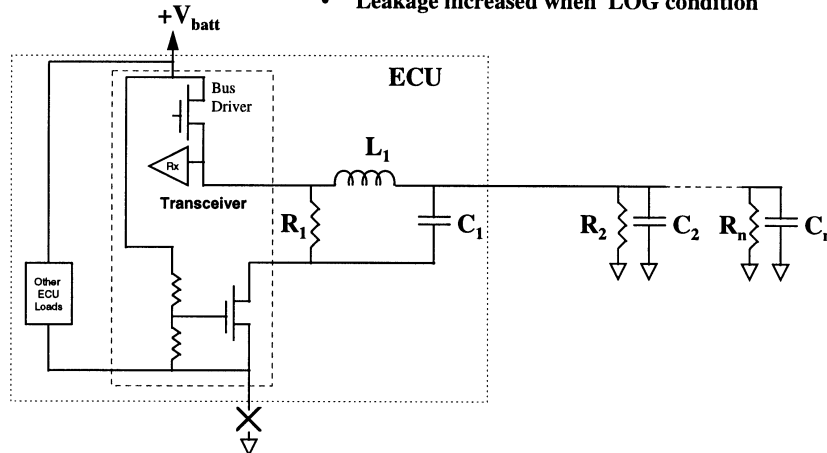


FIGURE 3—INTERRUPT METHOD FOR LOSS OF GROUND PROTECTION

The transceiver's loss of ground protection circuit connection to ground shall not be interrupted when the ECU ground is intact and the ECU is in the sleep mode. To accomplish this, all nodes shall maintain  $V_{batt}$  on the transceiver at all times when any serial communication can take place. This is to ensure that the unit resistive loads shall not be removed from the network timing circuit.

**5.4.1.2 Alternative Loss of Ground Protection Methods**—The loss of an ECU ground causes the ECU to source  $V_{batt}$  through the various ECU circuits to the communications bus instead of to the vehicle system ground as shown in Figures 4 and 5. The equivalent circuit is shown in Figure 5. This shows the effect of bus resistance in circuits which have experienced a loss of ground. The objective in these circuits is to make the  $R_{leak}$  node value high compared to the parallel equivalent resistance of the remaining nodes. This tends to keep the bus voltage offset sufficiently low to keep from continually sensing a dominant high voltage. The bus offset voltage due to the node leakage (loss of ground path + high side transmitter driver off state leakage) must be low enough to allow for a reasonable ground offset voltage and signal noise margin to keep the bus below the  $V_{ih}$  state when the bus is in the recessive state.

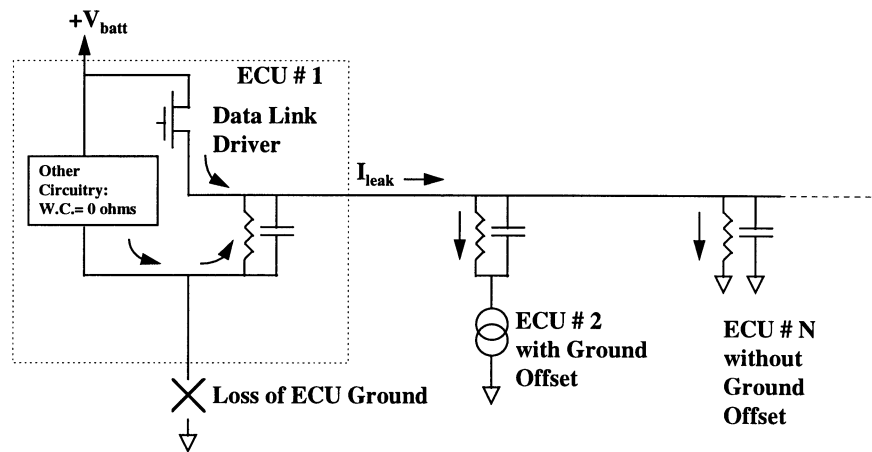


FIGURE 4—BUS VOLTAGE OFFSET SOURCES

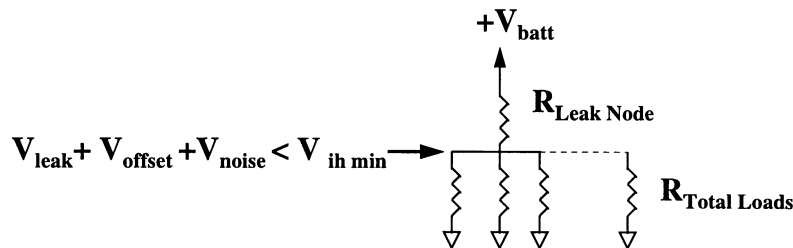


FIGURE 5—LOSS OF GROUND EQUIVALENT CIRCUIT

These methods do not require the ground interrupt circuit but they do require that each vehicle configuration be uniquely designed to assure that the loss of an ECU ground shall not inhibit communication among the remaining ECUs.