



SURFACE VEHICLE RECOMMENDED PRACTICE

J2628™

JUN2018

Issued 2002-08
Revised 2013-07
Stabilized 2018-06

Superseding J2628 JUL2013

Characterization, Conducted Immunity

RATIONALE

Test method has been well understood and used throughout industry as alternative form of transient immunity to understand design margins of a component. No new technology or transient types will be forthcoming in the near future.

STABILIZED NOTICE

This document has been declared "Stabilized" by the SAE Electromagnetic Compatibility (EMC) Standards Committee and will no longer be subjected to periodic reviews for currency. Users are responsible for verifying references and continued suitability of technical requirements. Newer technology may exist.

SAE Technical Standards Board Rules provide that: "This report is published by SAE to advance the state of technical and engineering sciences. The use of this report is entirely voluntary, and its applicability and suitability for any particular use, including any patent infringement arising therefrom, is the sole responsibility of the user."

SAE reviews each technical report at least every five years at which time it may be revised, reaffirmed, stabilized, or cancelled. SAE invites your written comments and suggestions.

Copyright © 2018 SAE International

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, without the prior written permission of SAE.

TO PLACE A DOCUMENT ORDER: Tel: 877-606-7323 (inside USA and Canada)
Tel: +1 724-776-4970 (outside USA)
Fax: 724-776-0790
Email: CustomerService@sae.org
<http://www.sae.org>

SAE WEB ADDRESS:

Full document details: SAE J2628_201806

SAE values your input. To provide feedback on this Technical Report, please visit http://standards.sae.org/J2628_201806

FOREWORD

This document establishes methods for characterizing the robustness of vehicle electronic modules to certain electrical and temperature environmental stresses using methods designed to address the deficiencies inherent in other commonly used validation methods. It is an extension of the philosophy detailed in a new SAE document J1211 (see ref 2.2.1) which was developed by the SAE International Automotive Electronic Systems Reliability Standards Committee and ZVEI (German Electrical and Electronic Manufacturers' Association). It can be summarized from this quote from the handbook.

"Robustness Validation relies first on knowledge-based modeling simulation and analysis methods to develop a highly capable design prior to building and testing physical parts; and then on test-to-failure (or acceptable degradation) and failure/defect susceptibility testing to confirm or identify Robustness Margins, to enable failure prediction and verify that manufacturing processes produce defect free parts. These techniques represent advancement beyond "test-to-pass" qualification plans which usually provide very little useful engineering information about failure modes, failure mechanisms and failure points".

1. SCOPE

The methods included in this document are:

- a. Voltage-Temperature Design Margins.
- b. Voltage Interruptions and Transients.
- c. Voltage Dropouts and Dips.
- d. Current Draw Under a Number of Conditions.
- e. Switch Input Noise

These methods are best applied during the Development stage but can be used at all stages (e.g., Pre-Qualification, Qualification or Conformity).

1.1 Measurement Philosophy

The main issues associated with contemporary mature electronic systems (non mechanical) are:

- a. Requirements not properly defined (e.g., functionality, environment).
- b. System interfaces.
- c. Trouble Not Indicated (TNI).

A typical validation test program may not sufficiently address these issues. Some common deficiencies are:

- a. Requirements validation - tested under ideal conditions (e.g., room temp, bench power supply).
- b. Environmental (non EMC) testing mainly wear-out oriented.
- c. EMC testing not realistic - room temp only, idealized noise signals.
- d. System interactions, interfaces and degradation not sufficiently addressed.

This document addresses much of the above using relatively simple and low cost techniques which:

- a. Requires minimal lab facilities.
- b. Allows maximum flexibility to experiment early in the program.
- c. Allows sufficient reaction time to react to potential issues.
- d. Stage where failures are good (maximizes information).

One main issue addressed here is Conducted Immunity (CI). That aspect of Electromagnetic Compatibility (EMC) has the highest potential for warranty and customer satisfaction issues. However, traditional validation testing for CI has major limitations. Specifically, CI testing is most often run at room temperature due to the nature of the test equipment and facilities - the response of the product could be different when cold or hot than at room temperature. Another limitation is that very repeatable, accurate and idealized signals are used to represent the "real world". While this would appear to be desirable, it is not necessarily the case. The "real world" contains randomness and other characteristics (e.g., complex impedances) not replicated by such idealized test signals. Randomness is extremely critical for a microprocessor type DUT since the stress event (e.g., transients) must often line up in time with a certain point(s) in software execution to have an effect.

It is important to note that many of these tests are not the "test for success" type where the results are classified as either pass or fail. Such testing is of limited value since it generates little information. The goal is to generate variable data or anomalies so that the maximum amount of information is obtained and an informed engineering judgement can be made.

2. REFERENCES

2.1 Applicable Document

The following publication forms a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of publications shall apply.

2.1.1 SAE Publication

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or 724-776-4970 (outside USA), www.sae.org.

SAE J1113-1 Electromagnetic Compatibility Measurement Procedures and Limits for Components of Vehicles, Boats (up to 15 m), and Machines (Except Aircraft) (16.6 Hz to 18 GHz)

2.2 Related Publications

The following publications are provided for information purposes only and are not a required part of this SAE Technical Report.

2.2.1 SAE Publication

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or 724-776-4970 (outside USA), www.sae.org.

SAE J1113-11 Immunity to Conducted Transients on Power Leads

SAE J1211 Handbook for Robustness Validation of Automotive Electrical/Electronic Modules

2.2.2 ISO Publication

Available from American National Standards Institute, 25 West 43rd Street, New York, NY 10036-8002, Tel: 212-642-4900, www.ansi.org.

ISO 7637-2 Road vehicles—Electrical disturbances from conduction and coupling—Electrical transient conduction along supply lines only

2.2.3 IEEE Publication

Comparison of ISO 7637 Transient Waveforms to Real World Automotive Transient Phenomena, 2005 IEEE EMC Symposium

2.2.4 Ford Publication

EMC Specification EMC-CS-2009.1 available at www.fordemc.com

3. DEFINITIONS

3.1 LOL, -X (Y), UOL-X (Y) - See Figure 1

Lower and Upper Operating Limit (when DUT ceases to operate or is erratic) for parameter X at specified conditions Y. For example LOL-V (T-hi) = Lower Operating Limit for voltage at T-hi temperature.

3.2 Tx, Ty - See Figure 1

T1, T2 = Lower /Upper temperature for guaranteed operation (minimum function). T3, T4 = Lower and Upper temperature for guaranteed performance (meets all specs).

3.3 Trouble Not Indicated (TNI)

Potentially defective modules (e.g., field return) where the cause of concern cannot be identified with traditional test methods.

3.4 Vx, Vy - See Figure 1

V1, V2 = Lower and Upper voltage for guaranteed performance (meets all spec). V3, V4 = Lower/Upper voltage for guaranteed operation (minimum function).

4. REQUIREMENTS DESCRIPTION

4.1 Voltage-Temperature Design Margins

This method evaluates Design Margins for voltage over temperature. It can be combined with noise immunity (see 4.2). This testing is especially useful for evaluating electronic design changes or degradation by comparing results before and after other stresses (e.g., thermal cycling). By testing beyond spec limits, it can force failures that would only show up over time in the field (e.g., electrolytic capacitor degradation over time). The data can be used to give a graphical representation comparing the DUT specification limits (voltage, temp) with the Design Margin envelope (figure 1).

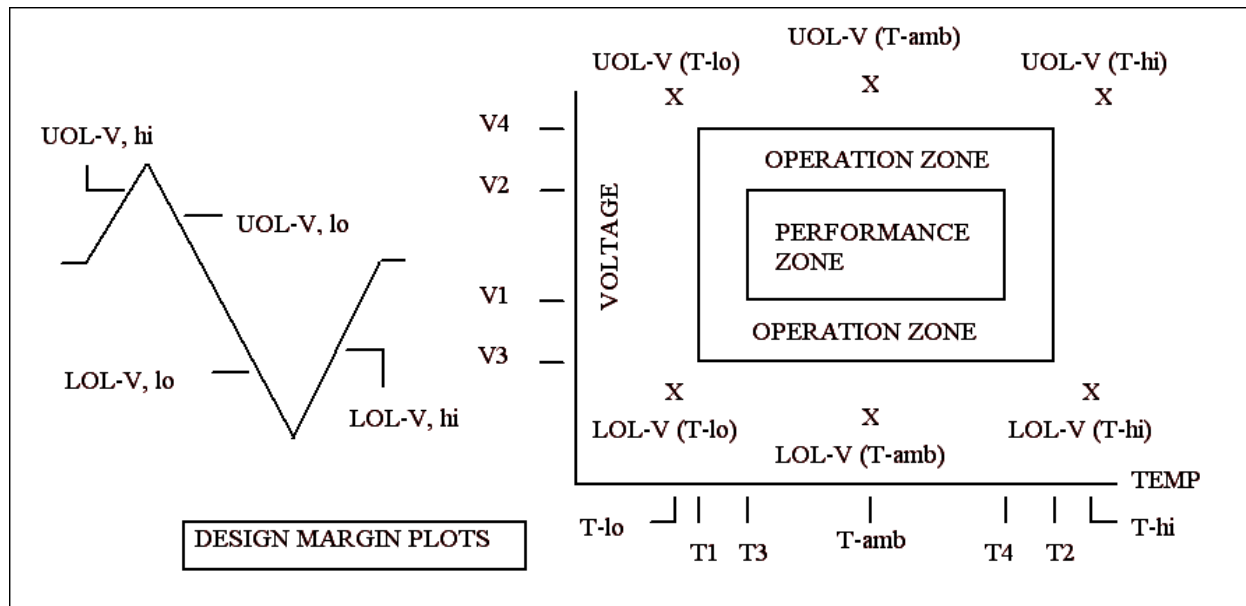


FIGURE 1 - DESIGN MARGINS PLOT - EXAMPLE

4.2 Voltage Interruptions-Transients

4.2.1 General

Although this section is presented separately, this testing can be combined with 4.1.

a. A key enabler is the “chattering relay” (Normally Closed relay contacts connected in series with the relay coil). It has the following properties:

- Creates randomness.
- Creates the actual complex mechanisms of the real event (e.g., contact arcing).
- Simple, low in cost.
- Makes it practical to be used in multi temperature testing.

b. R1-R2 simulate vehicle wiring inductance-resistance in the power and ground circuit and is important for developing voltage drops during transient conditions.

c. L1 simulates vehicle wiring inductance. R1 is to a degree redundant with L1.

d. L2 simulates vehicle inductive loads.

4.2.2 Power Cycle, Power Interruptions During Start-Up, Pulse F

The purpose of this test is to verify proper DUT start-up during ignition key-on (ignition switch or relay bounce) which can be severe over the full vehicle temperature range. This is especially important for verifying proper software initialization. It also addresses interruptions after start-up (e.g., poor connectors) in figure 2. Relay 1 provides the power on-off cycle and relay 3 is connected in a chattering configuration to provide the random noise representing contact bounce at power up and after. Figure 4 shows a typical example of the output from this circuit. This test applies to switched power and control circuits.

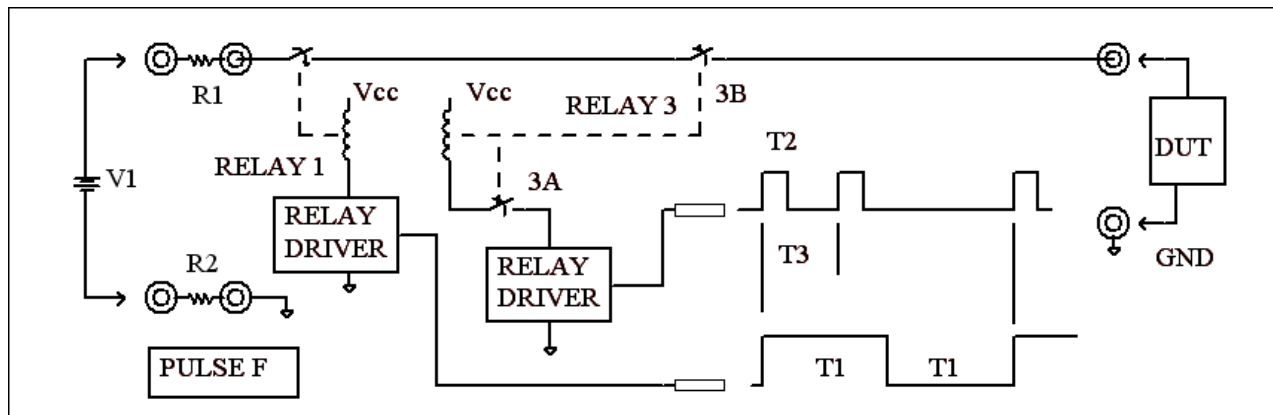


FIGURE 2 - TEST PULSE F SCHEMATIC

4.2.3 Inductive Transients - Pulse A1, A2, A1-a , A2-a, C

Historically ISO 7637-2 (reference 2.2.2) has been the standard for these types of vehicle transients but as reference 2.2.3 illustrates, this is not the case. The pulses in this document were developed to be a more realistic representation of actual vehicle transients. Figure 3 shows how they are generated.

Pulse A1 and A2 simulates the transients produced by switching off power to the DUT and an inductive load (L2) that is in parallel with the DUT. The pulse is produced at the start of period T1 when contact 3B opens. R3 provides adjustment of current through L2 to give different waveform characteristics (A1 = high current, A2 = low current). Figures 5 and 6 shows a typical example of the output from this circuit. This test applies to switched power and control circuits.