



SURFACE VEHICLE INFORMATION REPORT

J2716™

APR2016

Issued 2007-04
Revised 2016-04

Superseding J2716 JAN2010

(R) SENT - Single Edge Nibble Transmission for Automotive Applications

RATIONALE

1. Clarified clock variation refers to variation in clock tick time.
2. New appendix for High Speed 12 bit Sensors.
3. Changes for initialization and non-usage of serial message.
4. Changes to support option for independent 5V supply in sensor
5. Serial message cycle changed to ≤ 64 messages for greater flexibility and to allow more time for diagnostic information.
6. Clarification to EMC Susceptibility testing guidelines for Erroneous SENT frames which remain undetected by the SENT CRC
7. Added Appendix A.6 Temperature Sensor requirements
8. Added APPENDIX E
9. Added APPENDIX G for recommended connector
10. Created APPENDIX H (SENT Data Frame Formats) and moved generic sensor requirements from APPENDIX A to APPENDIX H
11. Changes to support higher current sensors
12. Added E.3 Error Messages and Signals
13. Added A.7 Position Sensors and Combined Position Temperature Sensors
14. Added *Overview of SENT standard structure (3.2)*

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1. SCOPE

This document defines a level of standardization in the implementation of the digital pulse scheme for reporting sensor information via Single Edge Nibble Transmission (SENT) encoding. This standard will allow ECU and tool manufacturers to satisfy the needs of multiple end users with minimum modifications to the basic design. This standard will benefit vehicle Original Equipment Manufacturers (OEMs) by achieving lower ECU costs due to higher industry volumes of the basic design.

Requirements stated in this document provide a minimum standard level of performance to which all compatible ECUs and media shall be designed. This assures data communication among all connected devices regardless of supplier.

This document is a communication interface specification and no to be treated as product specification.

The intended audience includes, but is not limited to, ECU suppliers, sensor suppliers, component release engineers and vehicle system engineers.

1.1 Overview

The Single Edge Nibble Transmission encoding scheme (SENT) is intended for use in applications where high resolution sensor data needs to be communicated from a sensor to an Electronic Control Unit (ECU). It is intended as a replacement for the lower resolution methods of 10 bit A/D's and PWM and as a simpler low cost alternative to CAN or LIN. The implementation assumes that the sensor is a smart sensor containing a microprocessor or dedicated logic device (ASIC) to create the signal.

SENT is a unidirectional communications scheme from sensor / transmitting device to controller /receiving device which does not include a coordination signal from the controller/receiving device. The sensor signal is transmitted as a series of pulses with data encoded as falling to falling edge periods. Details of the signal encoding may vary for specific sensor applications described in various appendices of this specification.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of SAE publications shall apply.

2.1.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or +1 724-776-4970 (outside USA), www.sae.org.

SAE J551 (All parts) Performance Levels and Methods of Measurement of Electromagnetic Compatibility for Vehicles and Devices

SAE J1113 (All parts) Electromagnetic Compatibility Measurement Procedures for Vehicle Components

SAE J1930 Electrical/Electronic Systems Diagnostic Terms, Definitions, Abbreviation and Acronyms

2.1.2 Other Publications

CISPR 25 Limits and Methods of Measurement of Radio Disturbance Characteristics for the Protection of Receivers Used On Board Vehicles (available at webstore.iec.ch).

ES-XW7T-1A278-AC Ford Component and Subsystem Electromagnetic Compatibility Worldwide Requirements and Test Procedures (available at www.fordemc.com. This document shall be referred to as the Ford EMC Spec.)

GMW3097 General Specification for Electrical / Electronic Components and Subsystems, Electromagnetic Compatibility (this document will be referred to as the GM EMC Spec.)

ANSI INCITS 4-1986 (R2007) American National Standards Institute, *Information Systems - Coded Character Sets - 7-Bit American National Standard Code for Information Interchange (7-Bit ASCII)*, 2007

USCAR United States Council for Automotive Research, USCAR EWCAP EWCAP Footprints Database, 1.2 mm Connectors (sealed), (available at <http://www.uscar.org/guest/teams/10/Electrical-Wiring-Component-Applications-Partnership>)

3. DEFINITION OF TERMS

3.1 GLOSSARY

3.1.1 Media

The physical entity that conveys the electrical (or equivalent means of communication) signal transmission between electronic devices.

3.1.2 Protocol

The formal set of conventions or rules for the exchange of information between electronic devices. This includes the specification of the signal frame administration, frame transfer and physical layer.

3.1.3 Message

One sequence of calibration pulse and specified number of nibble pulses for that implementation. The number of nibbles is constant for each implementation but the individual message times can vary depending on the specific values of the nibbles.

3.1.4 Radiated Emissions

The energy that radiates from the physical layer.

3.1.5 Radiated Immunity

The level of susceptibility of physical layer components to communication errors in the presence of high energy electromagnetic fields.

3.1.6 Receiver Module

The processor that receives the encoded signal. Generally an ECU with falling-edge detection and timing measurement capabilities.

3.1.7 Transmitter Module

The device that generates the message to the receiver module. Generally a smart sensor.

3.1.8 Nominal

Time period assuming no transmitter clock error.

3.1.9 Pulse Period

Time between consecutive falling edges of the transmitting signal.

3.1.10 Error

Indicates that a problem exists with current sample, data or message.

3.1.11 Fault

Indicates that enough errors have been detected (usually matured by counting X errors in-a-row or via up-down or X-out-of-Y counters or other filtering means) to develop into a fault which is latched until cleared.

3.1.12 Clock Tick Time

Fundamental time unit in transmitter used to construct SENT output signal.

3.1.13 Signal Ground Line

The reference point from which all SENT electrical interface voltage parameters are measured; transmitter requirements are defined with respect to the Signal Ground pin on the transmitting device; receiver requirements are defined with respect to the Return pin on the receiving module. An equivalent term for the Signal Ground Line is Signal Return Line. The suffix GND is linked to the Signal Ground Line.

3.1.14 Power Ground Line

The signal through which the primary power current for a module flows to a system level ground node. Under certain conditions it is possible, that Power Ground Line and Signal Ground Line are identical.

3.1.15 Medium Temperature

Measured temperature of a physical medium defined in the specification of the particular sensor or the transmitter.

3.1.16 Internal Reference Temperature

Measured internal temperature of some point within the transmitter (e.g., integrated circuit). This temperature can be used by the receiver as a reference to determine the status of the transmitter.

3.1.17 Reserved data ranges

Reserved data ranges shall be used, as specified in SAE J2716, or they are retained for future use by the SAE. These data ranges may not be assigned to any other use.

3.1.18 Fast Channel

The data transmitted on the data nibble pulses can carry the payload data of one or more Fast Channels. The data rate of these payload data channels is determined by the number of bits (e.g., 12 bits) in each signal data field and the period of the SENT transmission sequence. These channels are called Fast Channels, since their data rate is significantly larger than the data rate of the Serial Message Channel.

3.1.19 Slow Channel

The Serial Message Channel is also denoted as Slow Channel in earlier revisions of SAE J2716. The term Slow Channel is used as opposed to Fast Channel.

3.1.20 Serial Message Channel

Two bits per SENT data frame can be allocated to a serial message channel. Either Enhanced Serial Message Format or Short Serial Message Format can be used for data transmission over the serial message channel. The Enhanced Serial Message Format is recommended rather than the Short Serial Message Format.

3.1.21 Enhanced Serial Message Format

Recommended format of the Serial Message Channel frame.

3.1.22 Short Serial Message Format

Format of the Serial Message Channel frame.

3.1.23 Supplementary Data Channels

Enhanced Serial Message Format frames can carry supplementary data channels. These supplementary data channels can transmit measurement data from further sources at a lower rate than the data on the fast channels. A default assignment of supplementary data channels is defined for specific sensor classes.

3.2 OVERVIEW OF SENT STANDARD STRUCTURE

The main body of the standard defines the mandatory means of the physical as well as data link layer with limited degrees of freedom for implementation. The system designer has to specify the SENT compliant component by choosing the options and limit the variance given within physical and data link layer definitions of the main body.

The application specific definitions within the appendices are intended to help the system and component designer to limit the variance of implementations to support interchangeability of components, but following them is not mandatory.

The system designer should start by using the application specific protocols of APPENDIX A and additionally limit from the available ranges and choose from the set of available options for the transmitting component. Regardless the application specific protocols defined with APPENDIX A there are still some options which are open to be chosen for different implementations by the component designers. These options need to be defined with the component specifications and either be covered by the receiver design or have to be limited by the system designer.

A flexible receiver design adapting to different options is recommended and supports the interchangeability.

3.2.1 SENT Transmission Layers

Figure 3.2.1-1 illustrates the structure of the SENT standard and the relationship of as well the sections of the main body as the appendices of the document to the data transmission layers.

Since the functions which define one layer of the SENT protocol are required by the functions of the layer above it, this overview also explains the hierarchy of the sections of the SENT standard.

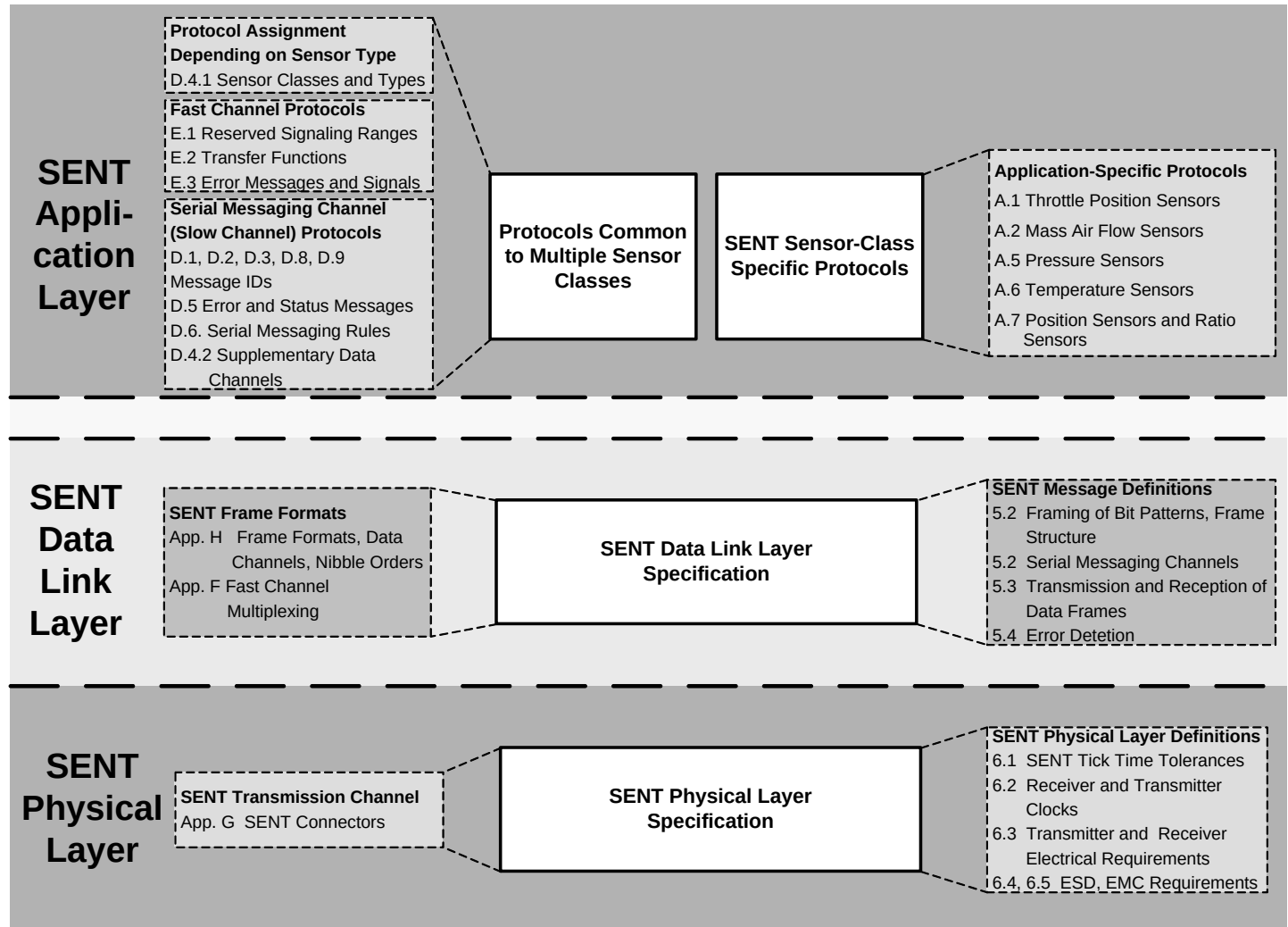


Figure 3.2.1-1 – SENT standard structure and transmission layers

3.2.2 SENT Appendices

Protocols and frame formats are common to multiple sensor types.

Application-specific sensor types, data transmission formats and protocols can be specified by references to respective sections that define generic functions and frame formats. SENT test conditions are specified in APPENDIX C.

4. ACRONYMS, ABBREVIATIONS, AND SYMBOLS

ASIC – Application Specific Integrated Circuit
CAN – Controller Area Network
ECU – Electronic Control Unit
EMC – Electromagnetic Compatibility
ESD – Electrostatic Discharge
FC – Frame Control (fast channel multiplexing)
ISO – International Organization for Standardization
kbits/sec – Thousands of data bits per second
LIN – Local Interconnect Network
LSN – least significant nibble
MAF – Mass Air Flow
MidLSN – middle least significant nibble
MidMSN – middle most significant nibble
MidN – middle nibble
MSN – most significant nibble
OEM – Original Equipment Manufacturer
RE – Radiated Emissions
RI – Radiated Immunity
SAE – Society of Automotive Engineers
SENT – Single Edge Nibble Transmission
TPS – Throttle Position Sensor

5. SENT SYSTEM REQUIREMENTS

5.1 General Requirements

Transmission occurs independently of any action of the receiver module, i.e., the transmission shall not require a synchronization signal from the receiver module.

Assumptions used to design the encoding scheme:

- Actual Transmission time may be dependent on the data values being sent and the transmitter clock variation.
- Message pulse order (i.e., message frame) is fixed for all transmitters.
- Transmitter is allowed a maximum clock tick time variation of $\pm 20\%$.
- Transmission time for the longest data message and max transmitter clock variation is less than 1.0 millisecond at 3 microsecond clock tick time and 6 data nibbles.
- A transmitter specific nominal clock period (tick) between 3 microseconds and 90 microseconds.
- The encoding scheme defines a number of diagnostic tests to be implemented in the receiving module. However, for example, the CRC checksum is 4 bit and not as robust as other checking schemes (see section 5.4.1). Therefore, the encoding scheme is targeted at systems that can tolerate a low probability of intermittent faulted messages not being detected via the scheme's diagnostic suite. In case additional robustness is needed, application level diagnostics should be used.

5.2 Message Definitions

5.2.1 Transmission Sequence

The encoding scheme consists of a sequence of pulses which is repeatedly sent by the transmitting module. The transmission consists of the following sequence (all times nominal):

- Calibration/Synchronization pulse period 56 clock ticks.
- One 4 bit Status and Serial Communication nibble pulse (defined in 5.2.4) of 12 to 27 clock ticks.
- A sequence of one up to six¹ 4 bit Data nibble pulses (12 to 27 clock ticks each) representing the values of the signal(s) to be communicated. The number of nibbles will be fixed for each application of the encoding scheme (i.e., throttle position sensors, mass air flow, etc.) but can vary between applications. For example, if two 12 bit values are transmitted, 6 nibbles will be communicated.
- One 4 bit Checksum nibble pulse (defined in 5.2.5) of 12 to 27 clock ticks.
- One optional pause pulse (defined in 5.2.6)

Figure 5.2.1-1 shows an example single message transmission for two 12 bit sensor values assuming a 3 microsecond clock tick. Note that the shortest length message, based on a valid checksum (determined using approach documented in section 5.4.2.2) consists of 154 clock ticks (Data nibbles [0 0 1 1 0] and Checksum 0, Data nibbles [0 0 1 0 0 0] and Checksum 1, and Data nibbles [1 0 0 0 0 1] and Checksum 0). Similarly, the longest message is 270 clock ticks (Data nibbles [\$E\$ \$F\$ \$F\$ \$F\$ \$F\$ \$E\$] and Checksum \$F\$, Data nibbles [\$F\$ \$F\$ \$E\$ \$F\$ \$F\$ \$F\$] and Checksum \$E\$, and Data nibbles [\$F\$ \$F\$ \$F\$ \$E\$ \$E\$ \$F\$] and Checksum \$F\$).

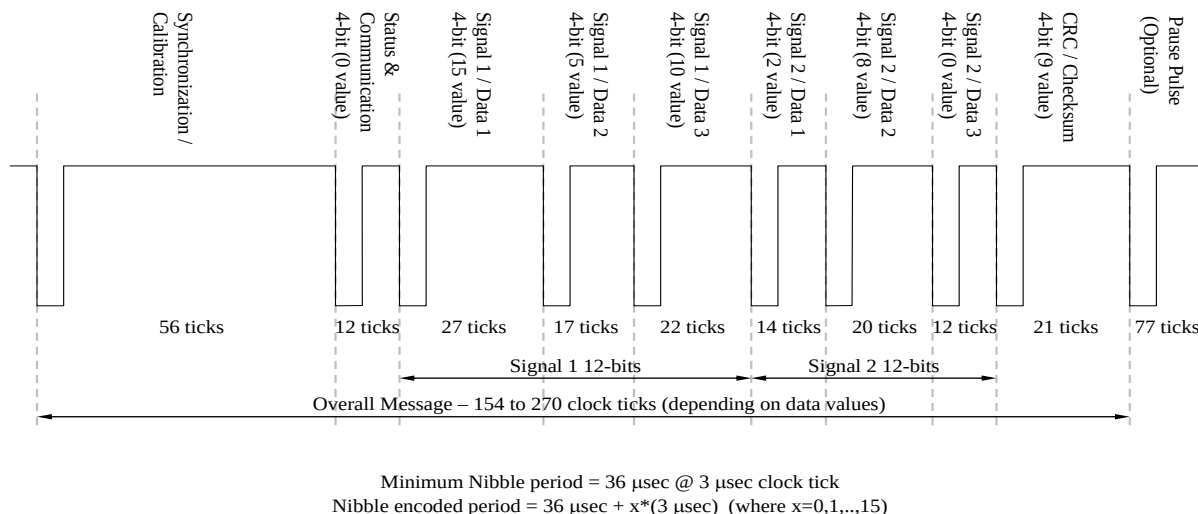


Figure 5.2.1-1 – Example encoding scheme for two 12 bit signals

Signals conveyed using the Data nibbles are also referred to as “Fast Channel” signals with this specification.

¹ For SENT receiver implementations, it is highly recommended to allow for up to at least 8 data nibbles to enable a forward-compatibility with future revisions of the J2716 standard.

5.2.2 Transmission Properties of Calibration/Synchronization Pulse

- Nominal pulse period is 56 clock ticks.
- More than 4 clock ticks driven low time (all remaining clock ticks driven high).
- Actual period measured by receiving module to correct for transmitter clock variation.

5.2.3 Transmission Properties of Nibble Pulse

- Minimum pulse period is 12 clock ticks.
- More than 4 clock ticks driven low time (all remaining clock ticks driven high).
- Each nibble count is 1 clock tick (0 – 15 counts $\Rightarrow$ 0 – 45 μ s at a 3 μ s clock tick).
- Minimum nibble pulse period (transmission value of 0) = 12 clock ticks (36 μ s at a 3 μ s clock tick).
- Maximum nibble pulse period (transmission value of 15) = 12 + 15 = 27 clock ticks (36 + 45 = 81 μ s at a 3 μ s clock tick).

See Figure 5.2.3-1 and Figure 5.2.3-2 for pictorial representation of some nibble properties.

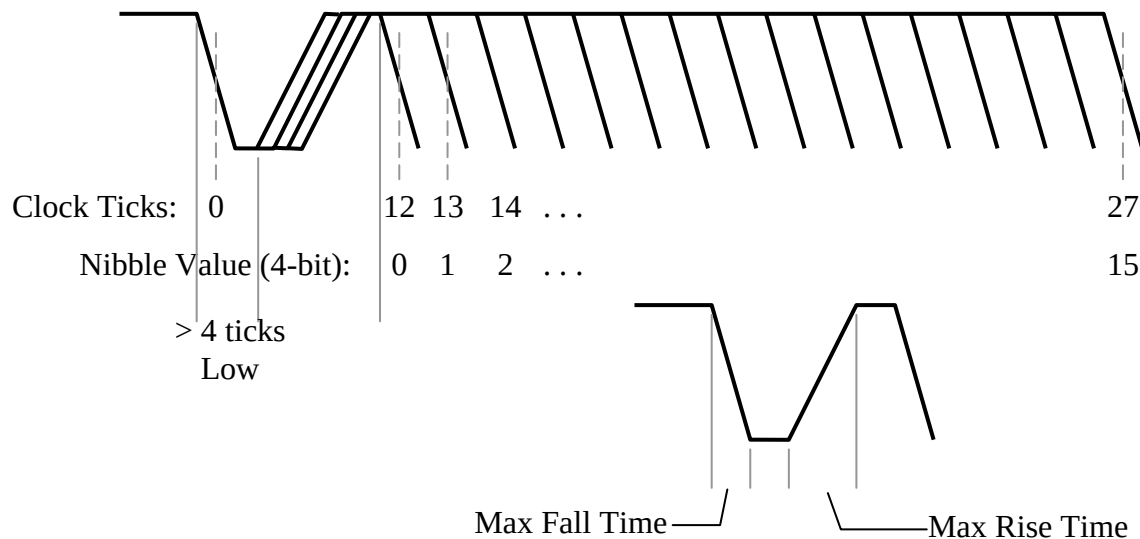


Figure 5.2.3-1 – Example nominal nibble times

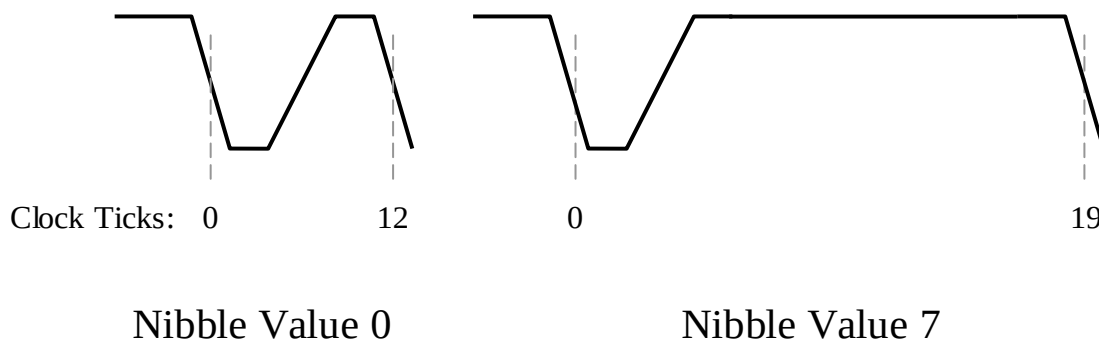


Figure 5.2.3-2 – Continued example nibble values

5.2.4 Status and Communication Nibble

This nibble is reserved to enable the sensor to transmit miscellaneous information such as part numbers or error code information. The nibble is defined in the following table:

Table 5.2.4-1 – Status and communication nibble description

Bit Number	Bit Function
0 (least significant)	Reserved for specific application
1	Reserved for specific application
2	See section 5.2.4.1 and 5.2.4.2 for definition of serial data message bits.
3 (most significant)	

Note that the Status and Communication Nibble is not included in the frame CRC calculation and therefore can have a higher occurrence of non-detected errors.

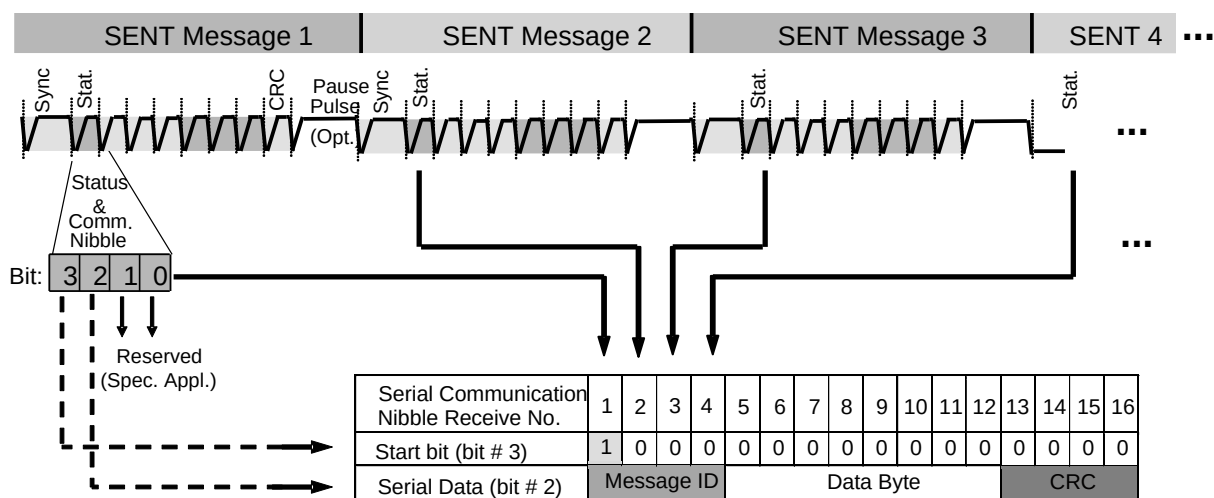
Bits 2 and 3 define a transmitter optional serial message channel which can be implemented either as a short serial message format or an enhanced serial message format as specified below. SENT receivers shall support both the short serial message format as well as the enhanced serial message format. The Enhanced Serial Message Format is recommended rather than the Short Serial Message Format.

5.2.4.1 Short Serial Message Format

Serial data is transmitted (bit by bit) in bit 2 (of the Status and Communication nibble) of consecutive messages from the transmitter. Serial data will be communicated in a 16-bit sequence as shown in Figure 5.2.4.1-1. The starting bit of a serial message is indicated by a “1” in bit 3 of the Status and Communication nibble. The next 15 received frames must contain a value of “0” in this same bit 3 position, as shown in Figure 5.2.4.1-1. All 16 frames must be successfully received (no errors, calibration pulse variation, data nibble CRC error, etc.) for the serial value to be received (Figure 5.2.4.1-1).

The 16-bit message consists of a 4 bit Message ID, a Data Byte, and a 4 bit CRC checksum. The CRC checksum is derived for the Message ID and Data Byte and is the same checksum algorithm as used to calculate the SENT CRC nibble (see 5.4). The Message ID is used to identify the type of data being communicated in the Data Byte. Actual Serial Data message IDs and data values are application specific.

All data transmitted in the Serial Data Bit (bit #2) is sent in the order Most Significant Bit to Least Significant Bit.



One serial message is composed of 16 SENT consecutive error-free messages.

Figure 5.2.4.1-1 – Construction of short serial data message from 16 SENT messages

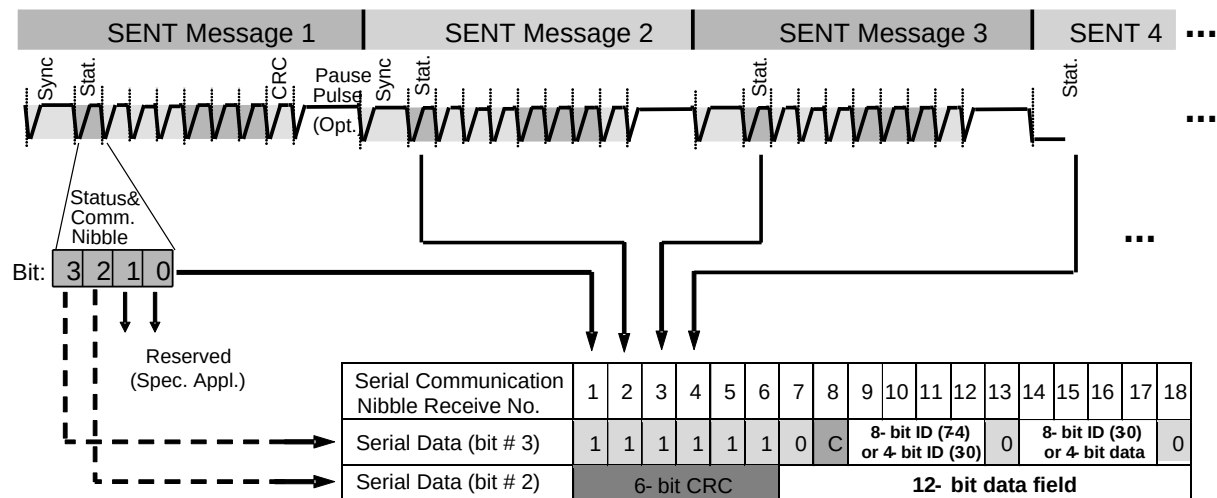
5.2.4.2 Enhanced Serial Message Format

An optional enhanced serial message format can be used by sensors, which require a serial communication channel with a larger data field and a larger set of message IDs. If the enhanced serial message format is used, serial data is transmitted in bit #2 and bit #3 of the status and communication nibble. A serial message frame stretches over 18 consecutive SENT data messages from the transmitter as shown in Figure 5.2.4.2-1. All 18 frames must be successfully received (no errors, calibration pulse variation, data nibble CRC error, etc.) for the serial value to be received.

The table in Figure 5.2.4.2-1 defines the frame format. The frame start of a serial message is indicated by the unique pattern “01111110” in bit 3 of the status and communication nibble (SENT message #18, #1 to #7). The first “1” in a series of six ones (after a “0”) indicates the start of a serial message frame. The “0” in SENT message #13 is defined to ensure the uniqueness of the start pattern. At initialization, it is recommended that the transmitter send the Serial data bit #3 sequence “0...01111110” (start with one or more SENT messages equivalent to #18). One starting “0” will guarantee the minimum latency start sequence and no interrupted message (due to sensor reset) will appear to be completed and incorrectly pass the CRC.

The serial message frame contains 20 bits of payload data. Two different configurations can be chosen determined by the configuration bit (serial data bit #3, serial communication nibble No. 8):

- 12-bit data and 8-bit message ID (configuration bit = 0)
- 16-bit data and 4-bit message ID (configuration bit = 1)



One serial message is composed of 18 SENT consecutive error-free messages.

Figure 5.2.4.2-1 – Construction of enhanced serial data message from 18 SENT messages

All data (data field, message ID and CRC) that is transmitted in the serial message channel is sent in the order MSB (most significant bit) to LSB (least significant bit). The mapping and the order of the data bits, the message ID, the configuration bit and the CRC is detailed in Figure 5.2.4.2-2 for the configuration 12-bit data + 8-bit ID and in Figure 5.2.4.2-3 for the configuration 16-bit data and 4-bit ID.

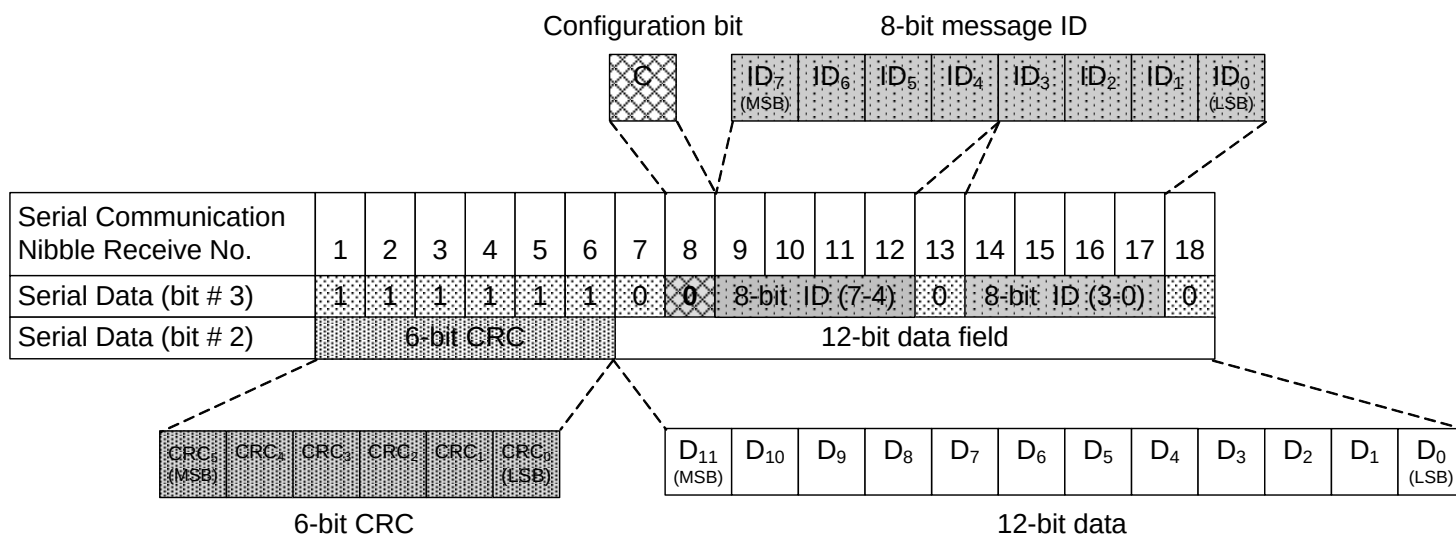


Figure 5.2.4.2-2 – Enhanced serial message format with 12-bit data field and 8-bit message id

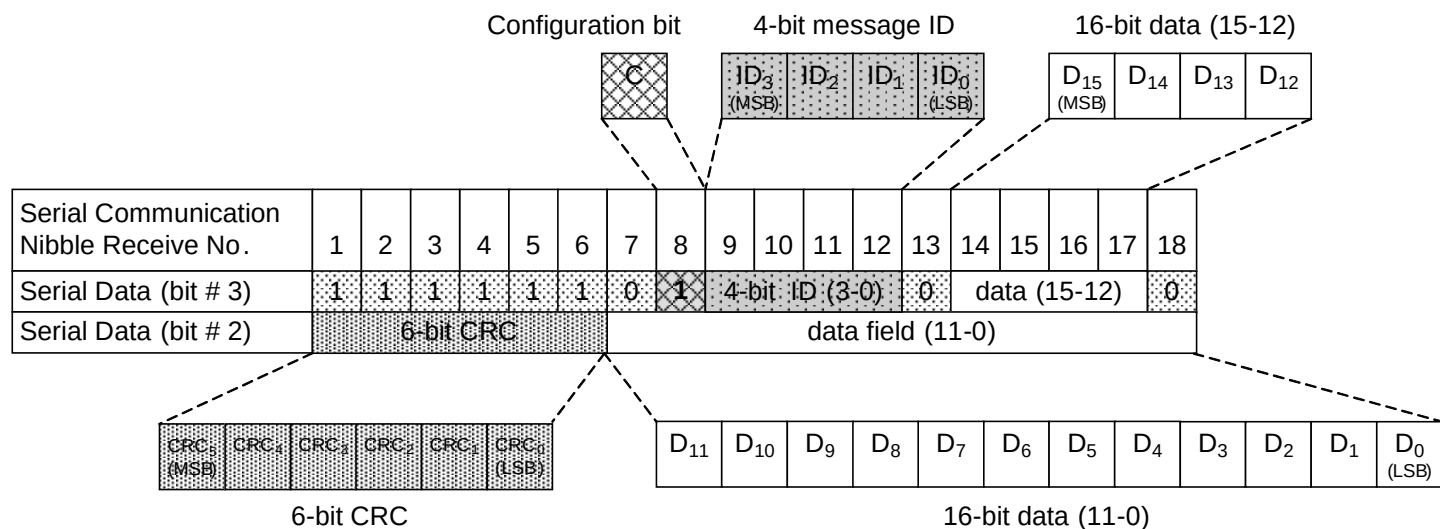


Figure 5.2.4.2-3 – Enhanced serial message format with 16-bit data field and 4-bit message id

5.2.4.3 Enhanced Serial Message Format CRC

This CRC-value is computed as a function of the contents of Serial data message bits #2 and #3 for frames 7-18 (the 12-bit data field, the 8-bit message ID, the configuration bit and “0” bits 7, 13 and 18). For purposes of the CRC calculation, the bits shall be ordered: $m = [\text{Frame 7 bit\#2}, \text{Frame 7 bit\#3}, \text{Frame 8 bit\#2}, \text{Frame 8 bit\#3} \dots \text{Frame 18 bit\#2}, \text{Frame 18 bit\#3}]$, see Figure 5.2.4.3-1. These bits contribute to the message data $m = [m_0 \ m_1 \ m_2 \ \dots \ m_{21} \ m_{22} \ m_{23}]$. Bit m_0 (which corresponds to frame bit D_{11} is the first received bit that is read-in for CRC generation, as illustrated in the lower half of Figure 5.2.4.3-1.

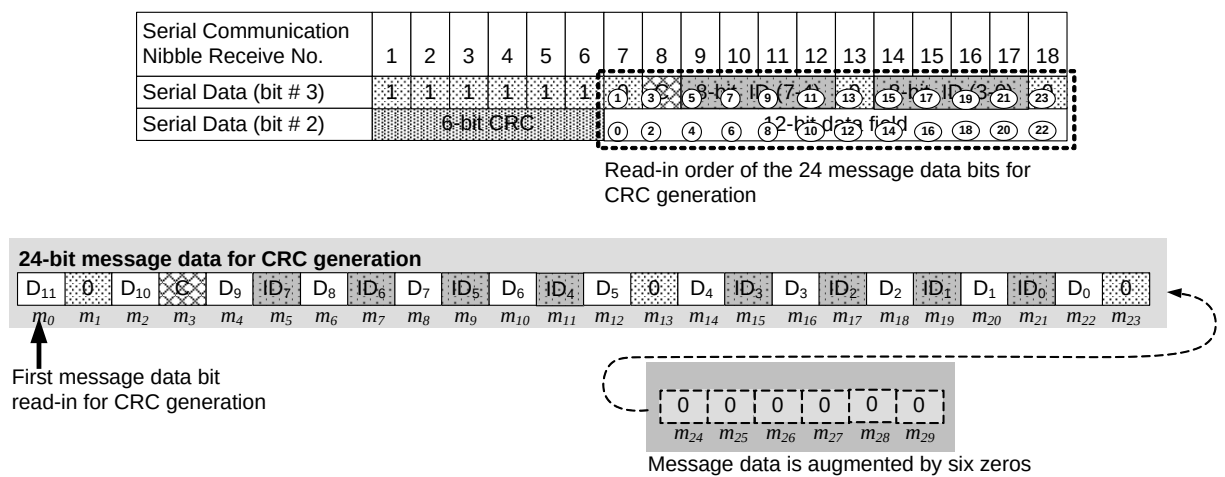


Figure 5.2.4.3-1 – Order of the message bits, 24-bit message used for CRC generation

The encoding is defined by the generating polynomial.

$$G(x) = x^6 + x^4 + x^3 + 1$$

with seed value 010101 (0x15 hex, 21 dec). For CRC generation, the message will be augmented by six zeros $m_{crc} = [m_0 \ m_1 \ m_2 \ \dots \ m_{21} \ m_{22} \ m_{23} \ 0 \ 0 \ 0 \ 0 \ 0 \ 0]$ and the 6-bit data for the CRC calculation processed as follows.

data(1) = { m₀ (=MSB), m₁, m₂, m₃, m₄, m₅ (=LSB) }

data(2) = { m₆ (=MSB), m₇, m₈, m₉, m₁₀, m₁₁ (=LSB) }

etc.

The 6-bit CRC polynomial $x^6 + x^4 + x^3 + 1$ allows to detect all 1-bit, 2-bit, 3-bit, 5-bit errors. The number of undetected 4-bit errors depends on the number of message data bits as shown in the Table 5.2.4.3-1.

Table 5.2.4.3-1 – Undetected 3 and 4 bit errors

Message Data	Number of undetected 3-bit errors	Number of undetected 4-bit errors
24 bit	0	365
24 bit + error detection of frame bits 7, 13 and 18	0	208

The number of possible 4-bit error patterns is $\binom{24}{4}$. The percentage of undetected 4-bit errors is approximately 3.4%.

The three serial data bits #3 of frames No. 7, 13 and 18 are known to be zero. If any of the three serial data bits #3 of nibbles No. 7, 13 and 18 differs from zero, the frame shall be considered as erroneous. This reduces the number of undetected 4-bit errors from 365 to 208.

5.2.4.3.1 Implementation Example for Enhanced Serial Message Format CRC

The CRC checksum can be implemented via a bit-wise exclusive OR with a 64 array lookup. The checksum is determined by reading-in 6-bit groups (in decimal representation) of the 24-bit message data in sequence, and then checksumming the result with an extra zero value (augmentation by six 0-bits). An example MATLAB implementation is:

```
% Table-based CRC generation with Matlab
% 24-bit message data
% data = 4 x 6-bit (Attention: Difference to 4-bit nibbles)
% data(1) = { m0 (=MSB), m1, m2, m3, m4, m5 (=LSB) }
% data(2) = { m6 (=MSB), m7, m8, m9, m10, m11 (=LSB) }
% etc.

% CRC table for poly = 0x59 (x^6+x^4+x^3+1)
% Seed 0x15 (21)
crc6_table = [ ...
    0 25 50 43 61 36 15 22 35 58 17 8 30 7 44 53 ...
    31 6 45 52 34 59 16 9 60 37 14 23 1 24 51 42 ...
    62 39 12 21 3 26 49 40 29 4 47 54 32 57 18 11 ...
    33 56 19 10 28 5 46 55 2 27 48 41 63 38 13 20 ];

Checksum64 = 21; % initialize checksum
for I=1:4
    Checksum64 = bitxor(uint8(data(I)), uint8(crc6_table(Checksum64+1)));
end
% checksum with an extra "0" value (message is augmented by six zeros)
Checksum64 = bitxor(uint8(0), uint8(crc6_table(Checksum64+1)));
```

Examples of the CRC computation are given in Appendix B.2.

5.2.4.4 Non-usage of Serial Message

If no serial message is to be transmitted, both serial data bits shall be set to zero for both formats. If the transmitter needs to interrupt an already commenced serial data sequence, it is the responsibility of the transmitter to ensure that the serial message to be received fails the checksum calculation by corrupting either the data or CRC transmitted. This requirement is not intended to cover transmitter resets.

5.2.5 Checksum Nibble

See 5.4

5.2.6 Pause Pulse (Optional)

The SENT transmission may optionally contain an extra fill pulse which is transmitted after the checksum nibble. For example, this pulse can be used to create a SENT transmission with a constant number of clock ticks. If implemented, the pause pulse shall have the following properties:

- Minimum Length 12 ticks (equivalent to a nibble with 0 value)
- Maximum Length 768 ticks (3 * 256)

For a message with 6 data nibbles, the minimum constant length SENT message would be 282 ticks (assuming correct checksum calculation) for a pause pulses range of 12 ticks to 128 ticks. If a maximum message length of less than 1ms is desired then the transmitter clock tick time tolerance must be decreased to (-20%, +18%) (see Table 6.2.1-1).

5.3 Transmission and Reception of Message

5.3.1 Transmission of Message

Each specific implementation of the encoding scheme (e.g., throttle sensors, pedal sensors, mass air sensors, etc.) shall have a defined sequence, a calibration pulse followed by a constant number of nibbles (and possibly a pause pulse). The transmitting module shall send the defined sequence repeatedly.

5.3.2 Adjustment of Received Message Nibble Lengths

The ECU shall receive the encoded signal by monitoring the time between falling edges (the pulse period). The measurement of a pulse period equal to the calibration pulse $\pm 20\%$ shall signal the start of a new message. The actual period of the calibration pulse received shall be used to adjust the period of the succeeding nibble pulses within the message. This calibration pulse is required to correct for clock tick time variation in the sensor/transmitting device.

The ratio R_{cal} between the measured calibration pulse period and the nominal (56 clock tick) period shall be calculated. Each of the message's remaining measured (nibble) pulse periods is then divided by this ratio to correct them back to the equivalent nominal period. These corrected periods then have the 12 clock tick minimum period subtracted and the resulting data length period divided by the nominal clock tick period and rounded to an integer value to obtain the data nibble value. The process is summarized by the following algorithm:

$R_{cal} = \text{Measured Calibration pulse period} / (56 * \text{Ticknom})$

$\text{Data Value } N = \text{Round}[(\text{Measure pulse period } N / R_{cal} - 12 * \text{Ticknom}) / \text{Ticknom}]$

Figure 5.3.2-1 shows the interpretation in a graphical way.

This section is intended to describe the theory of how data nibbles are to be interpreted by a receiver. Other methods which achieve this same end result are also acceptable.

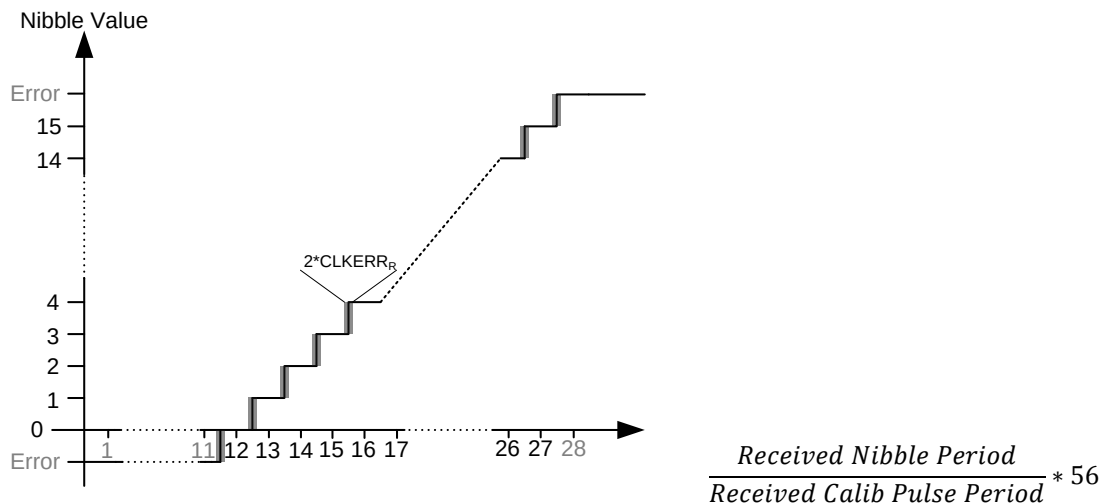


Figure 5.3.2-1 – Quantisation of sampled and calibrated nibble

5.3.3 Received Message Diagnostics

The receiver module shall monitor the message for the following conditions. If any of the below conditions are met, the receiver module shall declare that a message error has occurred and ignore the entire message. Note, not all diagnostics need to be run for each individual message if the message has already been deemed to be in error by a previous diagnostic.

- Calibration pulse length < 56 clock ticks $- 25\%$ or > 56 clock ticks $+ 25\%$.
- Not the expected number of falling edges between calibration pulses. (Message length is pre-defined by each sensor device)
- Checksum error.
- Any nibble data values measured as < 0 or > 15 .
- One of the following two conditions
 - Successive calibration pulses differ by $> +1.5625\%$ (1/64) or $< -1.5625\%$. See section 5.3.3.1 for more detail
 - (for pause pulse with fixed message length only) Ratio of calibration pulse to message length varies by $> 1.5625\%$ or $< -1.5625\%$. To minimize message latency, this diagnostic can be used as the receiver does not need to wait for the next calibration pulse to diagnose the current received frame. It is only recommended for precisely controlled constant message length.

Any of the errors above shall also cause the receiver to begin searching for a valid calibration pulse to re-synchronize reception to the transmitting device start of message. The diagnostics above will allow the reception of message with $\pm 25\%$ clock tick timing range. However, only systems with a maximum $\pm 20\%$ timing range will be certified as meeting the SENT requirements. Note, messages exceeding the 20% clock tolerance should be received correctly but may exceed the 1 ms transmission time target (3 μ s clock tick).

For systems with a pause pulse, during synchronization or re-synchronization of reception, if calibration pulses are detected one immediately following the other, the first calibration pulse shall be ignored as it may be a pause pulse with duration matching the calibration pulse range.

5.3.3.1 Successive Calibration Pulses

The diagnostic for detecting successive calibration pulses differing by $> 1.5625\%$ shall be implemented by one of two methods. Options are described with reference to Figure 5.3.3.1-1 where the calibration pulse of Frame n differs from Frames n-1, n+1 and n+2 by $> 1.5625\%$ threshold.

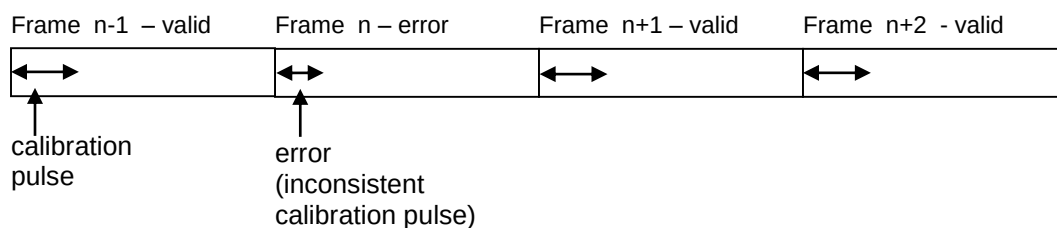


Figure 5.3.3.1-1 – Error pattern for successive calibration pulse detection

Preferred Option:

The calibration pulse of current frame is compared to the calibration pulse of the preceding frame. If they differ by > the threshold 1.5625%, the preceding frame is declared to be bad and ignored. No special initialization or resynchronization is required.

- i. Calibration pulse n-1 is compared to calibration pulse n and the entire message of Frame n-1 is declared to be bad even though the calibration pulse is correct.
- ii. Calibration pulse n is compared to calibration pulse n+1 and the entire message of Frame n is declared to be bad.
- iii. Calibration pulse n+1 is compared to calibration pulse n+2. Message n+1 passes the test.

Advantages of the Preferred Option:

- “Too many nibbles between calibration pulses” can be detected
- Clock variation affecting calibration pulse and immediately preceding or succeeding nibbles can be detected.

Disadvantages of the Preferred Option:

- Potentially, a valid frame (frame n-1) could be declared to be bad
- There is an extra latency of the length of the calibration pulse in processing the message in the receiver (see Figure 5.3.3.1-2).

Option 2 (should only be used if extra latency to process second calibration pulse cannot be tolerated)

The calibration pulse of current frame is compared to the calibration pulse of the last valid preceding frame (i.e., frame with no errors). If they differ by > the threshold 1.5625%, the frame is declared to be bad and ignored.

Initialization: The first calibration pulse shall be considered valid unless the message frame contains other errors.

Resynchronization: On the third successive calibration pulse error, the current calibration pulse value shall be considered as valid and the message accepted unless the message frame contains other errors.

- i. Calibration pulse n is compared to calibration pulse n-1 and the entire message of Frame n is declared to be bad.
- ii. Calibration pulse n+1 is compared to calibration pulse n-1 and the entire message of Frame n+1 is declared to be valid.
- iii. Calibration pulse n+2 is compared to calibration pulse n+1. Message n+2 passes the test.

Advantages of Option 2:

- Message processing can be completed within 1 ms worst case timing

Disadvantages of the Option 2:

- “Too many nibbles between calibration pulses” cannot be detected as the next calibration pulse has not been received.
- Clock variation affecting calibration pulse and immediately succeeding nibbles cannot be detected by calibration pulse comparison.

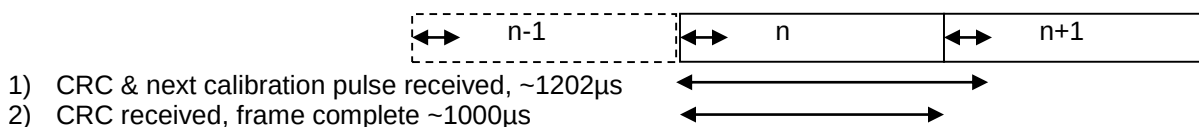


Figure 5.3.3.1-2 – Successive calibration pulse detection

5.3.4 Reset

Should the transmitting module reset for any reason, it shall start transmitting a new message immediately following its initialization procedure. The output signal shall be held in the high state until initialization is completed.

If the SENT interface of the transmitting module is initialized after a reset, while the measurement unit of the transmitting module is still initializing, the sensor shall not transmit a value within the measurement data range. It is recommended to transmit the initialization message (value zero), as defined in E.1.

5.4 Checksum Nibble Details

The Checksum nibble is a 4 bit CRC of the Data nibbles only. The Status and Communication Nibble is not included in the CRC calculation.

The CRC is calculated using polynomial $x^4 + x^3 + x^2 + 1$ with seed value of 0101. For CRC generation, the data nibbles will be augmented by a nibble with data = 0. Refer to Appendix B.1 for details.

5.4.1 Errors Detected and Not Detected by Checksum

The following bit flip errors are detectable using the polynomial:

1. All single bit errors.
2. All odd number of nonconsecutive bit errors.
3. All single burst errors of length ≤ 4 .
4. 87.5% of single burst errors of length = 5.
5. 93.75% of single burst errors of length > 5 .

The fault mode of most concern for the signal encoding scheme is a shifted falling edge which would cause one nibble to appear to be a longer (shorter) period followed by a nibble with a shorter (longer) period than intended by the transmitting device. The CRC detects all cases of 1, 2, 4, 8, 9, 10, 12, 13, 14 and 15 count shifts over two nibbles.

The CRC polynomial will not detect all cases of 3, 5, 6, 7, 11 count shifts. These undetectable patterns are listed in Table 5.4.1-1. For example, row 3 of Table 3 has error pattern 101 followed by 11. If nibble 1 was 4 (100) and nibble 2 0 (000), after the bit flips nibble 1 becomes 1 (001) and nibble 2 becomes 3 (011). Nibble 1 has shifted by -3 and nibble 2 by +3. It is assumed that the risk associated with not detecting these types of faults is acceptable given the high update rate available to the encoding scheme.

Table 5.4.1-1 – Bit Flip patterns over two nibbles not detectable using the CRC polynomial

Nibble 1 Error Pattern		Nibble 2 Error Pattern	
8	1000	1	1
13	1101	2	10
5	101	3	11
7	111	4	100
15	1111	5	101
10	1010	6	110
2	10	7	111
14	1110	8	1000
6	110	9	1001
3	11	10	1010

Nibble 1 Error Pattern		Nibble 2 Error Pattern	
11	1011	11	1011
9	1001	12	1100
1	1	13	1101
4	100	14	1110
12	1100	15	1111

Table 5.4.1-2 lists the missed detection rate for the shifted edge failure resulting in a longer followed by a correspondingly equally shortened pulse. Table 5.4.1-3 lists the missed detection rate for the same situation except that the shifted edge results in an offset of one in the change of the shortened versus the longer pulse.

**Table 5.4.1-2 – Checksum missed detection rate, edge shift between two nibbles
(valid frames only, recommended implementation)**

Shift Nibble X	Shift Nibble X+1	Not detected [%]
-15	15	0.00
-14	14	0.00
-13	13	0.00
-12	12	0.00
-11	11	16.00
-10	10	0.00
-9	9	8.16
-8	8	0.00
-7	7	4.94
-6	6	16.00
-5	5	6.61
-4	4	0.00
-3	3	11.83
-2	2	0.00
-1	1	0.00
1	-1	0.00
2	-2	0.00
3	-3	11.83
4	-4	0.00
5	-5	6.61
6	-6	16.00
7	-7	4.94
8	-8	0.00
9	-9	8.16
10	-10	0.00
11	-11	16.00
12	-12	0.00
13	-13	0.00
14	-14	0.00
15	-15	0.00

Table 5.4.1-3 – Checksum missed detection rate, asymmetrical edge shift offset by 1 between two nibbles (valid frames only, recommended implementation)

Shift Nibble X	Shift Nibble X+1	Not detected [%]
-14	15	0.00
-13	14	0.00
-12	13	33.33
-11	12	0.00
-10	11	0.00
-9	10	0.00
-8	9	0.00
-7	8	0.00
-6	7	17.78
-5	6	0.00
-4	5	3.03
-3	4	10.26
-2	3	8.79
-1	2	0.00
0	1	0.00
1	0	0.00
2	-1	7.62
3	-2	8.79
4	-3	2.56
5	-4	12.12
6	-5	0.00
7	-6	0.00
8	-7	0.00
9	-8	0.00
10	-9	0.00
11	-10	0.00
12	-11	20.00
13	-12	0.00
14	-13	0.00
15	-14	0.00
-15	14	0.00
-14	13	0.00
-13	12	0.00
-12	11	20.00
-11	10	0.00
-10	9	0.00
-9	8	0.00
-8	7	0.00
-7	6	0.00
-6	5	0.00
-5	4	12.12
-4	3	2.56
-3	2	8.79
-2	1	7.62
-1	0	0.00
0	-1	0.00
1	-2	0.00
2	-3	8.79

Shift Nibble X	Shift Nibble X+1	Not detected [%]
3	-4	10.26
4	-5	3.03
5	-6	0.00
6	-7	17.78
7	-8	0.00
8	-9	0.00
9	-10	0.00
10	-11	0.00
11	-12	0.00
12	-13	33.33
13	-14	0.00
14	-15	0.00

5.4.2 CRC Implementation

SENT receivers shall be capable of implementing both checksum implementations below but sensors should use the recommended implementation. The same 4-bit CRC implementation shall be used for both a per frame basis (i.e. checksum of all data nibbles) and for Short Serial Message Format checking.

5.4.2.1 Legacy Implementation (as in revision FEB2008 and older)

The CRC checksum can be implemented as a series of shift left by 4 (multiply by 16) followed by a 256 array lookup. An example MATLAB implementation is:

numNibbles is the number of nibbles to be check summed. The data array contains the nibble to be check summed and the 256 table is given below in MATLAB form:

```
% CRC 4 nibble lookup table
CRC4Table= [ ...
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 ...
13 12 15 14 9 8 11 10 5 4 7 6 1 0 3 2 ...
7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8 ...
10 11 8 9 14 15 12 13 2 3 0 1 6 7 4 5 ...
14 15 12 13 10 11 8 9 6 7 4 5 2 3 0 1 ...
3 2 1 0 7 6 5 4 11 10 9 8 15 14 13 12 ...
9 8 11 10 13 12 15 14 1 0 3 2 5 4 7 6 ...
4 5 6 7 0 1 2 3 12 13 14 15 8 9 10 11 ...
1 0 3 2 5 4 7 6 9 8 11 10 13 12 15 14 ...
12 13 14 15 8 9 10 11 4 5 6 7 0 1 2 3 ...
6 7 4 5 2 3 0 1 14 15 12 13 10 11 8 9 ...
11 10 9 8 15 14 13 12 3 2 1 0 7 6 5 4 ...
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 ...
2 3 0 1 6 7 4 5 10 11 8 9 14 15 12 13 ...
8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 ...
5 4 7 6 1 0 3 2 13 12 15 14 9 8 11 10 ...
];
```

```
Checksum = 5; % initialize checksum
for I=1:numNibbles
    tempCS = data(I)+Checksum*16;
    CheckSum = CRC4Table(tempCS+1);
end
```

This implementation is included for backwards compatibility. Based on valid patterns, it is subject to a 42% missed detection rate of edge shifts between the final data nibble and the checksum nibble and is not recommended.



5.4.2.2 Recommended Implementation

The recommended CRC calculation utilizes the same seed value and polynomial as the legacy calculation but also augments the message data with an extra 4 zero bits in the CRC calculation.

Example implementations are given below. Other implementations are possible. For example, the CRC can also be implemented as a series of bit-wise XOR and shift operations or a reduced sized table can be used. Example checksum values are given in APPENDIX B.

5.4.2.2.1 Implementation using 256 Element Array

The CRC checksum can be implemented as a series of shift left by 4 (multiply by 16) followed by a 256 element array lookup. The checksum is determined by using all data nibbles in sequence and then check summing the result with an extra zero value. An example MATLAB implementation is (same CRC4Table as in section 5.4.2.1):

```
Checksum = 5; % initialize checksum
for I=1:numNibbles
    tempCS = data(I)+Checksum*16;
    CheckSum = CRC4Table(tempCS+1);
end
% checksum with an extra "0" value
tempCS = CheckSum*16;
Checksum = CRC4Table(tempCS+1);
```

5.4.2.2.2 Implementation using 16 Element Array

The CRC checksum can be implemented as a bit-wise exclusive OR with a 16 element array lookup. The checksum is determined by using all data nibbles in sequence and then check summing the result with an extra zero value. An example MATLAB implementation is:

```
numNibbles=6; data=[7 4 8 7 4 8]; % initialization & data

%CRC table for poly = 0x1d
crc4_table = [0 13 7 10 14 3 9 4 1 12 6 11 15 2 8 5];

Checksum16 = 5; % initialize checksum
for I=1:numNibbles
    CheckSum16 = bitxor(uint8(data(I)), uint8(crc4_table(CheckSum16+1)));
end
% checksum with an extra "0" value
Checksum16 = bitxor(uint8(0), uint8(crc4_table(CheckSum16+1)));

% expected result for 748748: Checksum16=3
```

6. SENT PHYSICAL LAYER OPERATION

The physical layer is responsible for providing a method of transferring digital data encoded as time between two falling edges of a signal through the communication medium. This results in repeatable and time accurate switching of the input circuit of the physical layer interface which consists of power, ground and signal wires.

6.1 Normal Communication Mode and Transmission Rate

Transmission bit rate is variable depending on the clock tick period, data values sent and the transmitter nominal clock tick time variance and +/-20% clock tolerance. The longest transmission time for 6 Data nibbles is 270 clock ticks or 972 μ s at a 3 μ s clock tick period, this results in a worst case transmission rate of ~24.7 kBits/s. Similarly, the shortest valid 6 Data nibble message is 154 clock ticks which, at -20% clock tick time tolerance, results in a transmission rate of ~64.9 kBits/sec. These calculations ignore the contribution made by Serial data transmission (see 5.2.4).

6.2 Clock Tolerance

6.2.1 Transmitter–Receiver Communications

Table 6.2.1-1 lists the timing and resolution requirements for the transmitting and receiving modules. To avoid requiring a high cost oscillator in the transmitter, the transmitter clock tick time variation is allowed to be large. Requirements for Clock Drift Error and Jitter at intermediate clock tick periods shall be linearly interpolated between the minimum and maximum clock tick periods in Table 6.2.1-1.

Table 6.2.1-1 – Communication clock tolerance

Device Type	Symbol	Parameter	Clock Tolerance
Transmitter	$\Delta T_{osc}/T_{osc}$	Clock Accuracy	$\leq \pm 20\%$ on clock tick time without pause pulse $> -20\%, < + 18\%$, on clock tick time, with pause pulse (optional)
Transmitter	$ClkErr_T$	Clock Jitter and Drift Error (including systematic phase errors)	$\leq 0.3 \mu s^{(1)}$ variation of maximum nibble time ⁽²⁾ compared to the expected time derived from the calibration pulse time at a $3 \mu s$ clock tick ⁽³⁾
Transmitter	$Tick_{nom}$	Clock Tick Period Ranges	3 to $90 \mu s$ nominal ⁽³⁾
Receiver	$ClkErr_R$	Clock Jitter and Drift Error (including sampling quantization)	$\leq 0.3 \mu s^{(1)}$ variation of maximum nibble time ⁽²⁾ compared to the expected time derived from the calibration pulse time at a $3 \mu s$ clock tick ⁽³⁾

¹ In case of Gaussian distributed errors the time variation limit shall be compared to 6σ , where σ is the standard deviation of the absolute difference of measured maximum nibble times to the expected time derived from the corresponding calibration pulses. In case of other distributions the same error margin as for 6σ Gaussian distribution shall be guaranteed. The value for the transmitter is defined for an ideal receiver and the value for the receiver for an ideal transmitter. The value for the transmitter is defined at any constant trigger level as specified in Table 6.3.2-1 c and e.

² The maximum nibble time corresponds to nibbles with 27 clock tick nominal time.

³ For clock tick times greater than $3 \mu s$, transmitter and receiver "Clock Jitter and Drift Error" can be increased linearly proportionally to the $3 \mu s$ clock tick values (see Figure 6.2.1-1).

NOTE: Increased values of the clock jitter and drift error compared to Revision JAN2010 are due to a more precise and inclusive definition of the parameters. This change does not affect the design both of the transmitter and receiver.

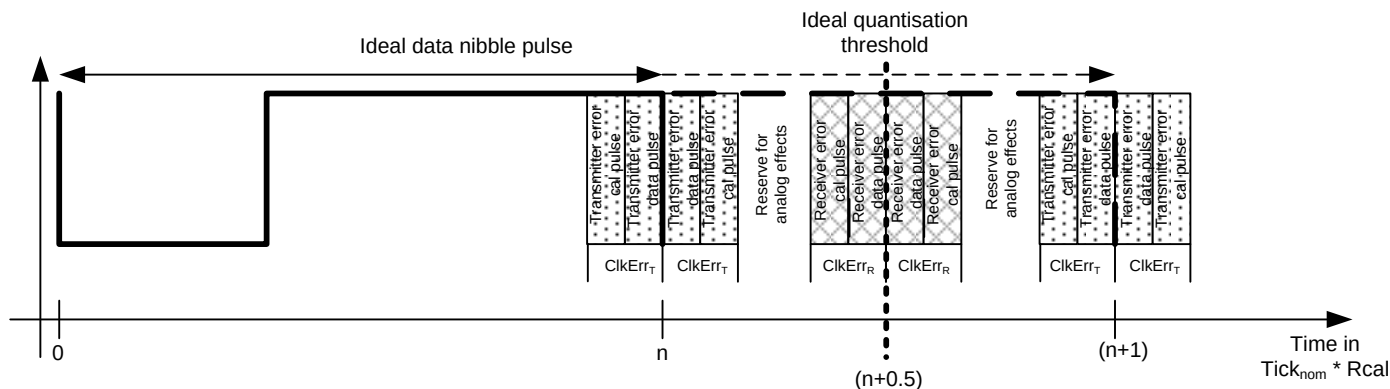


Figure 6.2.1-1 – Illustration of clock error accumulation as given in Table 6.2.1-1.

6.3 Electrical Interface Requirements

The SENT signal can be seen as a nominal 5 V square wave signal, but for low radiated emissions, signal shaping is required. To minimize ground and supply offset effects, the receiving device shall provide a regulated 5 V supply and ground reference to the transmitting device as specified below. This signal is intended to operate in automotive under-hood control system applications. The driver and receiver shall be protected from shorts to ground or vehicle voltages and various transient pulses as required below and by the specific vehicle EMC requirements.

Figure 6.3-1 illustrates a possible equivalent circuit for a SENT transmitter and receiver. The Transmitter portion of this circuit is an example only and should not be taken as a direct implementation requirement. All interface requirements in this document shall be met whether the implementation follows the example circuit topology or not.

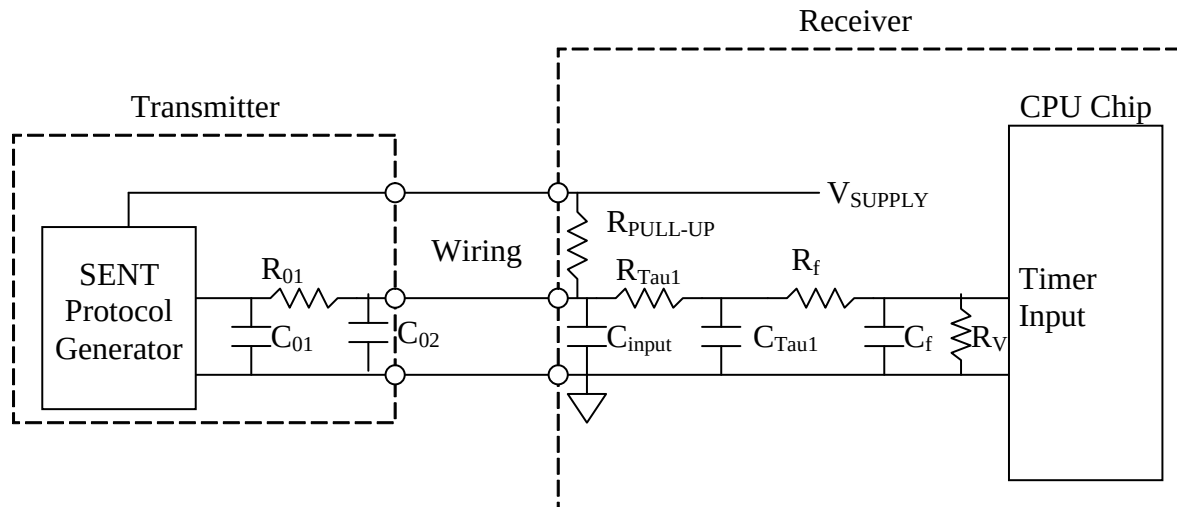


Figure 6.3-1 – Example SENT system interface circuit topology

6.3.1 Transmitter Driver Requirements

The transmitting device shall provide a driver with a configuration and technology suitable for the automotive environment. The driver shall ensure that the signal pulse parameter as defined in Figure 6.3.1-2, Table 6.3.1-1, Table 6.3.1-2 and Table 6.3.1-3 are met when driving into the receiver passive load defined in section 6.3.2. Protection requirements from damage due to voltage or current conditions on the output signal outside those defined in Table 6.3.1-1 shall be defined by the OEM specification. The requirements in Table 6.3.1-1, Table 6.3.1-2 and Table 6.3.1-3 shall be met over the entire transmitter environmental requirement range. Any loss or corruption of the transmitted signal due to open circuit or short of any of the transmitter pins shall be detected by the receiver via the message diagnostic tests defined in Section 5.3.3.

In addition an EMC filter consisting of a capacitor followed by a resistor in series with the output pin is recommended to attenuate RF energy coupled on the external signal line. See Figure 6.3-1. In order to meet radiated emission EMC requirements, it is expected that a “shaped” waveform (controlled slope and corner rounding) will need to be driven by the transmitter. Figure 6.3.1-1 illustrates an example shaped waveform (falling and rising edge) that could meet emissions requirements. SENT transmit pulse parameters are explained in Figure 6.3.1-2.

The transmitter shall meet the input threshold level at the receiver with maximum time constants of the input filters.

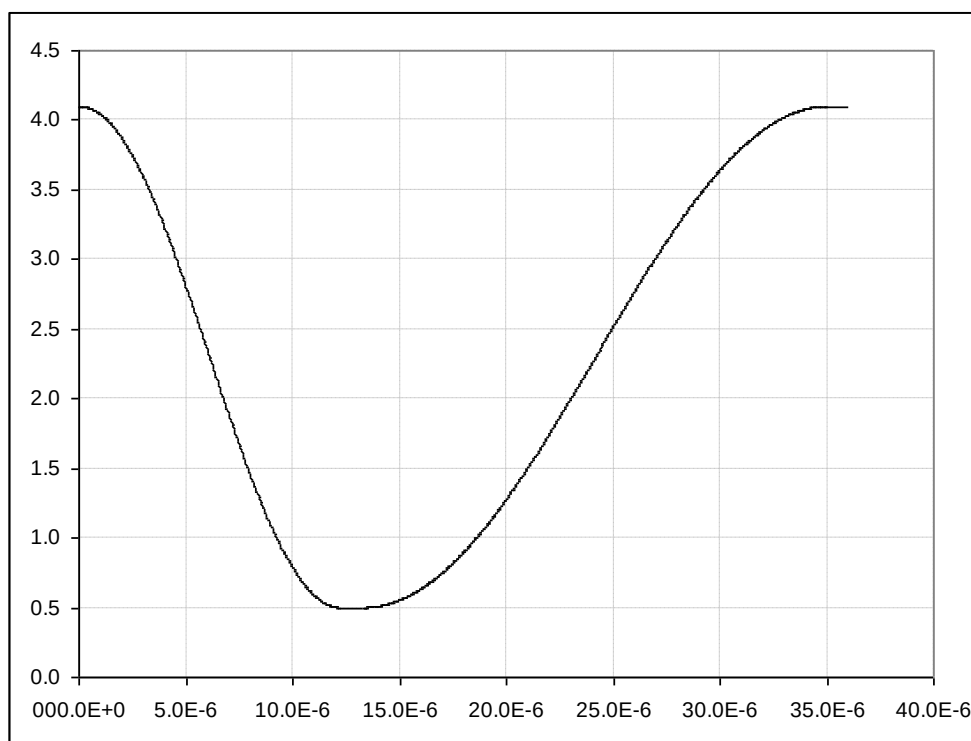


Figure 6.3.1-1 – Example SENT shaped waveform transmitter output

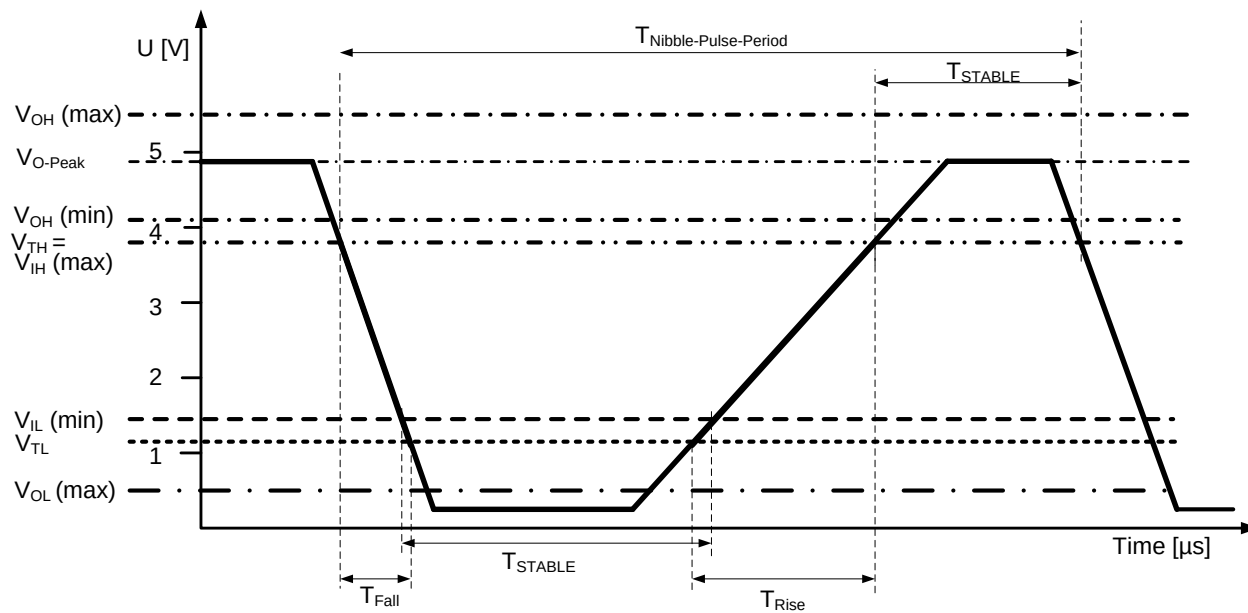


Figure 6.3.1-2 – SENT transmit pulse parameters

Table 6.3.1-1 – Transmitter driver requirements

Parameter			Limits (including component tolerances)		Units	Test Conditions / Definitions (on wire)
			Min	Max		
a.	V _{OL}	=		0.5	V	Low state Voltage @ 0.52 mA DC load current
b.	V _{OH}	=	4.1		V	High state Voltage @ 0.10 mA DC load current
c1.	I _{SUP}	=		50	mA	Average current consumption from Receiver 5V supply over one message
c2.	I _{GND}			50	mA	Average current through (Signal) Ground Line over one message
d.	I _{SUP-RIPPLE}	=		9.0 ⁽³⁾	mA	Peak-to-peak variation in supply current consumption over one message at frequencies up to f _c = 30 kHz measured as described in C.2
e1.	T _{FALL}	=		6.5 ⁽¹⁾	μs	From V _{TH} = 3.8 V to V _{TL} = 1.1 V, I _{SUP} ≤ 20 mA
e2.	T _{FALL}	=		5.0 ⁽¹⁾	μs	From V _{TH} = 3.8 V to V _{TL} = 1.1 V, 20 mA < I _{SUP} ≤ 50 mA
f.	T _{RISE}	=		18 ⁽¹⁾	μs	From V _{TL} = 1.1V to V _{TH} = 3.8V
g.	ΔT _{FALL}	=		0.1 ⁽¹⁾	μs	Edge to edge jitter with static environment for any pulse period
h.	T _{STABLE}	=	6 ⁽²⁾		μs	Signal stabilization time below V _{IL} (min) = 1.39V (low signal) or above V _{IH} (max) = 3.8V (high signal)

¹ For 3μs nominal clock tick including clock accuracy. For higher clock tick times these values can be increased proportionally.

² If “T_{FALL}”, “T_{RISE}” or “ΔT_{FALL}” are increased, T_{STABLE} has to be increased by the same ratio as well.

³ Devices or loads on the transmitter side other than one SENT output circuit may lead to higher current ripple, uncorrelated to that SENT transmission. In this case the current ripple has to be specified and considered in the design of the supply on the receiver side.

In case the transmitter is supplied from the receiver with a regulated 5V power supply as defined in Table 6.3.2-1 the transmitter shall satisfy those requirements defined in 6.3.1, that specify the SENT pulse shape together with the specific requirements in Table 6.3.1-1. The circuit topology for this case is depicted in Figure 6.3.1-3.

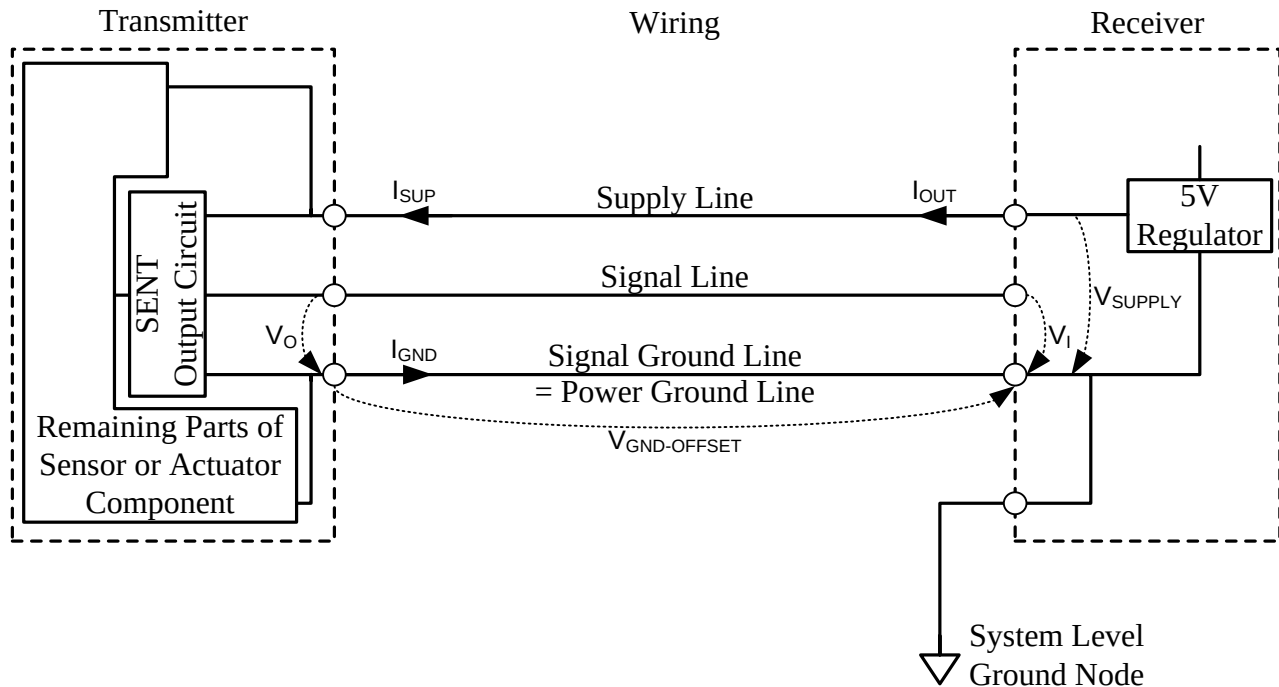


Figure 6.3.1-3 – SENT system interface circuit topology for a regulated 5v power supply of the transmitter by the receiver

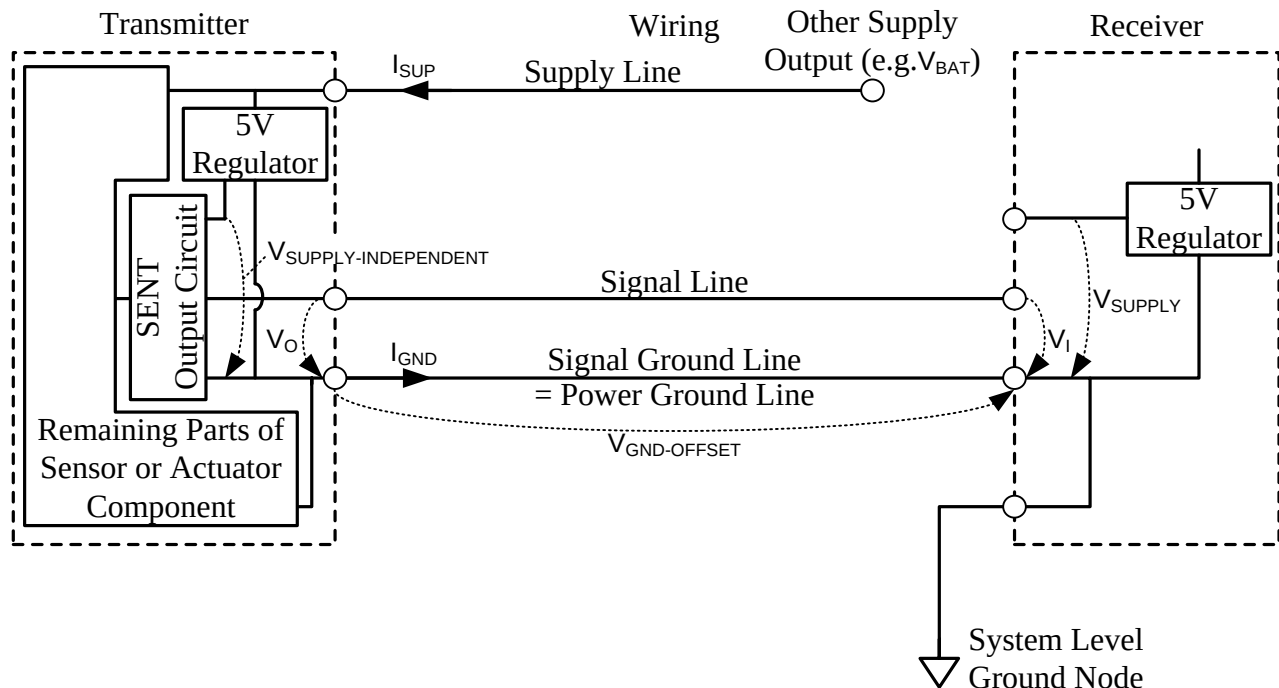


Figure 6.3.1-4 – SENT System Interface Circuit Topology for an Independent 5V Power Supply in the Receiver with Identical Signal Ground Line and Power Ground Line

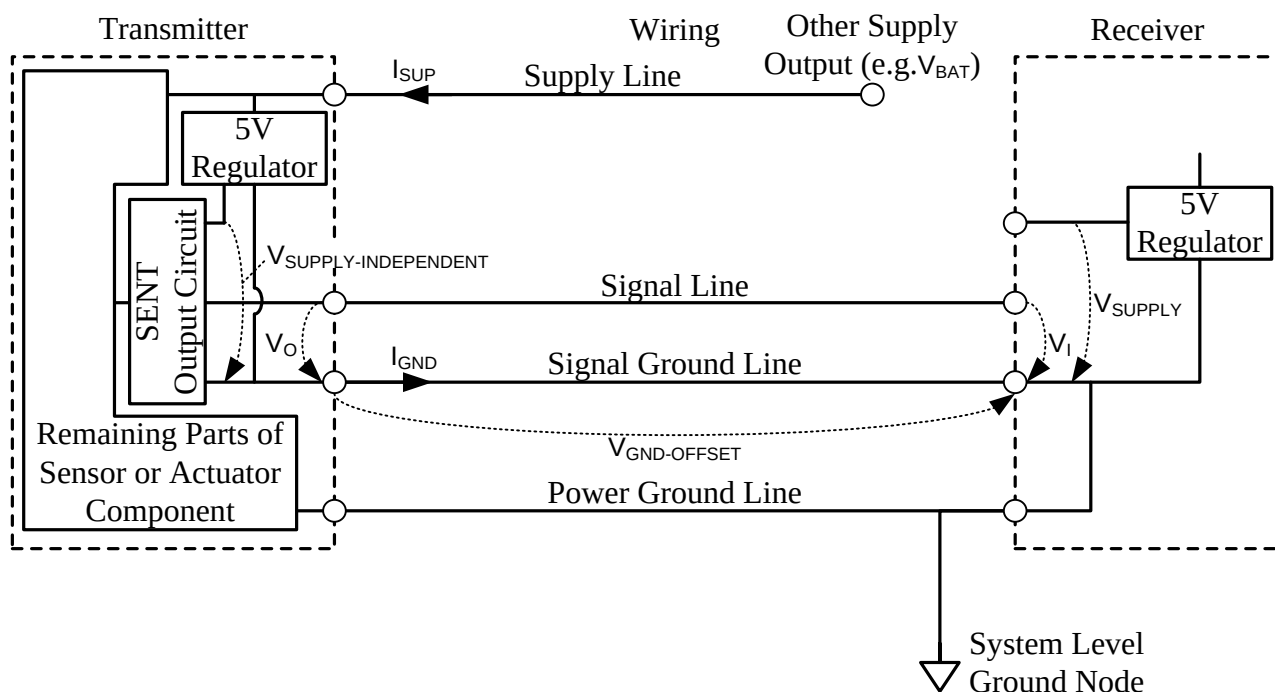


Figure 6.3.1-5 – SENT system interface circuit topology for an independent 5v power supply in the receiver with separate signal ground line and power ground line

The transmitting device may optionally implement a 5V regulator to power the SENT signal driver independently of the power supply from the receiver. In this option, the transmitter shall satisfy those driver requirements defined in 6.3.1, that specify the SENT pulse shape together with the specific requirements for independent 5V powered transmitters, as specified in Table 6.3.1-2. These requirements ensure that the optional transmitter interface will remain compatible with the standard SENT receiver requirements (Table 6.3.2-1). Additional specific requirements for independent 5V powered transmitters that require higher power consumption are specified in Table 6.3.1-3.

Note that while the 5V power may be independent of the receiver, the SENT transmitter shall connect its signal ground line to the ground signal provided by the SENT receiver to ensure that excessive ground offset will not disturb the SENT communication. This may be done with the signal ground line being identical to the power ground line as shown in Figure 6.3.1-4, if the transmitter design ensures sufficiently small ground offset $V_{GND-OFFSET}$ as defined in Table 6.3.1-3 m. Otherwise the power ground line must be isolated from the signal ground line on the transmitter side as shown in Figure 6.3.1-5, and the transmitter design must accommodate any voltage offset between these two signals.

Table 6.3.1-2 – Independent 5v powered transmitter requirements

Parameter			Limits (including component tolerances)		Units	Test Conditions / Definitions (on wire)
			Min	Max		
a.	V_{OL}	=		0.5	V	Low state Voltage @ 0.52 mA DC load current
b.	V_{OH}	=	4.1	5.5	V	High state Voltage @ 0.10 mA DC load current
c.	I_{GND}	=		50	mA	Average current through Signal Ground Line over one message.
e1.	T_{FALL}	=		6.5 ⁽¹⁾	μs	From $V_{TH} = 3.8$ V to $V_{TL} = 1.1$ V, $I_{SUP} \leq 20$ mA
e1.	T_{FALL}	=		5.0 ⁽¹⁾	μs	From $V_{TH} = 3.8$ V to $V_{TL} = 1.1$ V, 20 mA $< I_{SUP} \leq 50$ mA
f.	T_{RISE}	=		18 ⁽¹⁾	μs	From $V_{TL} = 1.1$ V to $V_{TH} = 3.8$ V

Parameter			Limits (including component tolerances)		Units	Test Conditions / Definitions (on wire)
			Min	Max		
g.	ΔT_{FALL}	=		0.1 ⁽¹⁾	μs	Edge to edge jitter with static environment for any pulse period
h.	T_{STABLE}	=	6 ⁽²⁾		μs	Signal stabilization time below V_{IL} (min) = 1.39V (low signal) or above V_{IH} (max) = 3.8V (high signal)
i.	$V_{\text{O-Peak-Range}}$			0.3	V	Stability of pulse peaks $V_{\text{O-Peak-Range}} = V_{\text{O-Peak}}(\text{max}) - V_{\text{O-Peak}}(\text{min})$ over one SENT message at $T_{\text{TICK}} = 3 \mu\text{s}$
j.	$I_{\text{GND-RIPPLE}}$	=		9.0 ⁽³⁾	mA	Peak-to-peak variation in ground current over one message at frequencies up to $f_c = 30 \text{ kHz}$

¹ For 3 μs nominal clock tick including clock accuracy. For higher clock tick times these values can be increased proportionally.

² If " T_{FALL} ", " T_{RISE} " or " ΔT_{FALL} " are increased, T_{STABLE} has to be increased by the same ratio as well.

³ Devices or loads on the transmitter side other than one SENT output circuit may lead to higher current ripple, uncorrelated to that SENT transmission. In this case the current ripple has to be specified and considered in the design of the supply on the receiver side.

Table 6.3.1-3 – Independent 5v supply high power transmitter additional requirements

Parameter			Limits (including component tolerances)		Units	Test Conditions / Definitions (on wire)
			Min	Max		
k1.	$I_{\text{GND-Increased}}$	=		100	mA	Average current through Signal Ground Line over one message (increased value, resulting in I1)
k2.	$I_{\text{GND-High}}$	=		200	mA	Average current through Signal Ground Line over one message (highly increased value, resulting in I2)
l1.	T_{TICK}	=	2.6		μs	Sensors with increased ground current $I_{\text{GND-Increased}}$: Minimum SENT clock tick period required to maintain compatible timing margin with receiver NOTE: 15% clock tolerance needed to achieve 1 ms worst case message transmission time and compatible timing margin
l2.	T_{TICK}	=	3.0		μs	Sensors with with highly increased ground current $I_{\text{GND-High}}$: Minimum SENT clock tick period required to maintain compatible timing margin with receiver NOTE: 10% clock tolerance needed to achieve 1 ms worst case message transmission time and compatible timing margin
m.	$V_{\text{GND-OFFSET}}$	=		200	mV	Sensors with current consumption $I_{\text{SUP-High}}$: Ground offset from transmitter to receiver connectors due to transmitter ground current

6.3.2 Receiver Input Requirements

Figure 6.3.2-1 and Figure 6.3.2-2 show two alternative receiver circuit topologies. One of the two or an alternative circuit (Figure 6.3.2-3) shall be used; however, Figure 6.3.2-1 is included for backwards compatibility with specification version FEB2008, is not recommended for new implementations and cannot be used with Open Drain Type Transmitters. Figure 6.3.2-2 represents the recommended approach for new implementations.

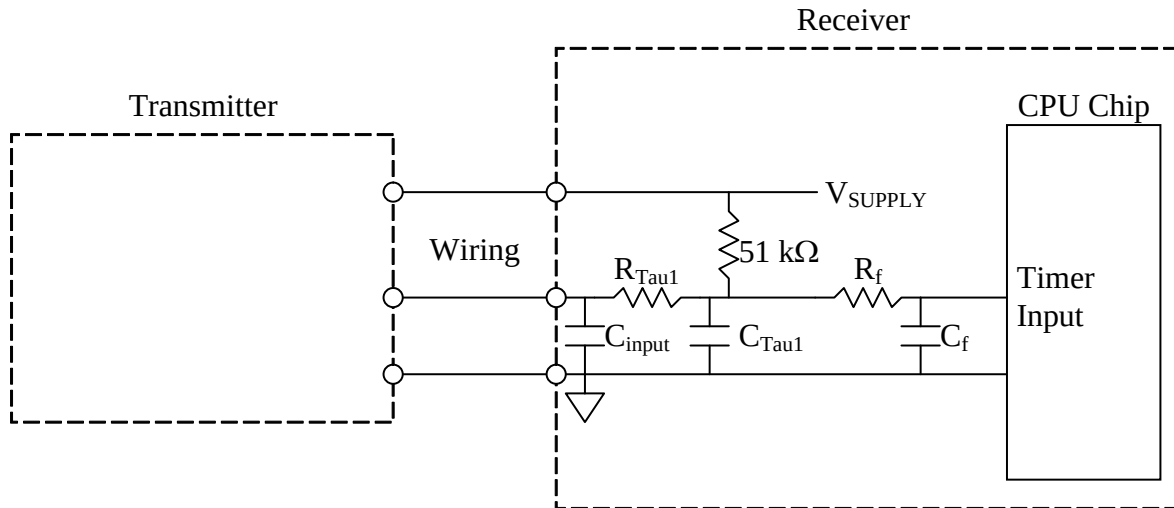


Figure 6.3.2-1 – Legacy SENT receiver interface circuit topology

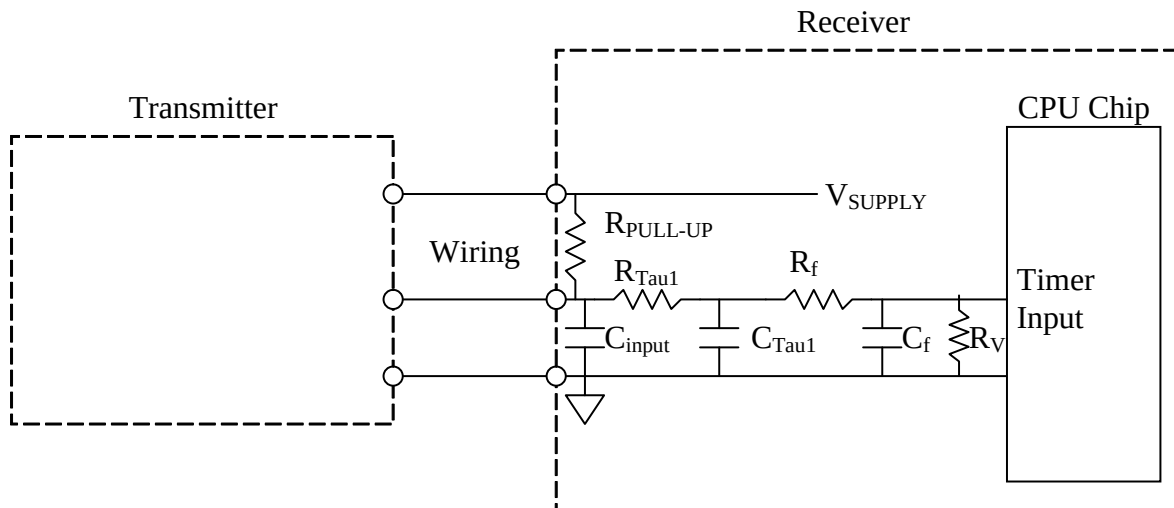


Figure 6.3.2-2 – Recommended SENT system interface circuit topology

The R_v resistor is an optional element used to create a Voltage divider to translate the SENT signal level into a level required by the CPU chip. The recommended discrete receiver input circuit topology (Figure 6.3.2-2) shall be used for transmitter testing and evaluation.

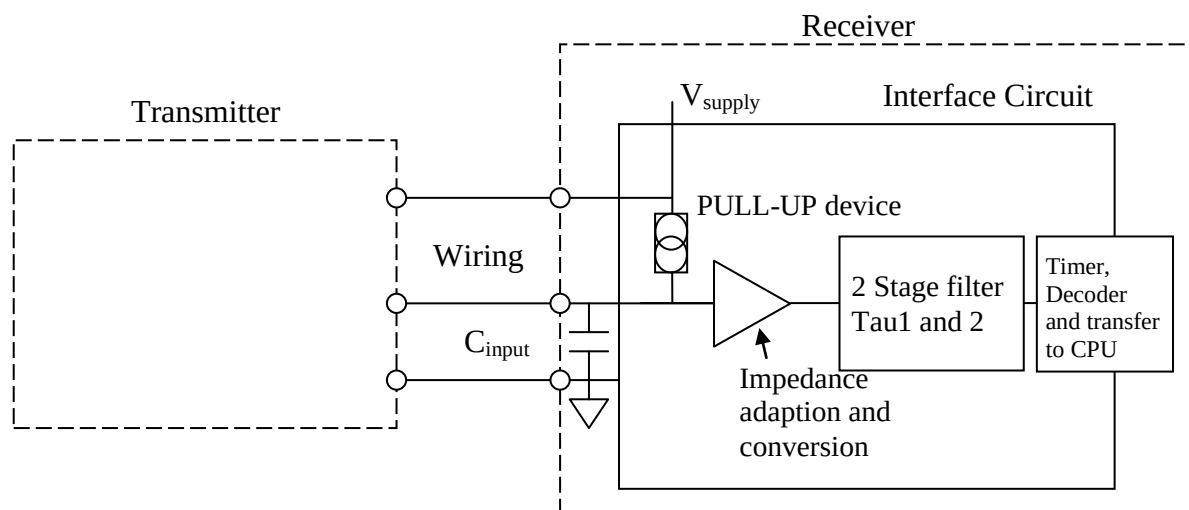


Figure 6.3.2-3 – Example alternative SENT system interface circuit topology

An alternative receiver circuit may be used (e.g., current source instead of the pull-up resistor). The alternative receiver circuit shall be designed such that the function of the SENT sub-system (transmitter and receiver) is equivalent to a sub-system with the reference receiver circuit of Figure 6.3.2-2. See APPENDIX I for more details.

EMC and EMI compliance of transmitter and receiver circuits are not in the scope of this standard, as these requirements are specified and may vary by the **OEM**. Note: both nonlinear behavior and parasitic parameters of the actual receiver circuits will have some influence on the transmitter's EMC performance.

The Receiving device shall provide a pull-up device to the supply voltage, a controlled threshold digital receiver, and a timing channel (to measure pulse periods). The receiver shall meet the requirements of Table 6.3.2-1 over the entire Receiving device environmental requirement range.

Table 6.3.2-1 – General receiver input requirements

Parameter	Limits (including component tolerances)		Units	Test Conditions / Definitions
	Min	Max		
c. V_{IL}	=	1.39	V	Input low state threshold range
d. $V_{IL-DELTA}$	=	-50	mV	Maximum input low state threshold variation over 1 millisecond interval with supply Voltage constant
e. V_{IH}	=	3.8	V	Input high state threshold range
f. V_{HYST}	=	0.3	V	Input electrical hysteresis ($V_{HYST} = V_{IH} - V_{IL}$)
g. τ_{1}	=	0.74	μs	Input filter time constant – first stage
h. τ_{2}	=	0.6	μs	Input filter time constant – second stage determined by R_v , R_f and C_f

If the legacy or recommended discrete receiver input circuits given in Figure 6.3.2-1 and Figure 6.3.2-2 are used, the elements of the circuit shall meet the requirements of Table 6.3.2-2 over the entire Receiving device environmental range. Otherwise, Table 6.3.2-2 shall be used for the definition of equivalent receiver input circuits. See APPENDIX I for analysis requirements.

In case the Receiving device also provides a regulated 5V power supply voltage to the Transmitter, it shall meet the requirements in Table 6.3.2-3 over the entire Receiving device environmental range.

Table 6.3.2-2 – Discrete receiver component values

Parameter			Limits (including component tolerances)		Units	Test Conditions / Definitions
			Min	Max		
a.	R _{PULL-UP}	=	10000	55000	Ohms	Input pull-up resistance
b.	C _{INPUT}	=		0.1	nF	Parasitic input capacitance and ESD protection
i.	R _{Tau1}		448	672	Ohms	560 +/- 20% overall tolerance must meet Tau1 requirement
j.	C _{Tau1}		1.54	2.86	nF	2.2 +/- 30% overall tolerance must meet Tau1 requirement
k.	R _f		4		kΩ	R _f should be chosen in such a way that the 0.1 mA sourcing capability of the transmitter is not exceeded.

Table 6.3.2-3 – Receiver power supply requirements

Parameter			Limits (including component tolerances)		Units	Test Conditions / Definitions
			Min	Max		
a.	V _{SUPPLY}	=	4.85	5.15	V	Supply Voltage
b.	I _{OUT}	=	(1)		mA	Available current for Transmitting device
c.	C _{LOAD}	=		(2)	μF	Supply to return load capacitance in transmitter
d.	V _{GND-OFFSET}	=		0.02	V	Signal return ground offset in Receiving device
e.	V _{3.3SUPPLY}	=	3.234	3.366	V	Internal 3.3 V supply (if needed by Receiver)

¹ The Receiver Power Supply shall be dimensioned application specific according to the Power Supply needs and current consumption of the connected sensors. The Power Supply dimensioning needs also include increased start up and ripple currents.

² OEM or application specific requirements may limit capacitive loading at sensor supply outputs.

6.3.2.1 ESD Transient Suppressor

If necessary, a circuit element such as a transorb (back-to-back zener) or a varistor device may be added in one or more places to provide ESD protection. However, when these devices are used they may add capacitance or introduce voltage and/or temperature variability to the signal time constant. When such devices are used the device load capacitor shall be reduced by an amount equivalent to the capacitance of the ESD transient suppressor.

6.3.3 Bus Wiring Harness and ECU Connectors

Combined resistance for all connectors and wiring shall have less than 1 Ohms per line over total vehicle life. The bus wiring shall utilize cables with less than 0.1nF per meter of wire length. The maximum cable length shall be 5 meters.

6.4 ESD Immunity

The transmitting and receiving module I/O pins shall withstand electrostatic discharges without any damage to the transmitting or receiving module when subjected to testing per the vehicle manufacturer's component Electrostatic Discharge test. The particular vehicle manufacturer's component technical specification shall state the Criticality Level of the device.

6.5 EMC Testing Requirements

The physical layer, when incorporated into an ECU or sensor design, shall function as specified in the device's intended electromagnetic environment. Additionally, the electromagnetic emissions produced during signal related operations shall not interfere with the normal operation of other ECU's or subsystems.

The particular vehicle manufacturer's component technical specification shall state the EMC testing requirements of the device.

6.6 Fault Protection Modes

Data communications may be interrupted under short of any impedance to supply or ground.

1. Wiring Short to Ground – There shall be no damage to any device when the signal or supply line is shorted to ground. An impedance of less than 50 ohms between the line and ground shall be considered a short to ground. Upon removal of the fault, a transmitter reset may occur and normal operation shall resume within the transmitter reset time. Operator intervention (for example a key cycle) shall not be required.
2. Wiring Short to Supply – There shall be no damage to any device when the signal or ground line is shorted to sensor supply V_{OUT} . An impedance of less than 50 ohms between the line and V_{OUT} shall be considered a short. Upon removal of the fault, a transmitter reset may occur and normal operation shall resume within the transmitter reset time. Operator intervention (for example a key cycle) shall not be required.

7. CONFIGURATION SHORTHAND

7.1 Shorthand Definition

A shorthand description for the various optional configurations is constructed using the following format and Table. Elements of the table are separated by dashes to form the final shorthand notation.

Table 7.1-1 – SENT configuration shorthand definition

Shorthand Description	Format	Requirements
SENT SAE J2716 revision	SENTxxxx	One of the following values depending on SENT revision supported: • 2007 • 2008 • 2010 • 2016
Clock Tick Length [μs]	xx.xus	$03.0 \leq xx.x \leq 90.0$
Number of Data Nibbles	x _{dn}	$1 \leq x \leq 6$
Pause Pulse Option	npp pp ppc(xxx.x)	no pause pulse pause pulse pause pulse with constant frame length, xx is number of clock ticks, $282.0 \leq xxx.x \leq 922.0$ (for 6 data nibbles)
Use of Serial Protocol	ssp esp nsp	short serial protocol enhanced serial protocol no serial protocol
Sensor Type	Ns A.1 A.3 A.4 D.1xxx ...	Not specified here (see manufacturer specification) Additional appendices may be referenced. Some examples: Dual Throttle Position sensors described in Appendix A.1 Single Secure sensors described in Appendix A.3 Single sensors described in Appendix A.4 Sensors class given in Table D.4.1-1, xxx are nibble values for bits D ₁₁ through D ₀ (APPENDIX D represents the sensors defined in Appendices A.2 and A.5)

Example Shorthand Description: SENT2010-03.0us-6dn-ppc(282.0)-nsp-A.1