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Clock Extension Peripheral Interface (CXPI)

RATIONALE

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FOREWORD

The objective of this document is to define a level of information in the implementation of low speed vehicle serial data network communications using the Clock Extension Peripheral Interface (CXPI) protocol.

The goal of this document is to provide an overview of the CXPI protocol describing the features and functions of the serial data physical layer, data link layer and application layer for use in the automotive Electronic Control Units (ECU). This standard will allow ECU and tool manufacturers to satisfy the needs of multiple end users with minimum modifications to the basic design. This standard will benefit vehicle Original Equipment Manufacturers (OEMs) by achieving lower ECU costs due to higher industry volumes of the basic design.

NOTE: Understanding of this document requires the knowledge of the JASO Clock Extension Peripheral Interface (CXPI) specification.

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1. SCOPE

1.1 Mission/Theme

This document is an information report and intended to provide an overview of the Clock Extension Peripheral Interface (CXPI) protocol.

1.2 Overview

This document describes the features and functions of the CXPI protocol. The CXPI protocol provides some selected features of the Controller Area Network (CAN) protocol implemented on a UART-based data link for mainly HMI (Human Machine Interface) of road vehicles electric systems.

1.3 Relationship to JASO D015 CXPI Specification

This information report is a description of the CXPI protocol, which is specified in the JASO D015 CXPI document published by JASO. The JASO D015 CXPI specification is the normative reference for the CXPI protocol. The CXPI specification is maintained by JSAE (Society of Automotive Engineers of Japan, Inc.).

This information report does not supersede any information contained in the JASO D015 CXPI specification. It has the sole purpose of providing textual description and graphical illustrations to ease reading and interpretation of the CXPI protocol.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of SAE publications shall apply.

2.1.1 SAE Documents

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or +1 724-776-4970 (outside USA), www.sae.org.

SAE J2602/1 LIN Network for Vehicle Applications

SAE J2602/2 LIN Network for Vehicle Applications Conformance Test

SAE J2602/3 File Structures for a Node Capability File (NCF)

2.1.2 ISO Documents

Copies of these documents are available online at <http://webstore.ansi.org/>

ISO 11898-1 Road Vehicles — Controller Area Network (CAN) — Part 1: Data Link Layer and Physical Signaling

ISO 14230 Road Vehicles — Diagnostic Communication over K-Line (DoK-Line)

ISO 17987 Road Vehicles — Local Interconnect Network (LIN)

2.1.3 JASO Documents

Copies of these documents are available online at http://www.jsae.or.jp/index_e.php

JASO D015 (all parts), Automobiles — Clock Extension Peripheral Interface (CXPI)

3. DEFINITION OF TERMS

3.1 GLOSSARY

3.1.1 Controller

portion which controls processing of a data link layer

3.1.2 Inter Byte Space

time between bytes on the communication bus

3.1.3 Inter Frame Space

time between frames on the communication bus

3.1.4 Master Node

node in the system that has the function of schedule management and primary clock master

3.1.5 Clock Master

node that transmits the clock to communication bus

3.1.6 Primary Clock Master

node that becomes clock master

3.1.7 Secondary Clock Master

node that transmits the clock when primary clock master doesn't transmit the clock

3.1.8 Slave Node

each node other than master node connected within the CXPI communication system

3.1.9 Schedule

information specifying which frame is transmitted at which timing that becomes the origin of periodic transmission

3.1.10 Sequence

procedure of transmission and reception of the data among two or more nodes

3.1.11 Idle State

existence of the frame is not recognized on the communication bus. Only the clock exists, and it is possible to transmit frames

3.1.12 PTYPE Field

includes the parity bit of "1 bit" and the frame TYPE of 7 bits.

3.1.13 PID Field

includes the parity bit of "1 bit" and the frame ID of 7 bits.

3.1.14 Nominal Baud Rate

baud rate within the protocol specification range and target value of baud rate actually used

3.1.15 Operational State

Supported wakeup/sleep; in the state of normal mode, non-supported wakeup/sleep; in the state of power-on

4. ACRONYMS, ABBREVIATIONS, AND SYMBOLS

4.1 Abbreviations

AP	Application Layer
CAN	Controller Area Network
CR	Collision Resolution
CRC	Cyclic Redundancy Check
CSMA	Carrier Sense Multiple Access
CT	Counter
CXPI	Clock eXtension Peripheral Interface
DLC	Data Length Code
DLL	Data Link Layer
ECU	Electronic Control Unit
FET	Field Effect Transistor
HI	High
HMI	Human Machine Interface
IBS	Inter Byte Space
ID	Identifier
IFS	Inter Frame Space
Ind	Indicator
JSAE	Society of Automotive Engineers of Japan, Inc.
LIN	Local Interconnect Network
LO	Low
LSB	Least Significant Bit
MSB	Most Significant Bit
NRZ	Non Return to Zero
NM	Network Management

OP	Option
OSI	Open Systems Interconnection
PID	Protected ID
PL	Physical Layer
PTYPE	Protected TYPE
PWM	Pulse Width Modulation
RX	Receive (data)
RXD	RXD pin of the Transceiver
TH	Threshold
TTL	Transistor-Transistor-Logic
TX	Transmit (data)
TXD	TXD pin of the Transceiver
UART	Universal Asynchronous Receiver Transmitter

4.2 Symbols

kbit/s	Kilobit per second
$RX_{(bit)}$	Receive (bit)
T_{bit}	Nominal bit time
$TX_{(bit)}$	Transmit (bit)
V/ μ s	Voltage per microsecond

5. CXPI PROTOCOL PRINCIPLES

5.1 Features

The CXPI protocol has been defined with the objective to combine significant features of CAN onto a UART-based data link with a Carrier Sense Multiple Access (CSMA) and Collision Resolution (CR) physical layer transceiver to improve the data exchange communication between ECUs compared to typical UART-based communication e.g., RS 232, ISO 14230 K-Line, ISO 17987 Local Interconnect Network (LIN).

The following is an overview of the CXPI protocol features:

- Carrier Sense Multiple Access (CSMA): the CXPI UART transceiver performs bit level arbitration,
- Collision Resolution (CR): the CXPI UART transceiver performs bit level collision resolution (avoidance),
- Bus master clock synchronization (Pulse Width Modulation (PWM) bit representation) of all nodes on the CXPI communication bus to trigger the slave nodes communication,
- Cyclic Redundancy Check (CRC) at the end of each frame,

- Single Master and multiple Slave Node Polling Schedules,
- Polling method to support periodic schedules,
- Event method to support the responsiveness of slave node communication,
- Sleep and Wakeup support,
- Maximum baud rate of 20 kbit/s,
- Up to 16 nodes connected to a CXPI communication bus,

In addition to above feature list very small CXPI devices (nodes) may be equipped without a UART and microcontroller. Those devices can be designed to support the CXPI protocol with a Pulse Width Modulation (PWM)-based communication which is compatible with the CXPI UART-based communication.

5.2 OSI Layer Structure

The CXPI protocol is compliant to the JIS X 0026: 1995, Glossary of terms used in information processing (Open Systems Interconnection). Figure 1 shows the CXPI layer structure. The Presentation, Session, Transport and Network Layers are not part of this Information Report.

Application Layer	Frame Transfer Management Wakeup / Sleep Frame ID Assignment
Presentation Layer	Not Applicable
Session Layer	Not Applicable
Transport Layer	Not Applicable
Network Layer	Not Applicable
Data Link Layer	Management of Retransmission Transmission Processing Reception Processing
Physical Layer	Encoding, Decoding Switching Signal Encoding/Decoding Clock Synchronization Clock Output

Figure 1 - CXPI layer structure

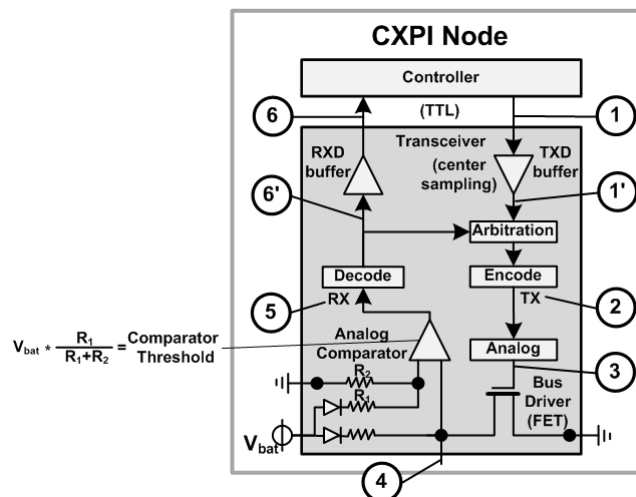
5.3 CXPI Transceiver Functionality

5.3.1 Transceiver Block Diagram and Signal References

The block diagram of the CXPI Transceiver with the signal references is used as a reference of all timing diagrams in the following chapters. Each CXPI node implements a CXPI Transceiver which consists of the following function blocks:

- (1): TXD signal from Controller: TXD buffer buffers a sending bit sent from the Controller (TTL level signal);
- Arbitration Unit: receives the sending bit from the TXD buffer and performs an arbitration (low bit wins) according to the Carrier Sense Multiple Access (CSMA) and Collision Resolution (CR) method;
- (2) TX Encode Unit: TTL signal after arbitration generated as PWM signal which will be transmitted;
- (3) TX Analog Unit with bus driver (FET): TX analog signal as input to the bus driver (FET);
- (4) CXPI bus signal: Physical analog waveform of the CXPI bus;
- (5) RX Decode Unit: TTL signal generated as output from the comparator as PWM signal;
- (6') Decoded RX signal: TTL signal generated from PWM signal as input for Arbitration Unit;
- (6) RXD signal to Controller: RXD buffer buffers the received bit (none arbitrated bits) and transmits to the Controller for software comparison with original transmitted byte;

Figure 2 shows the block diagram and signal references.



No

- 1 CXPI Node Controller TXD line which transmits bytes from the UART in TTL level
- 1' CXPI Node Transceiver TXD line which shows $\frac{1}{2} \times T_{bit}$ delay because of center sampling at (1)
- 2 Node Encoder logic which performs conversion of NRZ signal from TXD buffer to PWM signal
- 3 Node Transceiver analog circuit shapes the TTL into an analog signal
- 4 CXPI communication bus (analog signal waveform is interpreted by all connected nodes)
- 5 Actual CXPI communication bus analog RX signal waveform received by all nodes to be decoded
- 6 Controller RXD line which receives bytes from the RXD buffer in TTL level
- 6' Controller RXD line which receives bytes from the Decoder logic

Figure 2 - Block diagram and signal references

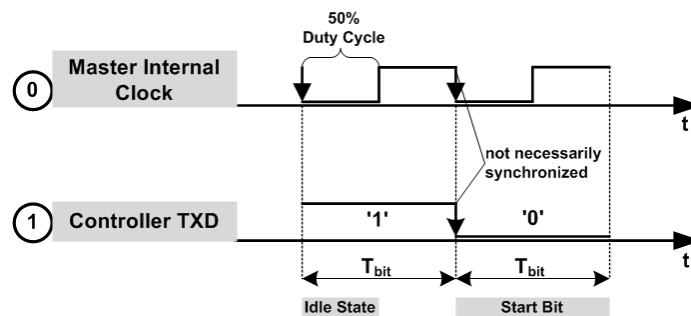
The block diagram shown in Figure 2 is common for all nodes. But there are two differences between a master and a slave node transceiver which are not illustrated in Figure 2.

- The master node transceiver operates based on the clock master (the clock supplied by a controller which is called master internal clock). On the other hand, the slave node transceiver operates based on the clock generated by detecting the falling edge of the CXPI bus signal (see RX signal (5) in Figure 2). Therefore, all slave transceivers operate synchronously, but slightly delayed from the master internal clock.
- In the master node transceiver, the TX signal (2) is generated to drive the CXPI bus for both, logic '1' and logic '0' states. In the slave node transceiver, the TX signal (2) is generated to drive the CXPI bus only when the CXPI bus is to be driven to dominant level (logic '0') to overwrap the slave signal on the CXPI bus master clock (logic '1' PWM signal generated by the master node). The reason is that only the master node outputs the bus master clock with a TXD signal (1).

5.3.2 Start Bit Falling Edge Timing

The master internal clock is generated by the master node. The master internal clock signal is a TTL signal with a 50% duty cycle (25 μ s logic '0' and 25 μ s logic '1', e.g. @20 kbps baud rate). The master internal clock triggers the bitwise transmission of the Controller transmitted frame bytes. On each falling edge of the master internal clock signal the logic state of the Controller TXD transmitted bit is started. Based on the physics of the components in the transceiver there might be a very small delay of the Controller TXD start bit timing compared to the master internal clock falling edge which is, for simplicity, not shown in the timing diagram.

Figure 3 shows the start bit falling edge timing.



No

0 CXPI Master Node Clock

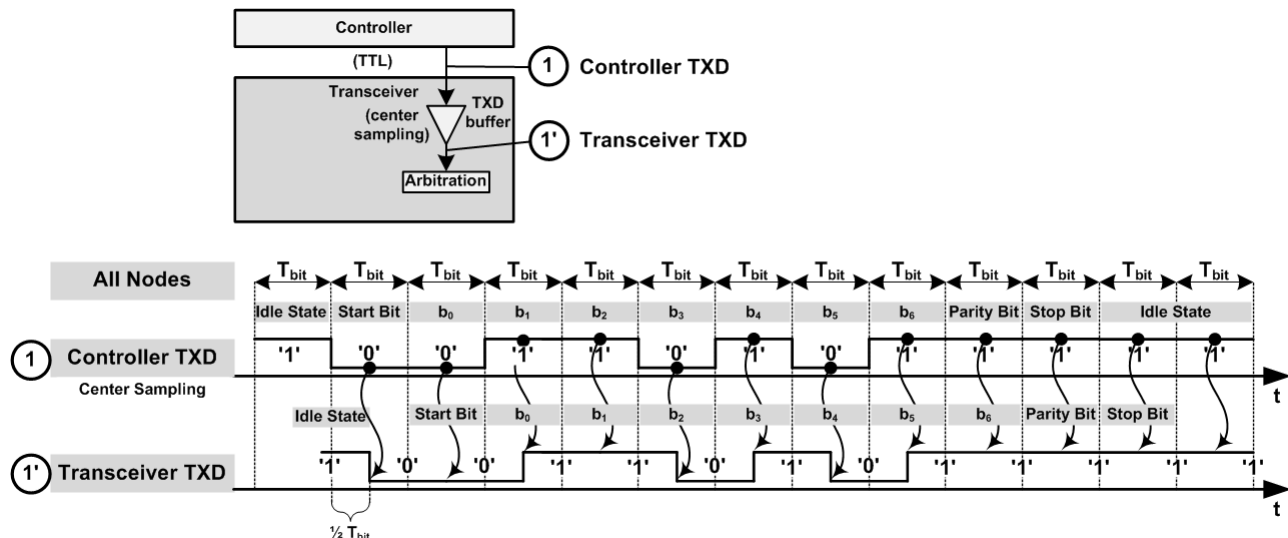
1 CXPI Node Controller TXD line which transmits bytes from the UART in TTL level

Figure 3 - Start bit falling edge timing

5.3.3 Internal TXD Signal Delay (relevant to all nodes)

The Controller TXD signal (1) is not directly connected to the Arbitration Unit but latched (sampled and hold) to become a Transceiver TXD signal (1'). The Transceiver TXD signal (1') is sampled around the center of the UART bit. Be aware of that it is not the center of the master internal clock bit. Thus the Transceiver TXD signal (1') is delayed from the Controller TXD signal (1) by $(1/2) \times T_{bit}$.

Figure 4 shows the internal TXD signal delay.



No

- 1 CXPI Node Controller TXD line which transmits bytes from the UART in TTL level
 1' CXPI Node Transceiver TXD line which shows $\frac{1}{2} \times T_{bit}$ delay because of center sampling at (1)

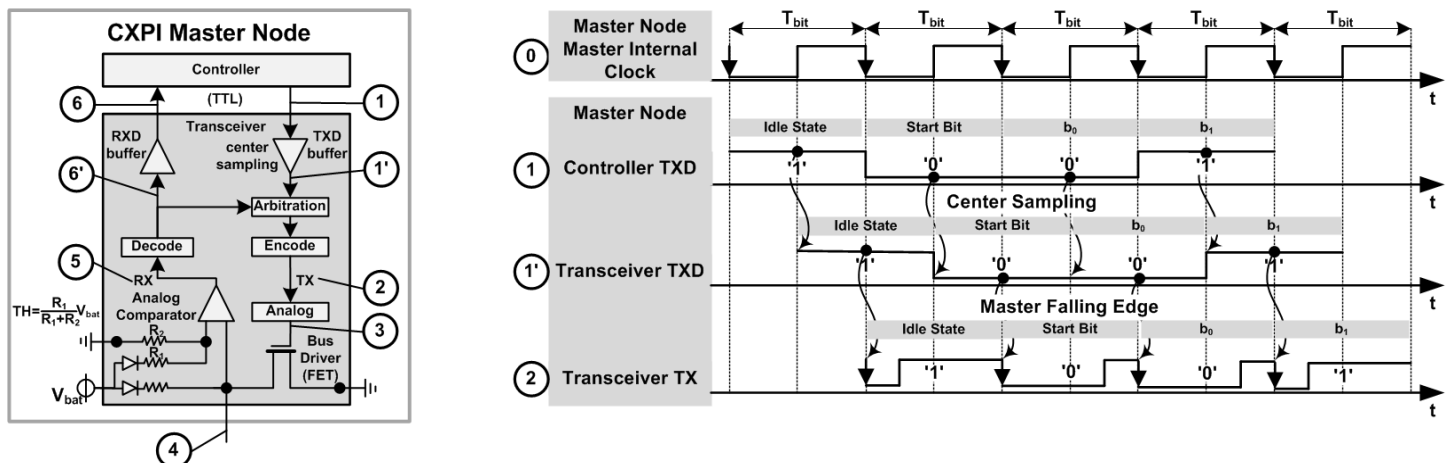
Figure 4 - Internal TXD signal delay

5.3.4 TX signal Generation

5.3.4.1 Master Node

The Transceiver TXD signal (1') bit is encoded into the Transceiver TX signal (2) at the next falling edge of the master internal clock signal after the Controller TXD signal (1) is latched. The falling edge of the Transceiver TX signal (2) is triggered by the sampling point of the Transceiver TXD signal (1') which is triggered by the falling edge of the master internal clock signal.

Figure 5 shows the internal TX signal generation (Master Node).



No

- 0 CXPI Master Node Clock
 1 CXPI Master Node Controller TXD line which transmits bytes from the UART in TTL level
 1' CXPI Master Node Transceiver TXD line which shows $\frac{1}{2} \times T_{bit}$ delay because of center sampling at (1)
 2 Master Node Encoder logic which performs conversion of NRZ signal from TXD buffer to PWM signal

Figure 5 - Internal TX signal generation (Master node)