



TECHNICAL REPORT

SSB-1.004

REV. A

Issued 1999-12
Revised 2009-04

Failure Rate Estimating

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TechAmerica Engineering Bulletin

Failure Rate Estimating

SSB-1.004-A

(Annex to SSB-1, Guidelines for Using of Plastic Encapsulated Microcircuits and Semiconductors in Military, Aerospace and Other Rugged Applications)

April 2009



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(Formulated under the cognizance of the G-12 Solid State Devices Committee.)

Published by

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Washington, DC 20004-2650
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Failure Rate Estimating

SSB-1.004

Revision	Description of change	Date
-	Initial Release	Dec 1999
A	Updated Section 4, Failure Rate Estimating Methodology, to introduce guidance on deriving failure rates when using multiple sources of data for the same failure mechanism.	Apr 2009

CONTENTS

Acknowledgments ii

1 Scope 1

2 Reference Documents 1

3 Use Condition Based Reliability Evaluation 2

4 Failure Rate Estimating Methodology 4

 4.1 Thermal Effects (HTOL Test Extrapolation)..... 7

 4.1.1 Voltage Acceleration for Microcircuits 8

 4.1.2 Voltage Derating for Discrete Semiconductor Devices 9

 4.2 Temperature-Humidity-Bias Effects (HAST Test Extrapolation)..... 10

 4.3 Thermo-mechanical Effects (Thermal Cycling Test Extrapolation) 11

 4.4 Thermal Effects for Nonvolatile Memory (NVM) Data Retention 12

 4.4.1 Data Retention Extrapolation Using the Arrhenius Life-Temperature Relationship 12

 4.4.2 Data Retention Extrapolation Using the T-Model 12

 4.5 Overall Failure Rate Summary..... 14

 4.6 Sub-System Level Analysis 14

5 Deriving Acceleration Test Parameters from Use Condition Parameters and Sub-System Failure Rate Requirements 16

 5.1 Temperature-Humidity-Bias Effects (HAST Test Extrapolation)..... 16

 5.2 Thermo-mechanical Effects (Thermal Cycling Test Extrapolation) 17

Acknowledgments

Members of Task Group G9903 of the G-12 Solid State Devices Committee developed this document. We would like to thank them for their dedication to this effort. While the principle members of the Task Groups are shown below, it is not possible to include all of those who assisted in the evolution of this Bulletin. To each of them, the members of the G-12 Solid State Devices Committee extend their gratitude.

Mr. Greg Bledsoe	Honeywell, Satellite Systems Operations
Mr. Wes Hubbell	Raytheon Systems Company, C3
Mr. Ted Krueger	General Semiconductor
Mr. Henry Livingston	Sanders, a Lockheed Martin Company

1 Scope

This document is an annex to EIA Engineering Bulletin SSB-1, *Guidelines for Using Plastic Encapsulated Microcircuits and Semiconductors in Military, Aerospace and Other Rugged Applications* (the latest revision).

Failure-Mechanism-Driven Reliability Monitoring draws upon the concepts and implementation of line controls, process stability, and effective monitoring programs in lieu of qualifying a product based solely on a fixed list of tests. A supplier must identify those failure mechanisms that may be actuated through a given product / process change(s), and must design and implement reliability tests adequate to assess the impact of those failure mechanisms on system level reliability. In order for this to be effective, the supplier establishes a thorough understanding of and linkage to their reliability monitoring program. Statistical Reliability Monitoring (SRM) is a statistically based methodology for monitoring and improving reliability; it involves identification and classification of failure mechanisms, development and use of monitors, and investigation of failure kinetics allowing prediction of failure rate at use conditions. Failure kinetics are the characteristics of failure for a given physical failure mechanism, including (where applicable) acceleration factor, derating curve, activation energy, median life, standard deviation, characteristic life, instantaneous failure rate, etc.

The failure rate of semiconductor devices is inherently low. As a result, the semiconductor industry uses a technique called accelerated testing to assess device reliability. Elevated stresses are used to produce the same failure mechanisms as would be observed under normal use conditions, but in a shorter time period. Acceleration factors are used by device manufacturers to estimate failure rates based on the results of accelerated testing. The objective of this testing is to identify these failure mechanisms and eliminate them as a cause of failure during the useful life of the product.

This document provides reference information concerning methods commonly used by the semiconductor industry to estimate failure rates from accelerated test results. These methods are frequently used by OEMs in conjunction with physics of failure reliability analysis to assess the suitability of plastic encapsulated microcircuits and semiconductors for specific end use applications.

2 Reference Documents

SSB-1.002	Environmental Tests and Associated Failure Mechanisms
SSB-1.003	Acceleration Factors

3 Use Condition Based Reliability Evaluation

The SEMATECH Reliability Technology Advisory Board (RTAB) developed a reliability evaluation methodology based on the use conditions that a component is expected to encounter in its market applications¹. Figure 1 depicts the process flow for use condition certification.

One of the most critical steps in the process is defining environmental, lifetime, and manufacturing use conditions (step I) since it provides the basis for all follow on activities that lead to establishing baseline performance (step VI). Determining the target market segment for a product establishes the use environment and lifetime that are appropriate for the technology.

It is important to note that semiconductor manufacturers derive baseline performance estimates for use conditions associated with their predominant market segment(s). Table 1, prepared by the SEMATECH RTAB, encompasses the majority of specific conditions within each major market segment. When assessing the suitability of a device for a specific application, it is essential to account for differences between the use environment and the environment the manufacturer used for reliability evaluation.

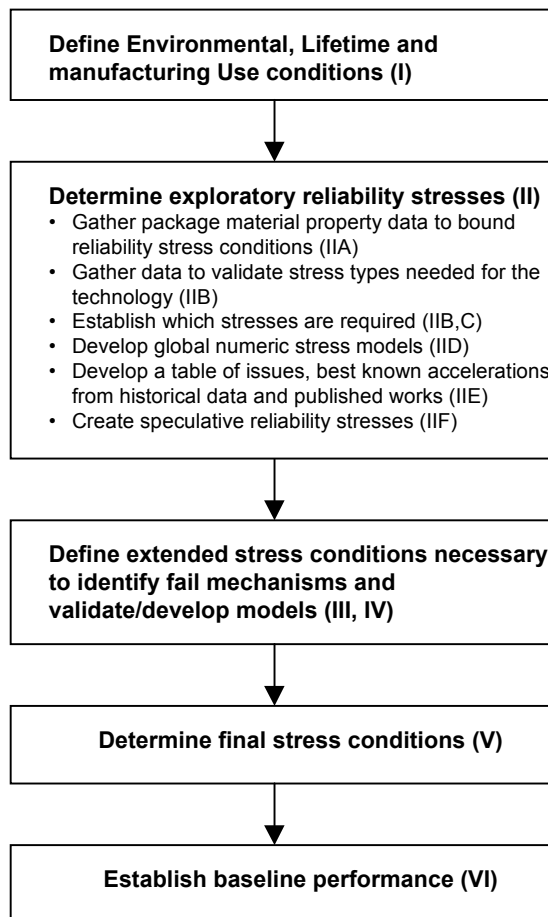


Figure 1— Process Flow for Use Condition Certification

¹ SEMATECH Technology Transfer # 99083810A-XFR: Use Condition Based Reliability Evaluation of New Semiconductor Technologies (Aug 20, 1999)