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S T A N D A R D S

Digital Video Subcommittee

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**Digital Broadband Delivery System:
Out of Band Transport Part 2: Mode B**

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Table of Contents

1.	INTRODUCTION	3
1.1	Revision History	3
1.2	Acronyms	3
1.3	References	4
2.	DAVIC OUT OF BAND AND UPSTREAM SIGNALING	5
2.1	Downstream Physical Interface Specification	6
2.1.1	Quaternary Phase Shift Keying (QPSK)	7
2.1.2	Coaxial Cable Impedance	11
2.1.3	Framing Structure	11
2.1.4	Signaling Link Extended Superframe (SL-ESF) Framing Forms	11
2.1.5	SL-ESF Frame Overhead	12
2.1.6	ESF Frame Alignment Signal	12
2.1.7	ESF Cyclic Redundancy Check	12
2.1.8	ESF M-bit Data Link	13
2.1.9	SL-ESF Frame Payload Structure	14
2.1.10	Definition of Slot Configuration Fields	17
2.1.11	ATM Cell Structure	21
2.2	Upstream Physical Interface Specification	22
2.2.1	Quaternary Phase Shift Keying (QPSK)	22
2.2.2	Coaxial Cable Impedance	26
2.2.3	Time Division Multiple Access (TDMA)	26
2.2.3.1	Slot Definition	26
2.2.3.2	Slot Definition Assignment	27
2.2.4	Contention Based Access	27
2.2.4.1	Slot Definition	28
2.2.4.2	Positive Acknowledgment	28
2.2.5	Relationship between Downstream MAC Control Channels and Upstream Channels	28
2.2.6	Slot Location and Alignment for the QPSK Upstream Channels	28
2.2.6.1	Upstream Data Rate - 1.544 Mbps/s	29
2.2.6.2	Upstream Data Rate - 256 kbit/s	29
2.2.6.3	Upstream Data Rate - 3.088 Mbps/s	30
2.3	Media Access Control Functionality	31
2.3.1	MAC Reference Model	31
2.3.2	Upstream and Downstream Channel Types	32
2.3.2.1	Downstream Out of Band Channel Requirements	32
2.3.2.2	Upstream Channel Requirements	32
2.3.3	MAC Information Transport	32
2.3.4	MAC Message Types	34
2.3.4.1	MAC Initialization, Provisioning and Sign On	34
2.3.4.1.1	Initialization and Provisioning	35
2.3.4.1.2	Sign On and Calibration	35
2.3.4.2	Connection Management	37
2.3.4.2.1	Connection Establishment	37
2.3.4.2.2	Connection Release	40
2.3.4.3	MAC Link Management	41

2.3.4.3.1	Power and Timing Management	41
2.3.4.3.2	TDMA Allocation Management	41
2.3.4.3.3	Channel Error Management	42
2.3.4.4	MAC Message Definitions	42
2.3.4.4.1	Initialization, Provisioning and Sign On Messages	42
2.3.4.4.2	Connection Management Messages	50
2.3.4.4.3	Link Management Messages	61
2.3.4.4.4	MAC message timeouts	72

Table of Figures

FIGURE 2-1	SPECTRUM ALLOCATION FOR THE BI-DIRECTIONAL PHY ON COAX	5
FIGURE 2-2	SPECTRUM ALLOCATION FOR THE INTEGRATED UNIDIRECTIONAL AND BI-DIRECTIONAL PASSBAND PHY ON A SINGLE COAX	6
FIGURE 2-3	DHCT OOB TRANSCEIVER CONCEPTUAL BLOCK DIAGRAM	6
FIGURE 2-4	QPSK DOWNSTREAM TRANSMITTER POWER SPECTRUM	8
FIGURE 2-5	SL-ESF FRAME STRUCTURE	11
FIGURE 2-6	SL-ESF PAYLOAD STRUCTURE FORMAT	15
FIGURE 2-7	CONCEPTUAL DIAGRAM OF THE CONVOLUTIONAL INTERLEAVER AND DE-LEAVER	17
FIGURE 2-8	BOUNDARY DEFINITIONS	17
FIGURE 2-9	SLOT BOUNDARY DEFINITION FIELD VALUES	18
FIGURE 2-10	ADDITIONAL SLOT BOUNDARY DEFINITION FIELD VALUES FOR EXTENDED RANGE CONTROL STATUS	19
FIGURE 2-11	RELATIONSHIP OF US SLOT TO DS INDICATOR	20
FIGURE 2-12	ATM CELL STRUCTURE	21
FIGURE 2-13	QPSK UPSTREAM TRANSMITTER POWER SPECTRUM	23
FIGURE 2-14	UPSTREAM SLOT STRUCTURE	27
FIGURE 2-15	MAC REFERENCE MODEL	31
FIGURE 2-16	INITIALIZATION AND PROVISIONING SEQUENCE	35
FIGURE 2-17	SIGN-ON MESSAGING SEQUENCE	36
FIGURE 2-18	STATE DIAGRAM FOR RANGING AND CALIBRATION	37
FIGURE 2-19	CONNECTION ESTABLISHMENT SIGNALING SEQUENCE	39
FIGURE 2-20	CONNECTION RELEASE SIGNALING	41

Table of Tables

TABLE 1-1:	ACRONYMS	3
TABLE 2-1	QPSK DOWNSTREAM TRANSMITTER POWER SPECTRUM	8
TABLE 2-2	SPECIFICATIONS FOR QPSK MODULATION (DOWNSTREAM)	9
TABLE 2-3	EXTENDED SUPERFRAME OVERHEAD STRUCTURE	12
TABLE 2-4	QPSK UPSTREAM TRANSMITTER POWER SPECTRUM	22
TABLE 2-5	SPECIFICATIONS FOR QPSK MODULATION (UPSTREAM)	23
TABLE 2-6	DAVIC MAC MESSAGES	34
TABLE 2-7	MAC MESSAGE TIMEOUTS	72

1. Introduction

1.1 Revision History

This document is identical to SCTE 55-2 2008 except for informative components which may have been updated such as the title page, NOTICE text, headers and footers. No normative changes have been made to this document.

Revision History

Revision	Date	Editor	DESCRIPTION
0.0	June 26, 1998		QPSK Out of Band Channels based on DAVIC, first draft
1.0	September 9, 1999	J. Bagley	Changed typo of DAVIC 1.1 to DAVIC 1.2
2.0	March 10, 2000	J. Bagley	Clarification and editorial changes

1.2 Acronyms

Table 1-1 provides a definition of the acronyms used throughout this document.

Table 1-1: Acronyms

AAL	ATM Adaptation Layer	CDT	Carrier Definition Table	DS-3	Digital Signal Level 3
AAL1	ATM Adaptation Layer 1	CF	Continuous Feed	DSM-CC/DSMCC	Digital Storage Media Command and Control
AAL5	ATM Adaptation Layer 5	CFS	Continuous Feed Session	DVB-ASI	Digital Video Broadcasting Asynchronous Serial Interface
ACK	Acknowledge	CM	Configuration Management	DVB	Digital Video Broadcasting (European)
ACS	Access Control and Security	CMB	CRC Message Block	DVSG	Digital Video Software Group
AG	Administrative Gateway	CMIP	Common Management Information Protocol	EA	Entitlement Agent (PowerKEY)
AHE	Analog Headend	CMIS	Common Management Information Service	EAI	External Alarm Interface
AMS	Alarms Management Subsystem	CMS	Customer Management System	ECM	Entitlement Control Message
AM-VSB	Amplitude Modulation- Vestigal-Sideband	CORBA	Common Object Request Broker Architecture	EIA	Electronic Industries Association
API	Applications Programmatic Interface	CRC	Cyclical Redundancy Check	EID	Entitlement Identifier
ARP	Address Resolution Protocol	CS	Convergence Sublayer	EM	Element Manager . Generically, any control software that manages hardware elements.
ASN	Abstract Syntax Notation	CW	Control Word	EMM	Entitlement Management Message
ATM	Asynchronous Transfer Mode	DAP	Directory Access Protocol	ENT	Entitlement Name Table
ATSC	Advanced Television System Committee	DAVIC	Digital Audio Visual Council	EPG	Electronic Program Guide
BASS	Business Applications Support System	DBAPI	Database Application Programming Interface	ESBI	External Status and Billing Interface
BCS	Broadcast Control Suite	DBDS	Digital Broadband Delivery System	ESF	Extended Super Frame
BFS	Broadcast File Server	DBS	Digital Broadcast Service	EUT	Entitlement Unit Table
BM/G	Broadband Multiplexer/Gateway	DCT	Display Channel Table	FAS	Frame Alignment Signal
BMM	Broadcast Manager Module	DES	Digital Encryption Standard	FAT	Forward Applications Transport
BOOTTERM	Boot Terminal	DHCT	Digital Home Communications Terminal	FDDI	Fiber Data Distribution Interface
BOSS	Business Operations Support System	DHCTSE	Digital Home Communications Terminal Secure Element	FDM	Frequency Division Multiplexed
BPS	Bits per second	DHEI	Digital Headend Extended Interface	FEC	Forward Error Correction
CA	Conditional Access	DIS	Digital Interactive Service	FPM	Forward Purchase Messages
CAA	Conditional Access Authority (PowerKEY)	DMS	Digital Multicast Service	FTP	File Transfer Protocol
CAM	Conditional Access Manager	DMSI	Digital Multicast Service Information	GBAM	Global Broadcast Authenticated Message
CAT	Conditional Access Table	DNCS	Digital Network Control System	GOP	Group Of Pictures
CATV	Cable Television			GPS	Global Positioning System
CCM	Continues Code Management				
CDN	Cable Digital Network				

GUI	Graphical User Interface
HEC	Headend Code
HEX	Hexadecimal
HFC	Hybrid Fiber Coax
HID	Hub ID
HRC	Harmonically Related Carrier
IANA	Internet Assigned Number Authority
IBDS	Interactive Broadband Delivery System
ID	Identifier
IDL	Interface Definition Language
IETF	Internet Engineering Task Force
IGU	Integrated Gateway Unit
IP	Internet Protocol
IPA	Internet Protocol Address
IPPV	Impulse Pay Per View
IRC	Incrementally Related Carrier
ITU	International Telecommunications Union
IVSN	Interactive Video Services Network
IXC	Inter-Exchange Carrier
L1	Level 1
LAN	Local Area Network
LCR	Local Clock Reference
LCT	Logical Channel Table
LDAP	Lightweight Directory Access Protocol
LOC	Line of Code
LUG	Line Up Group
MAC	Media Access Control
Mbps	Mega-bits per second
MHz	Mega-Hertz
MIB	Management Information Base
MMDS	Multi-Megabyte Digital Service
MMT	Modulation Mode Table
MPEG	Moving Pictures Expert Group
MSK	Multi-Session Key
MUX	Multiplexer
N/A	Not Applicable
NAK	Not Acknowledged
NE	Network Element
NFS	Network File System
NI	Network Inventory
NIC	Network Information Center
NIT	Network Information Table
NMS	Network Management System
NSAP	Network Service Access Point
NTP	Network Time Protocol
NTSC	National Television System Committee
NVOD	Near Video On Demand
NVSC	Non-Volatile Storage Cell
OC-3	Optical Carrier Level 3
OMG	Object Management Group
OMS	Object Management Server
ONC	Open Network Computing
OQPSK	Offset Quadrature Phase Shift Keying
ORB	Object Request Broker
OS	Operating System
OSF	Operations System Functions
OSI	Open System Interconnect
OSS	Operations Support System
OUI	Organization Unique Identifier
PA	Physical Address
PAT	Program Association Table
PCR	Program Clock Reference

PDU	Payload Data Unit
PEN	Private Enterprise Number
PES	Packetized Elementary Stream
PID	Process ID
PIN	Personal Identification Number
PKCS	Public Key Cryptography Standards
PKYCS	Power Key Control Suite
PMT	Program Map Table
POSIX	Portable Operating System Interface Unix
POTS	Plain Old Telephone Service
PPV	Pay Per View
PRBS	Pseudo-Random Bit Stream
PS	Program Stream
PSI	Program Specific Information
PVC	Permanent Virtual Circuit
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RDBMS	Relational Database Management System
RF	Radio Frequency
RPC	Remote Procedure Call
RS	Reed-Solomon (coding)
SAR	Subassembly and Reassembly
SAR-PDU	Subassembly and Reassembly Protocol Data Unit
SET	Secure Electronic Transaction
Sev	Severity
SG	Service Gateway
SI	Service Information
SID	Session Identifier
SLIP	Serial Line Internet Protocol
SM	System Manager
SMS	Subscriber Management System
SMI	Structure of Management Information
SN	Sequence Number
SNP	Sequence Number Protection
SNMP	Simple Network Management Protocol
SNVM	Secure Non-Volatile Memory
SONET	Synchronous Optical Network
SP	Service Provider
SPE	Synchronous Payload Envelope
SRM	Session and Resource Manager
SSL	Secure Sockets Layer
STS-3c	Synchronous Transport Signal level 3 concatenation (155.552 Mbps)
SW	Software
SWIF	Single Wire Interface
TCP	Transport Control Protocol
TCP/IP	Transport Control Protocol/Internet Protocol
TDMA	Time Division Multiple Access
TED	Transition Encryption Decryption
TLI	Transport Level Interface
TMN	Telecommunications Management Network
TS	Transport Stream
UDP	User Datagram Protocol
UI	User Interface
UNISON	Uni-directional SONET
UPA	Ultra SPARC Port Architecture
UPS	Universal Power Supply
USID	Universal Service Identifier
VASP	Value-Added Service Provider
VBI	Video Blanking Interval

VCI	Virtual Circuit Indicator
VCR	Video Cassette Recorder
VCT	Virtual Channel Table
VOD	Video On Demand
VPI	Virtual Path Indicator
VSP	Video Service Provider
XDR	External Data Representation

1.3 References

Reference	Document
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ANSI/SCTE 55-2 2019

Reference	Document
1	Digital Audio Visual Council 1.3.1 Specification part 8, “Lower Layer Protocols and Physical Interfaces” as of 19978(prior to any corrigenda) NOTE: This document has become ISO-16500-4.
2	ITU-T recommendation I.361, “B-ISDN ATM Layer Specification”, November 1995
3	ITU-T recommendation I.363.5; “B-ISDN ATM Adaptation Layer specification: AAL5”, August 1996

2. DAVIC Out of Band and Upstream Signaling

The following has been extracted from the DAVIC 1.3.1 part 8 [Ref. 1] specification: Section 7.8, Passband Bi-directional PHY on coax. This does not include or track the issuance of corrigenda.

This Physical Layer Interface supports transmission over radio frequency coax (up to 1GHz bandwidth). It is referred to as the bi-directional QPSK-link on HFC (Hybrid Fiber Coax).

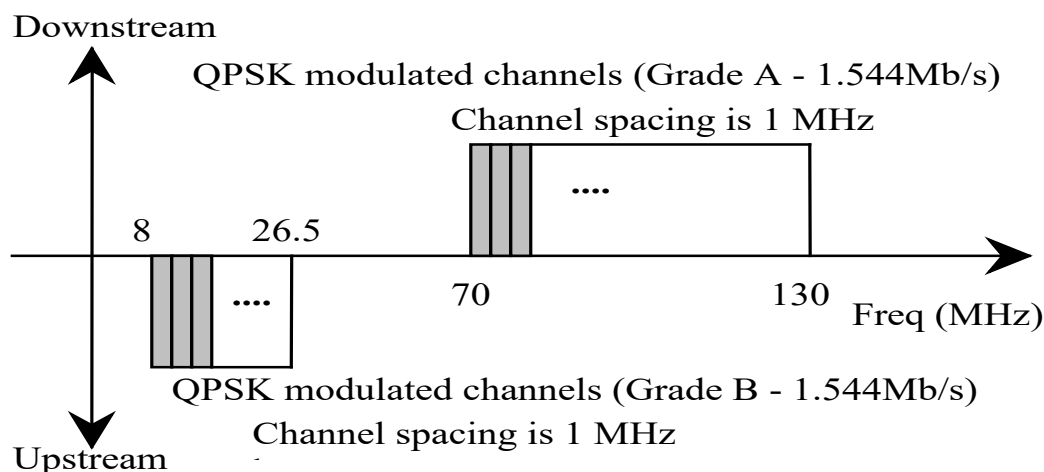


Figure 2-1 Spectrum Allocation For the Bi-directional PHY on Coax

This Physical Layer Interface describes the complete physical layer structure, i.e. framing structure, channel coding and modulation for each direction Downstream and Upstream). For the downstream QPSK modulation channel Grade A is mandatory and Grade B is optional. For the upstream QPSK channel Grade B is mandatory and Grades A and C are optional.

A summary of the spectrum allocation is depicted in

The Passband Bi-directional **PHY** on coax and the Passband Unidirectional **PHY** on coax may be used together on the same physical medium. Figure 2-2 shows the spectrum allocation in this case.

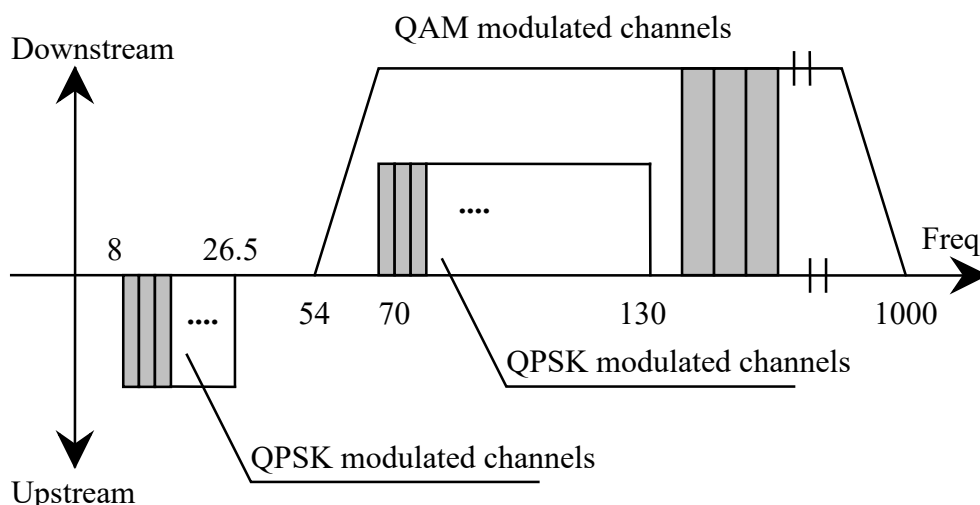


Figure 2-2 Spectrum allocation for the integrated unidirectional and bi-directional passband PHY on a single coax.

†

Conceptual block diagrams of the DHCT transceivers are shown in Figure 2-3 .

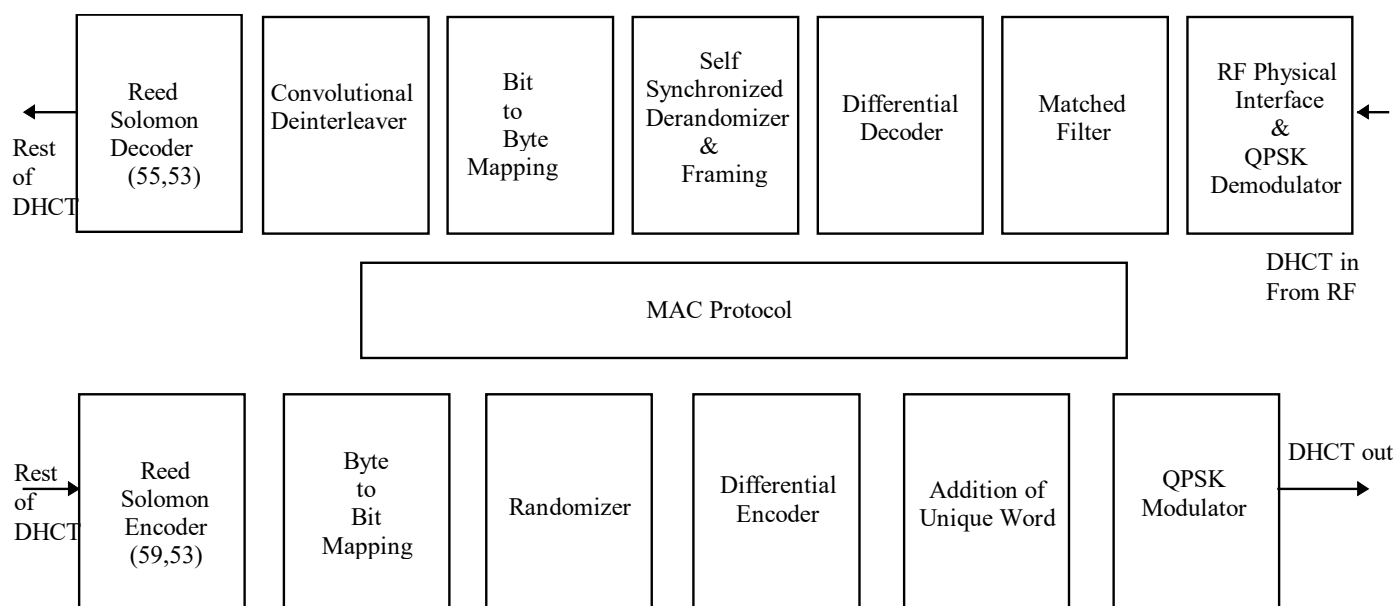


Figure 2-3 DHCT OOB Transceiver Conceptual Block Diagram

2.1 Downstream Physical Interface Specification

To carry downstream information a combination of quaternary phase shift keying (QPSK) and a framing structure are specified. QPSK is specified due to its increased error performance, its spectral efficiency, and its low peak to average power allow transmission at a high average power. The DAVIC specified Grade A QPSK is mandatory with Grade B being optional.

2.1.1 Quaternary Phase Shift Keying (QPSK)

QPSK modulation is used as a means of encoding digital information over wireline or fiber transmission links. The method is a subset of Phase Shift Keying (PSK) which is a subset of Phase Modulation (PM). Specifically QPSK is a four level use of digital phase modulation (PM). Quadrature signal representations involve expressing an arbitrary phase sinusoidal waveform as a linear combination of a cosine wave and a sine wave with zero starting phases.

The time-domain response of a square-root raised-cosine pulse with excess bandwidth parameter α is given by:

$$g(t) = \frac{\sin\left[\frac{\pi t}{T}(1 - \alpha)\right] + \frac{4\alpha t}{T} \cos\left[\frac{\pi t}{T}(1 + \alpha)\right]}{\frac{\pi t}{T} \left[1 - \left(\frac{4\alpha t}{T}\right)^2\right]}$$

where T is the symbol period.

The output signal shall be defined as

$$S(t) = \sum_n [I_n \cdot g(t - nT) \cdot \cos(2\pi f_c t) - Q_n \cdot g(t - nT) \cdot \sin(2\pi f_c t)]$$

with I_n and Q_n equal to ± 1 , independently from each other, and f_c the QPSK modulator's carrier frequency.

The QPSK modulator divides the incoming bit stream so that bits are sent alternately to the in-phase modulator I and the out-of-phase modulator Q. These same bit streams appear at the output of the respective phase detectors in the demodulator where they are interleaved back into a serial bit stream.

The QPSK signal parameters are:

RF bandwidth $BW = (f_b / 2) * (1 + \alpha)$

Occupied RF Spectrum $[f_c - BW/2, f_c + BW/2]$

Symbol Rate $f_s = f_b / 2$

Nyquist Frequency $f_N = f_s / 2$

with f_b = bit rate, f_c = carrier frequency and α = excess bandwidth.

For both bit rates: 1.544 Mbps/s (Grade A) and 3.088 Mbps/s (Grade B), the Power Spectrum at the QPSK transmitter shall comply to the Power Spectrum Mask given in Table 2-1 and

Figure 2-4. The Power Spectrum Mask shall be applied symmetrically around the carrier frequency.

Table 2-1 QPSK Downstream Transmitter Power Spectrum

$ (f - f_c) / f_N $	Power Spectrum
$\leq 1 - \alpha$	0 ± 0.25 dB
at 1	-3 ± 0.25 dB
at $1 + \alpha$	≤ -21 dB
≥ 2	≤ -40 dB

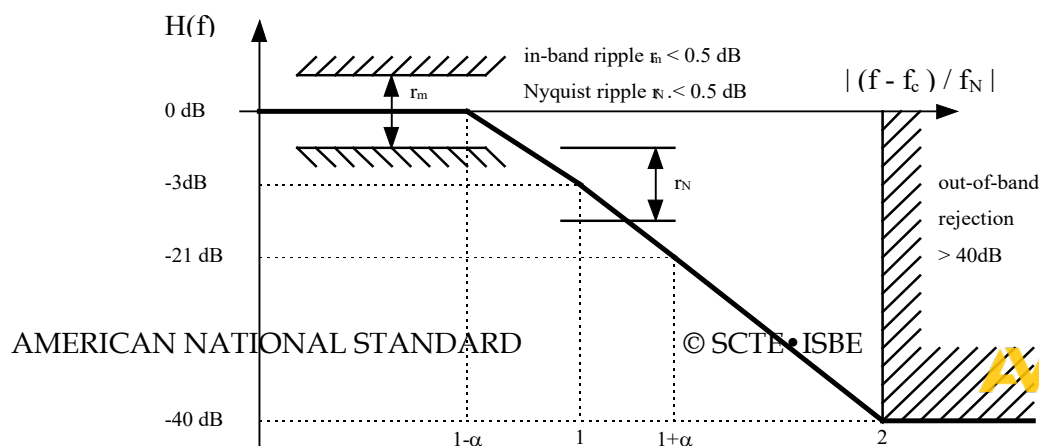


Figure 2-4 QPSK Downstream Transmitter Power Spectrum

QPSK systems require the use of differential encoding and corresponding differential detection. This is a result of the receivers having no method of determining if a recovered reference is a sine reference or a cosine reference. In addition, the polarity of the recovered reference is uncertain.

Differential encoding transmits the information in encoded phase differences between the two successive signals. The modulator processes the digital binary symbols to achieve differential encoding and then transmits the absolute phases. The differential encoding is implemented at the digital level.

The implementation of the QPSK (de)modulator shall comply to the specifications given in Table 2-2 Table 2-2 Specifications for QPSK Modulation (Downstream)

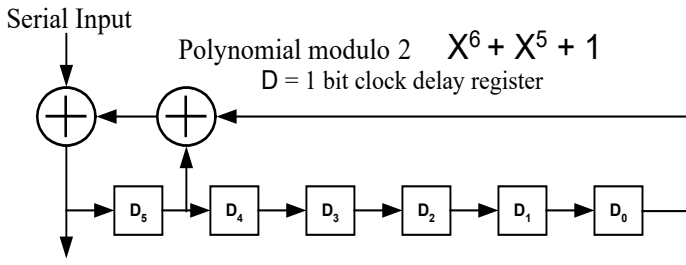
Table 2-2	Specifications for QPSK Modulation (Downstream)
Transmission Rate	1.544 Mbps/s for Grade A 3.088 Mbps/s for Grade B A QPSK demodulator shall support Grade A (B is optional)
Modulation	Differentially encoded QPSK.
Transmit Filtering	Filtering is $\alpha = 0.30$ square root raised cosine
Channel Spacing	1 MHz for Grade A 2 MHz for Grade B
Frequency Step Size	250 kHz (center frequency granularity)
Randomization	After addition of the FEC bytes, MSB first byte to serial conversion is performed and then, all of the 1.544 Mbps/s or 3.088 Mbps/s data is passed through a six register linear feedback shift register (LFSR) randomizer to ensure a random distribution of ones and zeroes. The generating polynomial is: $x^6 + x^5 + 1$. Randomizer:  A complementary self-synchronizing derandomizer is used in the receiver to recover the data. Derandomizer:

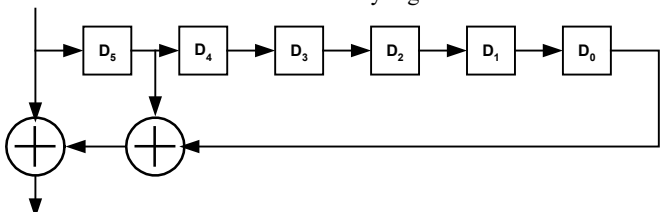
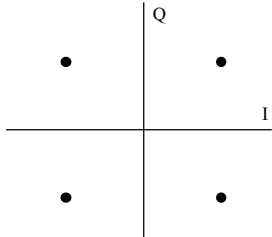
Table 2-2	Specifications for QPSK Modulation (Downstream)															
	Serial Input D = 1 bit clock delay register  Serial Output															
Differential Encoding	Bytes entering the byte-to-symbol encoder are divided into four bit pairs, each bit pair generating one QPSK symbol. Byte boundaries coincide with bit pair boundaries: that is, no bit pairs overlap two bytes. The bit pair corresponding to the MSBs of the byte is sent first. Within each bit pair, the more significant bit is referred to a ‘A’ and the less significant as ‘B’. The differential encoder shall accept bits(A,B) in sequence, and generate phase changes as follows: <table><tr><td><u>A</u></td><td><u>B</u></td><td><u>Phase Change</u></td></tr><tr><td>0</td><td>0</td><td>none</td></tr><tr><td>0</td><td>1</td><td>+ 90 degrees</td></tr><tr><td>1</td><td>1</td><td>180 degrees</td></tr><tr><td>1</td><td>0</td><td>- 90 degrees</td></tr></table> Initialization: The differential encoder state at the start of the payload (equivalent to at the end of the preamble) must be [I,Q]=[01].	<u>A</u>	<u>B</u>	<u>Phase Change</u>	0	0	none	0	1	+ 90 degrees	1	1	180 degrees	1	0	- 90 degrees
<u>A</u>	<u>B</u>	<u>Phase Change</u>														
0	0	none														
0	1	+ 90 degrees														
1	1	180 degrees														
1	0	- 90 degrees														
Signal Constellation	The outputs I, Q from the differential encoder map to the phase states as follows: 															
Carrier Center Frequency Range	70 to 130 MHz. The receiver shall operate over the entire specified frequency range.															
Frequency Stability	+/- 50 ppm measured at the upper limit of the frequency range															
Symbol Rate Accuracy	+/- 50 ppm															
Transmitter Power Spectrum Mask	A common mask for both bit rates: 1.544 Mbps/s (Grade A) and 3.088 Mbps/s (Grade B) is given in Table 2-1															
Carrier Suppression	> 30 dB															
I/Q Amplitude Imbalance	< 1.0 dB															
I/Q Phase Imbalance	< 2.0 degree															
Receive Power Level at the demodulator input (downstream	42 - 75 dBmicroV (RMS) (75 Ohm)															

Table 2-2	Specifications for QPSK Modulation (Downstream)
out-of-band)	
C/N at the DHCT input (Nyquist bandwidth, white noise)	≥ 20 dB for BER $< 1 \times 10^{-10}$ (after R/S error correction) (i.e. 1 error in 2 hours at 1.5 Mbps/s) > 18 dB for BER $< 1 \times 10^{-6}$ before R/S error correction

2.1.2 Coaxial Cable Impedance

The coaxial cable nominal impedance shall be 75 Ohm over the frequency range as specified in.

2.1.3 Framing Structure

The framing organization shall be based on Signaling Link Extended Superframe (SL-ESF) format, an SL-ESF payload structure, and an ATM cell structure.

2.1.4 Signaling Link Extended Superframe (SL-ESF) Framing Forms

The Signaling Link Extended Superframe (SL-ESF) frame structure is illustrated in . The bitstream is partitioned into 4632 bit Extended Superframes. Each Extended Superframe consists of 24 193-bit frames. Each frame consists of 1 overhead (OH) bit and 24 bytes (192 bits) of payload.

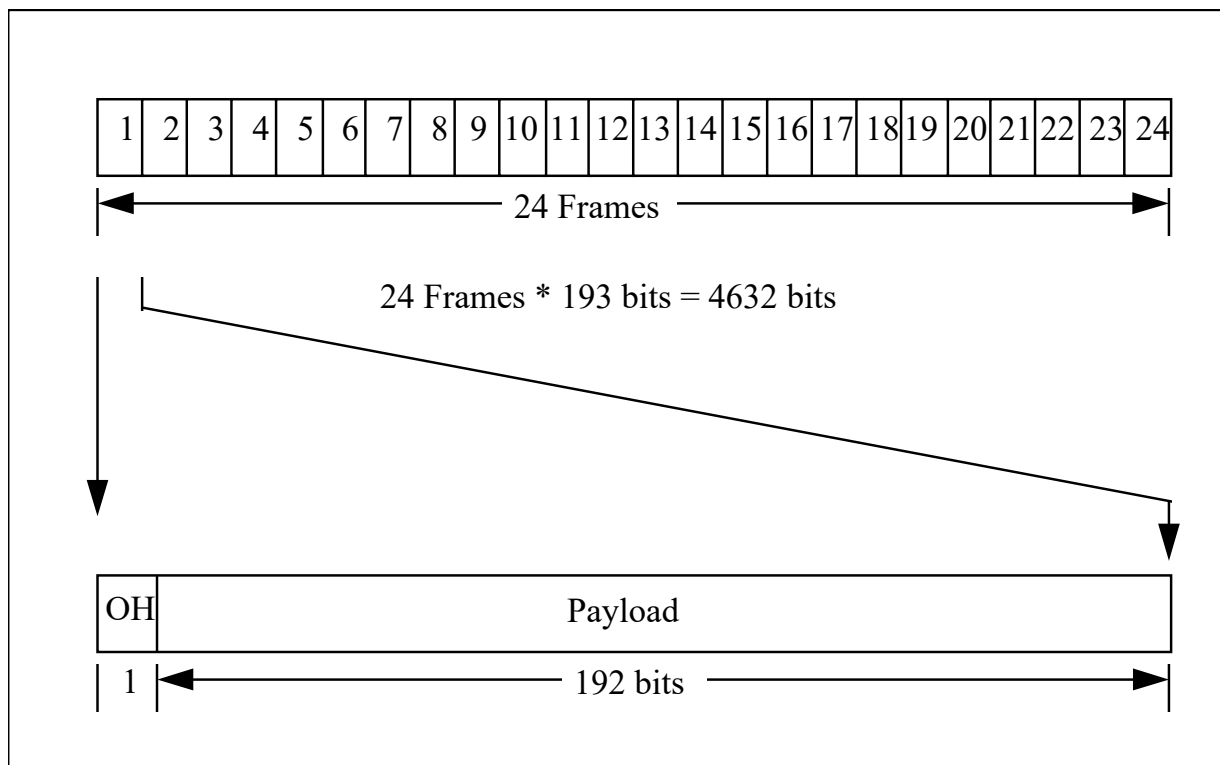


Figure 2-5 SL-ESF Frame Structure**2.1.5 SL-ESF Frame Overhead**

There are 24 frame overhead bits in the Extended Superframe which are divided into Extended Superframe Frame Alignment Signal (F1-F6), Cyclic Redundancy Check (C1-C6), and M-bit Data Link (M1-M12), as illustrated in Table 2-3.

Table 2-3 Extended Superframe Overhead Structure

Frame Number	Bit Number	Overhead Bit	Data (192 bits)	
1	0	M1		♦ SlotPosition
2	193	C1		
3	386	M2		
4	579	F1 = 0		
5	772	M3		
6	965	C2		
7	1158	M4		
8	1351	F2 = 0		
9	1544	M5		♦ SlotPosition
10	1737	C3		
11	1930	M6		
12	2123	F3 = 1		
13	2316	M7		
14	2509	C4		
15	2702	M8		
16	2895	F4 = 0		
17	3088	M9		♦ SlotPosition
18	3281	C5		
19	3474	M10		
20	3667	F5 = 1		
21	3860	M11		
22	4053	C6		
23	4246	M12		
24	4439	F6 = 1		

FAS: Frame Alignment Signal (F1 - F6)

DL: Mbps Data Link (M1 - M12)

CRC: Cyclic Redundancy Check (C1 - C6)

2.1.6 ESF Frame Alignment Signal

The ESF Frame Alignment Signal (FAS) is used to locate all 24 frames and overhead bit positions. The bit values of the FAS are defined as follows:

F1 = 0, F2 = 0, F3 = 1, F4 = 0, F5 = 1, F6 = 1.

2.1.7 ESF Cyclic Redundancy Check

The Cyclic Redundancy Check field (Table 2-3) contains the CRC-6 check bits calculated over the previous Extended Superframe (CRC Message block [CMB] size = 4632 bits). Before calculation, all 24 frame overhead bits are equated to the value “1”. All information in the other bit positions is unchanged. The check bit sequence C1-C6 is the remainder after multiplication by x^6 and then division by the generator polynomial x^6+x+1 of the CMB. C1 is the most significant bit of the remainder. The initial remainder value is preset to all zeros.

2.1.8 ESF M-bit Data Link

The M-bits in the SL-ESF serve two purposes:

- to mark the slot positions for the upstream Contention based and Contentionless based signaling links
- to provide slot count information for upstream message bandwidth allocation management in the DHCT.

M-bits M1, M5, and M9 mark the start of an upstream slot position for upstream message transmission.

Think of M-bits M10 - M1 as a register, which counts from 0 to N, where N is an integer which indicates slot position cycle size (the value of N is sent in the MAC Default Configuration Message as Service_Channel_Last_Slot). The upstream slot position register indicates the upstream slot positions that will correspond to the next SL-ESF frame. Upstream slot positions are counted from 0 to N. There are 3 upstream slots per upstream slot position when the upstream data rate is 1.544 Mbps/s, there are 6 upstream slots per upstream slot position when the upstream data rate is 3.088 Mbps/s, and there is 0.5 upstream slot per upstream slot position when the upstream data rate is 256 kbit/s. The corresponding upstream slot rates are, therefore, 3000 upstream slots/sec when the upstream data rate is 1.544 Mbps/s, 6000 upstream slots/sec when the upstream data rate is 3.088 Mbps/s, and 500 upstream slots/sec when the upstream data rate is 256 kbit/s. The algorithm to determine the upstream slot position counter value is given below:

```
if (downstream_rate == 3.088 Mbps/s) {n = 1;}
else {n = 0;}
```

```
upstream_slot_position_register = value of M-bits latched at bit_position M11 (M10 - M1)
```

```
if (upstream_rate==1.544 Mbps/s) { m = 3;}
else if (upstream_rate==3.088 Mbps/s) {m = 6;}
else {m = 0.5}
```

```
if ( bit_position==M1 and previous M12 ==1)
{ upstream_slot_position_counter = upstream_slot_position_register * 3 * m; }
```

```
if ( bit_position == M5)
if ( (n == 0) or (n == 1 and previous M12 == 0) )
{ upstream_slot_position_counter = upstream_slot_position_counter+m; }
```

```

if (bit_position == M9)
if ( (n = 0) or (n = 1 and previous M12 == 1) )
{ upstream_slot_position_counter = upstream_slot_position_counter + m; }

if (bit_position == M11)
{ temp_upstream_slot_position_register = (M10, M9, M8, ..., M1); }

if ( (bit_position == M12 ) and ( M12 == 1) )
{upstream_slot_position_register = temp_upstream_slot_position_register;}

```

where, the M-bits (see Table 2-3) will be defined as follows:

M1 - M10 = 10 bit ESF counter which counts from 0 to N with M10 the most significant bit (MSB);

M11 = odd parity for the ESF counter, i.e., M11 = 1 if the ESF_value (M1-M10) has an even number of bits set to 1;

M12 = 1: ESF counter valid
0: ESF counter not valid

The values assigned to M12 are as follows:

(1) When the QPSK downstream channel bit rate is 1.544 Mb/s, the M12 bit, is always set to the value '1'.

(2) When the QPSK downstream channel bit rate is 3.088 Mb/s, the information is always transmitted in pairs of superframe, where superframe-A is the first superframe in the pair, and superframe-B is the second superframe in the pair. In this case, the M12 bit of superframe-A is set to the value '0' and the M12 bit of superframe-B is set to the value '1'.

2.1.9 SL-ESF Frame Payload Structure

The SL-ESF frame payload structure provides a known container for defining the location of the ATM cells and the corresponding Reed Solomon parity values. The SL-ESF payload structure is shown in Figure 2-6

1	← 2 →		← 53 →	← 2 →		
1	R1a	R1b	ATM Cell	RS parity		
2	R1c	R2a			R2b	
3	R2c	R3a				
4	R3b	R3c			R4a	
5	R4b	R4c				
6	R5a	R5b			R5c	
7	R6a	R6b				
8	R6c	R7a			R7b	
9	R7c	R8a				
10	R8b	R8c			T	T

Figure 2-6 SL-ESF Payload Structure Format

The SL-ESF payload structure consists of 5 rows of 57 bytes each, 4 rows of 58 bytes each which includes 1 byte trailer, and 1 row of 59 bytes, which includes a 2 byte trailer. The first bit of the SL-ESF payload structure follows the M1 bit of the SL-ESF frame. The SL-ESF payload fields are defined as follows.

The two T fields shall be set to 0 to facilitate future enhancements.

Rxa-Rxc is a 24 bit field containing slot configuration information for the related upstream channel “x” and is defined as:

$$\begin{aligned} Rxa &= (b0 \dots b7) \\ Rxb &= (b8 \dots b15) \\ Rxc &= (b16 \dots b23) \end{aligned}$$

$$\begin{aligned} \text{qpsk_x_slot_configuration} &= (b0 \dots b23) \\ &= \text{slot configuration information for the upstream channel “x”} \end{aligned}$$

where

b0	= ranging control slot indicator for next 3ms period
b1-b6	= slot boundary definition field for next 3ms period
b7	= slot 1 reception indicator for second previous 3ms period
b8	= slot 2 reception indicator for second previous 3ms period
b9	= slot 3 reception indicator for second previous 3ms period
b10	= slot 4 reception indicator for second previous 3ms period
b11	= slot 5 reception indicator for second previous 3ms period
b12	= slot 6 reception indicator for second previous 3ms period
b13	= slot 7 reception indicator for second previous 3ms period
b14	= slot 8 reception indicator for second previous 3ms period
b15	= slot 9 reception indicator for second previous 3ms period
b16-17	= reservation control for next superframe
b18-b23	= CRC 6 parity (see definition in SL-ESF section)

When the upstream data channel is a 256 kbit/s data channel, then only the first three slot reception indicators are valid. These slots indicator refer to the three available slots which span over two 3ms period periods in the 256 kbit/s. When the upstream data channel is a 3.088 Mb/s data channel, two consecutive qpsk_slot_configuration fields are used. The definition of the first slot configuration field is unchanged. The definition of the second slot configuration field extends the boundary definition to upstream slots 10 through 18, and the reception indicators cover upstream slots 10 through 18.

When the Downstream MAC channel is a 3.088 Mbps/s data channel, the Slot Configuration fields in superframe-B are used when one or more 3.088 Mbps/s upstream QPSK channels are being utilized. The index for the overhead bytes in superframe-B will be R9a, R9b..., R16a, R16b, R16c.

Reed-Solomon encoding shall be performed on each ATM cell with T=1. This means that 1 erroneous byte per ATM cell can be corrected. This process adds 2 parity bytes to the ATM cell to give a codeword of (55,53).

The Reed-Solomon code shall have the following generator polynomials:

Code Generator Polynomial: $g(x) = (x + \mu^0)(x + \mu^1)$, where $\mu=02\text{hex}$

Field Generator Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$

Convolutional interleaving shall be applied to the ATM cells contained in the SL-ESF. The Rxa - Rxc bytes and the two T bytes shall not be included in the interleaving process. Convolutional interleaving is applied by interleaving 5 lines of 55 bytes.

Following the scheme of Figure 2-7, convolutional interleaving shall be applied to the error protected packets. The Convolutional interleaving process shall be based on the Forney approach, which is compatible with the Ramsey type III approach, with $I=5$. The Interleaved frame shall be composed of overlapping error protected packets and a group of 10 packets shall be delimited by the start of the SL-ESF.

The interleaver is composed of I branches, cyclically connected to the input byte-stream by the input switch. Each branch shall be a First In First Out (FIFO) shift register, with depth (M) cells (where $M = N/I$, $N = 55 =$ error protected frame length, $I =$ interleaving depth). The input and output switches shall be synchronized.

For synchronization purposes, the first byte of each error protected packet shall be always routed into the branch "0" of the interleaver (corresponding to a null delay). The third byte of the SL-ESF payload (the byte immediately following R1b) shall be aligned to the first byte of an error protected packet.

The deinterleaver is similar, in principle, to the interleaver, but the branch indexes are reversed (i.e. branch 0 corresponds to the largest delay). The deinterleaver synchronization is achieved by routing the third data byte of the SL-ESF into the "0" branch.

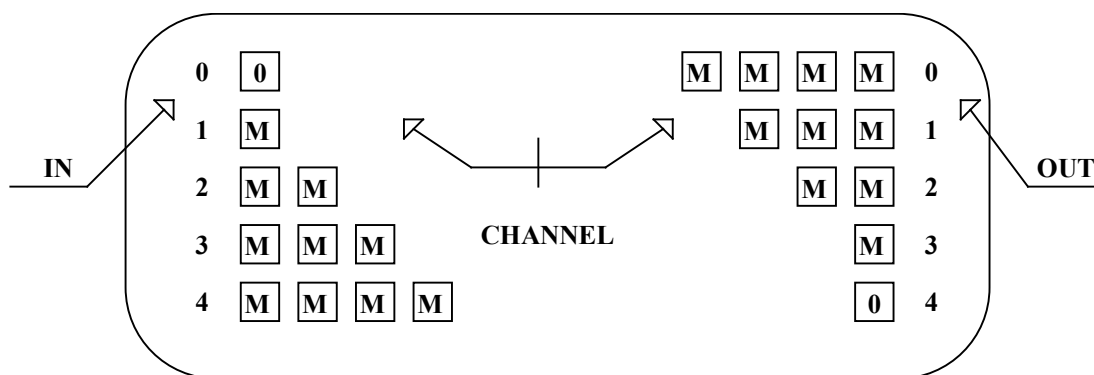


Figure 2-7 Conceptual Diagram of the Convolutional Interleaver and De-leaver

2.1.10 Definition of Slot Configuration Fields

Ranging Control Slot Indicator (b0) - When this bit is active ($b0 = 1$), the first three slots of upstream channel "x" which correspond to the occurrence of the next 3 msec period are designated as ranging control slots. A ranging control message may be transmitted in the second ranging control slot, and the first and third ranging control slots may not be used for transmission (guard band for ranging operations).

Slot Boundary Definition field (b1-b6) - Slot types are assigned to upstream slots using bits b0-b6. The slots are grouped into regions within the 3 msec period such that slots of a similar type are contained within the same region. The order of the regions is Ranging slot, Contention based slots, Reserved slots and Contentionless based slots. If a ranging slot is available within a 3 msec period it will consist of the first three slot times in the 3 msec period. A ranging slot is indicated by b0 = 1. The boundaries between the remaining regions of the 3 msec are defined by b1-b6. The boundaries are defined in Figure 2-8

Boundary 0	
Boundary 1	slot 1
Boundary 2	slot 2
Boundary 3	slot 3
Boundary 4	slot 4
Boundary 5	slot 5
Boundary 6	slot 6
Boundary 7	slot 7
Boundary 8	slot 8
Boundary 9	slot 9

Figure 2-8 Boundary Definitions

The boundary positions are defined by b1-b6 in Figure 2.9.,

row = Contention based/Reserved region boundary

column = Reserved packet/Contentionless based region boundary

(example : b0=0, b1-b6=22: Contention (1-2), Reserved (3-5), Contentionless (6-9))

	0	1	2	3	4	5	6	7	8	9
0*	0	1	2	3	4	5	6	7	8	9
1*		10	11	12	13	14	15	16	17	18
2*			19	20	21	22	23	24	25	26
3				27	28	29	30	31	32	33
4					34	35	36	37	38	39
5						40	41	42	43	44
6							45	46	47	48
7								49	50	51
8									52	53
9										54

(*) note: When the ranging control slot indicator (b0) is set to “1”, the values in rows 0 - 2 are illegal values, and values in row 3 means that there are no aloha slots, because slots 1-3 are defined as ranging control slots.

Figure 2-9 Slot Boundary Definition Field Values

The remaining values of the Slot Boundary Definition Field are provided in Figure 2-10 .

b1-b6 value	Ranging Control slots	Contention slots	reservation slots	Contentionless slots
55	1-6	7-9	-	-
56	1-6	7-8	-	9
57	1-6	7	8-9	-
58	1-6	7	8	9
59	1-6	7	-	8-9
60	1-6	-	7-8	9
61	1-6	-	7	8-9
62	1-6	-	-	7-9

Note: For b1-b6 = 55 - 63, b0 must be set to 1.

Figure 2-10 Additional Slot Boundary Definition Field Values for Extended Range Control Slots

The values in Figure 2-9 and Figure 2-10 are derived from b1-b6 in the following manner:

$$b1 + (b2 * 2) + (b3 * 4) + (b4 * 8) + (b5 * 16) + (b6 * 32)$$

When the upstream data channel is a 256 kbit/s data channel, then only the first three slot boundary positions are valid. In this case, only the first three rows and columns in Figure 2-9 are valid, and Figure 2-10 is not valid. When the upstream data channel is a 3.088 mbit/s data channel, each slot boundary definition field applies to 9 slots within the 3 msec period. In this case, there will be two slot boundary definition fields which define the 3 msec period.

Slot Reception Indicators (b7 - b15) - When a slot reception indicator is active ("1"), this indicates that a cell was received without collision. The relationship between a given US slot and its indicator is shown in Figure 2-11. When the indicator is inactive ("0"), this indicates that either a collision was detected or no cell was received in the corresponding upstream slot.

	1.544Mbit/s Downstream	3.088 Mbps/s Downstream
256 kbit/s Upstream		
1.544 Mbps/s Upstream		
3.088 Mbps/s Upstream		
Notes	1) 'I' indicates the downstream frame(s) in which Indicators (contained within the MAC Flag Sets) are sent. These indicators control the upstream slots in the shaded area. 2) In the 3.088 downstream, two successive frames contain MAC Flag Sets 0..15 1. Two successive MAC Flag Sets are used to control the 18 slots of a 3.088 upstream channel.	

Figure 2-11 Relationship of US Slot to DS Indicator

Reservation Control (b16-b17) - When the reservation control field has the value of 0, no reservation attempts are allowed to be transmitted on the corresponding QPSK upstream channel during the slot positions associated with the next 3 msec period. When the reservation