

SEMI 3D10-0814 (Reapproved 0420) GUIDE TO DESCRIBING MATERIALS PROPERTIES FOR INTERMEDIATE WAFERS FOR USE IN A 300 mm 3DS-IC WAFER STACK

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NOTICE: This Document was reapproved with minor editorial changes.

1 Purpose

1.1 This Guide is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure processed wafers to be used in a 3DS-IC process.

2 Scope

2.1 This Guide provides the tools to describe individual wafers in a 3DS-IC process. In particular, this Document provides direction for describing the dimensions, materials, and devices for wafers that have undergone processing and are entering 3D stacking process steps. Since a 3D stacking process may include wafers from multiple fabrication facilities, it is important that this information is available to ensure additional process steps are performed correctly.

2.2 This Guide describes wafers and wafer stacks with nominal diameter of 300 mm and nominal thickness of 775 μm , although the actual wafer diameter and/or thickness may differ due to 3D stacking requirements and/or the effects of prior processing steps.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This Document does not describe dimensions and procedures related to wafers and wafer stacks other than notched, 300 mm nominal diameter.

3.2 This Guide does not address issues associated with the bonding of chips to wafers; neither does it address issues associated with bonding of chips to other chips, nor does it describe interposer material.

3.3 This Document does not address issues associated with processing, bonding, or handling individual diced chips.

3.4 This Document currently does not provide recommended ordering information for glass device wafers for 3DS-IC applications, but may be added in future versions.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M59 — Terminology for Silicon Technology

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

4.2 *ANSI Standards*¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

4.3 *ASTM Standards*²

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specific Precision, the Average for a Characteristic of a Lot or Process

4.4 *JEITA Standards*³

JEITA EM-3401 — Terminology of Silicon Wafer Flatness

4.5 *JIS Standards*⁴

JIS H 0611 — Methods of Measurement of Thickness, Thickness Variation and Bow of Silicon Wafer

JIS Z 8741 — Specular Glossiness – Methods of Measurement

4.6 *MHIA Standards*⁵

CEA 556-C — Outer Shipping Container Bar Code Label Standard

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Most terms, acronyms, and symbols associated with silicon wafers and silicon technology are listed and defined in SEMI M59. Most of these terms and acronyms can be applied to wafers in a 3DS-IC process.

5.2 *Definitions*

NOTE 1: Many of these definitions are similar to, but slightly different from, those in SEMI M59. In many cases the definitions in SEMI M59 can be generalized to include 3DS-IC terms, but this is not being done at the present time.

5.2.1 *back surface* — the surface of a wafer upon which the SEMI T7 mark appears.

5.2.2 *bottom surface* — an arbitrarily defined external surface of a wafer stack.

5.2.3 *carrier wafer* — a silicon or glass wafer used for temporary bonding to another wafer.

5.2.4 *device wafer* — a silicon wafer on which devices are formed.

5.2.5 *diameter, of a 3D wafer stack* — the diameter of the minimum circle that encloses all wafers.

5.2.6 *front surface* — the surface of a wafer opposite to that with the SEMI T7 marking.

5.2.7 *intermediate wafer* — a wafer which has undergone processing and is intended for use in, or has been included in, a wafer stack.

5.2.8 *top surface* — the external surface, opposite to the Bottom Surface, of a wafer stack.

5.2.9 *wafer bond* — a process by which two or more wafers are physically attached to each other using chemical and/or thermal and/or mechanical means.

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² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>

³ Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; <http://www.jeita.or.jp>

⁴ Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: +81.3.3583.8005, Fax: +81.3.3586.2014, <http://www.jsa.or.jp>

⁵ Material Handling Industry of America (MHIA), 8720 Red Oak Blvd., Suite 201, Charlotte, NC 28217, USA; Telephone: +1.704.676.1190, Fax: +1.704.676.1199, <http://www.mhia.org>

5.2.10 *wafer bond, permanent* — a wafer bond which is intended to remain through the lifetime of the bonded layers.

5.2.11 *wafer bond, temporary* — a wafer bond which is intended to be de-bonded.

5.2.12 *wafer stack* — two or more wafers bonded to one another.

6 Intermediate Wafer for 3DS-IC Application

6.1 Because an intermediate wafer has been processed, its initial specification may no longer be accurate. The details that describe an intermediate wafer are shown in Table 1. Users of this Guide should note that a number of elements have been identified as key to the correct description of intermediate wafers for 3DS applications; these elements are indicated by a ♦ symbol in the left-most column of Table 1, Intermediate Wafer for 3D Stacked IC Application Tracking Form, Parts 1 and 2. Blocks with a ♦ symbol in the left-most column of Table 1 must be at least partially filled for this Table to be useful; however, which elements of the block are required for a specific process flow must be negotiated between the supplier and the customer.

NOTE 2: This table describes a 300 mm (nominal dimension) processed, single wafer that is in a 3D Stacked IC process flow. The wafer described in this table may be glass, silicon, or another material. Not all measurements are required at all process steps. The receiving party is expected to specify its requirements to the sending party. The terms used in this table are defined in §§ 6.2 through 6.6, below.

Table 1 Intermediate Wafer for 3D Stacked IC Application Tracking Form

Part 1: General Information – Add descriptor lines as necessary

ITEM	INFORMATION	DATE
Part Name		
Customer Name		
Purchase Order Number		
Line Number		
Item Number		
General Specification Number		
Revision Level		
Part Number/Revision		
Other _____		
Other _____		

Part 2: Intermediate Wafer Description

ITEM	SPECIFICATION	MEASUREMENT METHOD
2-1 INTERMEDIATE WAFER INFORMATION (Note that ♦ indicates a required item for which a value or choice must be indicated in order to minimally specify an intermediate wafer for 3DS-IC application.)		
♦ 2-1.1	Wafer Material ☐ Silicon ☐ Glass: (specify type) _____ ☐ Other: (specify) _____	
♦ 2-1.2	Wafer Function ☐ Interposer ☐ Carrier ☐ Device ☐ Other: (specify) _____	