

SEMI 3D14-0523

GUIDE FOR INCOMING/OUTGOING QUALITY CONTROL AND TESTING FLOW FOR 3DS-IC PRODUCTS

This Standard was technically approved by the 3D Packaging and Integration Global Technical Committee.
This edition was approved for publication by the global Audits and Reviews Subcommittee on June 30, 2022.
Available at www.semiviews.org and www.semi.org in May 2023; originally published June 2015.

1 Purpose

1.1 To ensure consistent yield control of 3DS-IC products, common criteria for incoming quality control (IQC) and outgoing quality control (OQC) of outsourced subassembly and test (OSAT) are needed. The generic testing flows for different 3DS-IC products defined in this Guide will expedite the progress of 3DS-IC testing.

2 Scope

2.1 This Guide will define the criteria for IQC and OQC of OSATs, such as appearance, discoloration, missing ball or crack to clarify the manufacturer's responsibilities and to improve product yield. This Guide will also define the generic testing flows for different 3DS-IC products, such as chip on chip (CoC), chip on substrate (CoS), chip on wafer (CoW), stacked chip on substrate (SCoS), and wafer on wafer (WoW) to help accelerate the progress of 3DS-IC testing.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This Standard does not specify details of the testing procedures.

4 Referenced Standards and Documents

4.1 None.

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Abbreviations and Acronyms

5.1.1 *CoC* — chip on chip

5.1.2 *CoS* — chip on substrate

5.1.3 *CoW* — chip on wafer

5.1.4 *IQC* — incoming quality control

5.1.5 *OQC* — outgoing quality control

5.1.6 *OSAT* — outsourced subassembly and test

5.1.7 *SCoS* — stacked chip on substrate

5.1.8 *WoW* — wafer on wafer

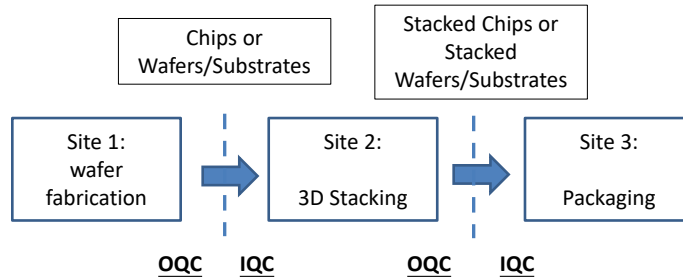
6 3DS-IC IQC and OQC

6.1 This Guide is applicable to the IQC and OQC of OSAT 3DS-IC manufacturing chains where the products, especially semi-finished goods, could be moved around among different sites. Some examples are given below and depicted in Figure 1.

6.2 After stacking, the stacked chips (i.e., CoC chips), could be sent out to an assembly house for packaging.

6.3 The wafers or substrates with chips stacked on top of them could be sent out to an assembly house for die saw and packaging.

6.4 The stacked wafers (i.e., WoW), could be sent out to an assembly house for die saw and packaging.



#1 The IQC and OQC are required in the 3DS-IC manufacturing flow, where the product is in the form of semi-finished goods and a site-to-site transfer occurs.

Figure 1
Manufacturing Flow

7 IQC

7.1 This section defines the IQC criteria of 3DS-IC products. The 3DS-IC product, either stacked chips or wafers, and the documents attached to describe this product are examined separately in the IQC process.

7.2 *Review of Attached Documents* — The items listed below would be checked from the box label, flow card, and map information which are attached with the product to ensure that the right product is received.

7.2.1 Documents checklist:

1. Device number
2. Lot number
3. Wafer pieces
4. Chip quantity
5. Wafer size
6. Mask code
7. Wafer thickness
8. Wafer identification
9. Flat/notch direction
10. Wafer type: unbond or bonded, single or double side patterned wafer (e.g., interposer)
11. Chip type: single chip or stacked chip
12. Pad material/bump/pillar: Al, Au, etc.
13. Pad structure/bump/pillar
14. Summary report including automatic optical inspection (AOI) data

7.3 *Review of Product* — The following inspections would be performed sequentially to ensure that good product is received.

7.3.1 *Visual Inspection* — Check for any scratch, chips, and breaks in the product.