

SEMI 3D15-0316 (Reapproved 1122) GUIDE FOR OVERLAY PERFORMANCE ASSESSMENT FOR 3DS-IC PROCESS

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NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

1 Purpose

1.1 This Guide will assist the user in conducting the overlay performance assessment for the face to back (F2B) and face to face (F2F) wafer in 3DS-IC process. A generic overlay performance assessment specification will be addressed in order to provide criteria and common baselines of the middle-end process for related upstream and downstream manufacturers fabricating the 3DS-IC products.

2 Scope

2.1 This Guide will provide a generic optical measurement methodology and linear dimensional parameters such as translation, expansion, rotation, residue errors and vector plots for overlay performance assessment in 3D-IC middle end process quality control. It includes generic overlay target design methodology, instrument configuration, theoretical model and measurement algorithm consideration for F2F and F2B wafer in 3D-IC process. It focuses on the various measurement methods available, rather than on particular instruments. This Guide does not provide an exhaustive list of the state of the art of overlay methodology of 3D-IC process.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This Standard does not specify details of overlay measurement procedures.

4 Referenced Standards and Documents

4.1 None.

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Abbreviations and Acronyms

5.1.1 *CMP* — chemical mechanical planarization

5.1.2 *DOF* — depth of focus

5.1.3 *F2B* — face to back

5.1.4 *F2F* — face to face

5.1.5 *TIS* — tool induced shift

5.2 Definitions

5.2.1 *centerline* — a reference line that is equidistant from opposite edges of a feature.

5.2.2 *feature* — area within a single continuous boundary that have any physical property that is distinct from the background area outside the feature. (Refer to Figure 4.)

5.2.3 *offset direction* — overlay vectors should be decomposed into orthogonal components, X and Y , along the directions of the stepper stage motion, and a rotation angle θ calculated by X and Y offset values. X Direction is positive to the right, Y Direction is positive to the up, Theta direction is positive counter clockwise, as indicated in the following figure. (Refer to Figure 3.)

5.2.4 *overlay* — a vector quantity defined at every point on the wafer. It is the difference, $\vec{O}$, between the vector position, $\vec{P}_1$, of a substrate geometry, and the vector position of the corresponding point, $\vec{P}_2$, in an overlaying pattern, which may consist of photoresist: $\vec{O} = \vec{P}_1 - \vec{P}_2$. (Refer to Figure 1.)

5.2.5 *pattern* — a group of features for overlay metrology. (Refer to Figure 4.)

5.2.6 *registration* — a vector quantity defined at every point on the wafer. It is the difference, $\vec{R}$, between the vector position, $\vec{P}_1$, of a substrate geometry, and the vector position of the corresponding point, $\vec{P}_0$, in a reference grid: $\vec{R} = \vec{P}_1 - \vec{P}_0$. (Refer to Figure 2.)

NOTE 1: Note that overlay is a relative quantity, while registration is an error compared to an absolute standard $\vec{P}_0$.

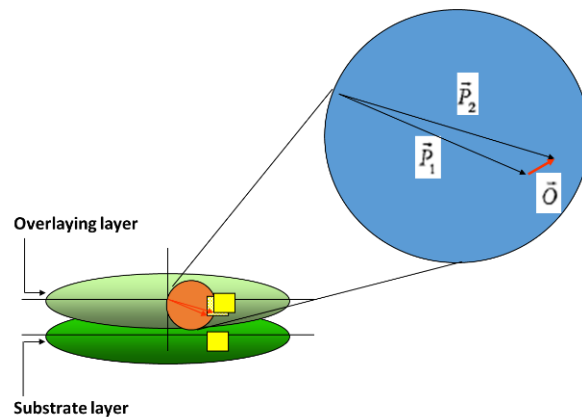


Figure 1
Schematic of Overlay Vectors

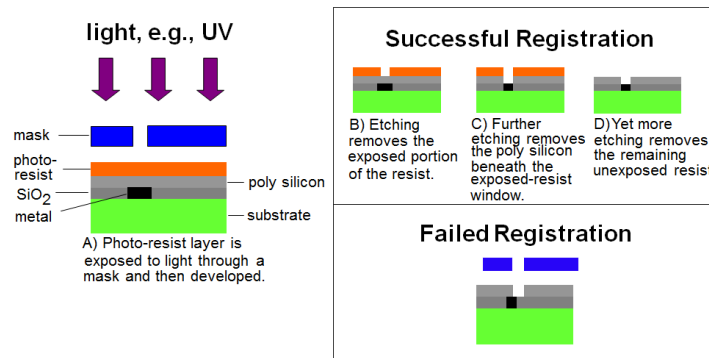


Figure 2
Schematic of Registration Processes
Left: Before Photolithography, Right: After Photolithography

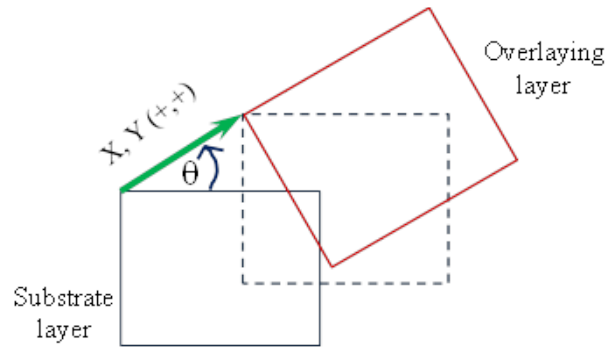


Figure 3
Overlay Vectors Definition

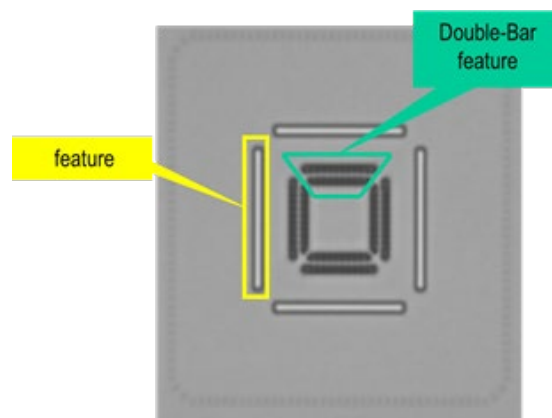


Figure 4
Features and Pattern

6 Sample and Instrumentation General Specification

6.1 Overlay Pattern Design Guideline

- The pattern should be able to represent in-circuit errors (e.g., box-based and frame-based marks).
- The pattern should be robust to process circuit damage.
- The pattern should not introduce new classes of error (e.g., large areas which will become dished during chemical mechanical planarization [CMP] operations).
- The pattern should be practical to be printed in production conditions.
- Different patterns structures should be printed at different layers of stacking wafer surfaces.
- General Methodology* — Two-Dimensional symmetrical targets are recommended. The patterns should be symmetric with respect to vertical and horizontal centerlines (90° rotational symmetry). Space must be provided between patterned line edges to avoid optical measurement interference. The designed patterns should be large enough for easy imaging by Infrared bright-field microscopy. The specific patterns can be box-in-box, frame-in-frame, or bar-in-bar. The following figures are designed examples.