

SEMI 3D16-1116

SPECIFICATION FOR GLASS BASE MATERIAL FOR SEMICONDUCTOR PACKAGING

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1 Purpose

1.1 This Specification is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure glass as base material to be used in a 3DS-IC process or in similar applications. Such glass may be specified with or without openings for through glass vias (TGV) or blind vias (BV).

2 Scope

2.1 This Specification describes dimensional and thermal characteristics of glass base material for interposers, RF devices, and other similar packaging substrates.

2.2 This Specification also applies to openings in glass.

2.3 The glass substrate is in shape of a wafer (round) or a panel (square or rectangular).

2.4 If present, the openings of the glass substrate may be intended to be further processed with metal fillings.

2.5 The glass substrate is intended to remain permanently in the package or device.

2.6 Methods of measurements suitable for determining the characteristics in this Specification are indicated.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This Document does not address issues associated with processing, bonding, or de-bonding of glass substrates.

3.2 Metal fillings, redistribution layers (RDL), and bumps are not addressed in this Document.

3.3 Manufacturing of the glass substrate and its openings are not covered by this Document.

3.4 This Document does not apply to glass substrates used as carrier wafers in a temporarily bonded state.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI 3D7 — Guide for Alignment Mark for 3DS-IC Process

SEMI 3D11 — Terminology for Through Glass Via and Blind Via in Glass Geometrical Metrology

SEMI 3D12 — Guide on Measuring Flatness and Shape of Low Stiffness Substrates

SEMI E119 — Mechanical Specification for Reduced-Pitch Front-Opening Box for Interfactory Transport of 300 mm Wafers

SEMI G90 — Specification for 300 mm Wafer Coin-Stack Type Shipping Container Used for Test and Packaging Processes

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M31 — Mechanical Specification for Front-Opening Shipping Box Used to Transport and Ship 300 mm Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M40 — Guide for Measurement of Roughness of Planar Surfaces on Polished Wafers

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M59 — Terminology for Silicon Technology

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI MS1 — Guide to Specifying Wafer-Wafer Bonding Alignment Targets

SEMI T7 — Specification for Back Surface Marking of Double-sided Polished Wafers with a Two-Dimensional Matrix Code Symbol

4.2 *ANSI Standards*¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

ANSI/OEOSC OP1.002-2009 — Optics and Electro-Optical Instruments – Optical Elements and Assemblies – Appearance Imperfections

4.3 *ASTM Standards*²

ASTM C623 — Standard Test Method for Young's Modulus, Shear Modulus, and Poisson's Ratio for Glass and Glass-Ceramics by Resonance

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specific Precision, the Average for a Characteristic of a Lot or Process

ASTM E289 — Standard Test Method for Linear Thermal Expansion of Rigid Solids with Interferometry

4.4 *ISO Standard*³

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence (TXRF) Spectroscopy

4.5 *JEITA Standard*⁴

JEITA EM-3401 — Terminology of Silicon Wafer Flatness

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² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>

³ International Organization for Standardization, ISO Central Secretariat, 1, ch. de la Voie-Creuse, CP 56, CH-1211 Geneva 20, Switzerland; Telephone: +41.22.749.01.11, Fax: +41.22.733.34.30, <http://www.iso.org>

⁴ Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; <http://www.jeita.or.jp>

4.6 JIS Standards⁵

JIS H 0611 — Methods of Measurement of Thickness, Thickness Variation and Bow of Silicon Wafer

JIS H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

4.7 MHI Standard⁶

CEA-556-C — Outer Shipping Container Bar Code Label Standard

4.8 Other Documents

International Technology Roadmap for Semiconductors, 2009 Edition, Chapter on Interconnect

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Abbreviations and Acronyms

5.1.1 *BV* — blind via

5.1.2 *FQA* — fixed quality area

5.1.3 *RDL* — redistribution layer

5.1.4 *SR* — surface roughness

5.1.5 *TGV* — through glass via

5.2 General Definitions

NOTE 1: Many of these definitions are similar to, but slightly different from, those in SEMI M59. In many cases the definitions in SEMI M59 can be generalized to include 3DS-IC terms, but this is not being done at the present time.

5.2.1 *back surface* — the surface of a wafer upon which the SEMI T7 mark appears.

5.2.2 *base material* — a material which is intended to become a substrate for further processing. For instance, in a chip, the base material may be silicon. Another example is the use of a dielectric material as a substrate for printed circuit boards.⁷

5.2.2.1 *substrate* — a surface upon which something is deposited, etched, attached, or otherwise prepared or fabricated. It can also provide physical support and insulation. The terms ‘substrate’ and ‘base material’ are often used interchangeably.

5.2.3 *diameter* — the diameter of the minimum circle that encloses the wafer.

5.2.4 *front surface* — the surface of a wafer opposite to that with the SEMI T7 marking.

5.2.5 *interposer* — a substrate that has been modified in such a way as to allow the routing of electrical signals, power and ground, enabling connections between multiple die and/or passive components, and which may subsequently be enclosed in a package or module.

5.2.6 *waist* — minimum diameter of the middle section or part of an object, especially when narrower than the rest.

5.3 Specific Definitions

5.3.1 Terms, acronyms, and symbols associated with TGV and BV technology are listed and defined in SEMI 3D11.

5.3.2 *glass base material* — glass in form of a wafer or panel, prepared for openings in glass and intended to be used permanently bonded in an application.

⁵ Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: +81.3.3583.8005, Fax: +81.3.3586.2014, <http://www.jsa.or.jp>

⁶ MHI, 8720 Red Oak Blvd., Suite 201, Charlotte, NC 28217, USA. Telephone: +1.704.676.1190; Fax: +1.704.676.1199, <http://www.mhi.org>

⁷ Electrical and Electronics Engineering Dictionary, © Wiley, Wiley-IEEE Press; 1 edition, January 22, 2004.

5.3.3 *glass carrier wafer* — a wafer used for temporarily bonding to a device wafer during one or more process steps. A carrier wafer has neither active nor passive electrical parts.

5.3.4 *glass for interposers* — glass base material with openings intended for further processing into an interposer.

5.3.5 *glass interposer* — interposer with glass as substrate.

5.3.6 *glass with openings* — glass substrate with unfilled blind or through openings (etched, laser-drilled, etc.).

5.3.7 Expansive explanations of terms used to measure the shape and flatness of low stiffness wafers or panels such as thin and large glass substrates are listed and defined in SEMI 3D12.

6 Ordering Information for Glass as Base Material Without or With Openings

6.1 The order information can be used for glass base material without or with openings.

6.2 General information required for ordering glass base material without or with openings is listed in Table 1 Part 1.

6.3 Purchase orders for glass base material furnished to this Specification shall include the items identified in Table 1 Part 2 by a ♦ symbol in the left-most column in addition to the general information in Table 1 Part 1.

6.4 Purchase orders for openings in glass for TGV and BV in glass furnished to this Specification shall include the items identified in Table 1 Part 3 by a ◇ symbol in the left-most column in addition to ¶¶ 6.1 and 6.2.

6.4.1 Shapes and dimensions of purchase orders that refer to openings in glass any other than through or BVs, must be specified separately.

6.5 The purchase order shall indicate the test method to be used in evaluating each of those items for which alternate test procedures exist.

6.6 Requirements for bulk, front, and back surface defects, such as bubbles, scratches, edge chips, and indents, and surface contamination requirements together with appropriate test methodology should be included in the purchase order.

6.7 Those specifications without ♦ or ◇ symbol should be included in the purchase order or contract but are not mandatory.

6.8 Some specifications leave optional values to be specified in the purchase order or contract. They are marked by '[] Other: _____' in the tables.

6.9 If there is no measurement method identified, customer and supplier should agree on appropriate test method if needed.

6.10 If other types of glass wafers or panels are required for an application or for research purposes, these may be ordered through the use of this Document.

6.11 The following items must also be included in the purchase order:

6.11.1 Lot acceptance procedures,

6.11.2 Certification (if required),

6.11.3 Packing and shipping container labeling requirements.

Table 1 Order Form

Part 1 General Information

<i>Item</i>		<i>Information</i>	<i>Date:</i>
1-1	Customer Name		
1-2	Purchase Order Number		
1-3	Line Number		
1-4	Item Number		
1-5	General Specification Number		

Item		Information	Date:
1-6	Revision Level		
1-7	Part Number/Revision		

Part 2 Standardized Specifications for Glass Wafers or Panels as Base Material

		Parameter	Requirement	Measurement Method
◆	2-1	Dimensions	Wafer: Diameter ☐ 200.0 mm $\pm$ 0.2 mm ☐ 200.4 mm $\pm$ 0.2 mm ☐ Other: _____ mm $\pm$ _____ mm ☐ 300.0 $\pm$ 0.2 mm ☐ 300.4 $\pm$ 0.2 mm ☐ Other: _____ mm $\pm$ _____ mm Panels: Length by Width ☐ Other: _____ mm $\pm$ _____ mm by _____ mm $\pm$ _____ mm	☐ SEMI MF2074 ☐ Other: _____
◆	2-2	ID Marking	☐ None ☐ SEMI T7 ☐ SEMI M12 ☐ Other: _____	
◆	2-3	Nominal Ground Edge Exclusion	☐ None ☐ Other: _____	
◆	2-4	Thickness	Wafers (measured as center point) ☐ 300 μm $\pm$ 5 μm ☐ 400 μm $\pm$ 5 μm ☐ 500 μm $\pm$ 5 μm ☐ 675 μm $\pm$ 5 μm ☐ 700 μm $\pm$ 5 μm ☐ Other: _____ μm $\pm$ _____ μm Panels (not measured as center point) ☐ _____ μm $\pm$ 5 μm ☐ _____ μm $\pm$ 10 μm ☐ _____ μm $\pm$ 20 μm ☐ Other: _____ μm $\pm$ _____ μm	☐ SEMI MF533 ☐ SEMI MF1530 ☐ JIS H 0611 ☐ Other: _____
◆	2-5	Total Thickness Variation (GBIR)	☐ ≤ 1 μm ☐ ≤ 2 μm ☐ ≤ 5 μm ☐ Other: _____ μm	☐ SEMI 3D12 ☐ SEMI MF533 ☐ JIS H 0611 ☐ SEMI MF657 (partial scan) ☐ SEMI MF1530 (full scan) ☐ Other: _____
	2-6	Bow	☐ ≤ 30 μm ☐ ≤ 100 μm ☐ Other: _____ μm	☐ SEMI 3D12 ☐ SEMI MF534 ☐ JIS H 0611 ☐ Other: _____