

SEMI 3D17-1217

SPECIFICATION FOR REFERENCE MATERIAL FOR BONDED WAFER STACK VOID METROLOGY

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1 Purpose

1.1 A bonded wafer reference sample of known void dimensions is needed for metrology system development and calibration. This Specification provides the details that shall be used to create such a bonded wafer reference sample and is based on 300 mm reference samples used in a SEMI round robin study and published as SEMI AUX032-0715, Round Robin Study of Method for Measurement of Voids in Bonded Pairs of Silicon Wafers.

2 Scope

2.1 This Specification describes requisite test structures, including design, manufacturing, and certification procedure for a bonded wafer reference sample composed of two wafers.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 The tools that are available to identify and measure the programmed voids after bonding that result from use of this Specification are not described in this document, but can be found in SEMI 3D13.

3.2 The potential and actual effects of bond voids on the performance and reliability of fabricated devices are not considered for this reference material specification.

3.3 The actual shape of the void trenches and the measurement technology used will affect the accuracy of the measurement(s).

3.4 This Document makes no determination of the usefulness of the test structure in a stack of more than two wafers.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI 3D13 — Guide for Measuring Voids in Bonded Wafer Stacks

SEMI M20 — Practice for Establishing a Wafer Coordinate System

4.2 Other Documents

SEMI AUX032-0715 — Round Robin Study of Method for Measurement of Voids in Bonded Pairs of Silicon Wafers

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Abbreviations and Acronyms

5.1.1 *BWP* — bonded wafer pair

5.2 Definitions

5.2.1 *cap wafer* — the top wafer of the bonded wafer pair (BWP) that is typically unpatterned (i.e., not etched). If overlay fiducials are used in the bonding process the cap wafer shall have etched fiducials.

5.2.2 *void wafer* — the bottom wafer of the bonded wafer pair (BWP) that has been etched with the specified pattern to simulate voids.

6 Reference Test Specimen

6.1 The reference test specimen consists of two wafers—a patterned Void Wafer and an unpatterned Cap Wafer—that are bonded together to form a bonded wafer pair (BWP). This reference test specimen includes die-sized arrays with sub-die regions with known void sizes and locations. The programmed bond voids are created by etching square wells in the Void Wafer of each BWP. The etched wells shall be patterned with openings ranging from $0.5\ \mu\text{m}$ to $300\ \mu\text{m}$ wide per the specified pattern, as shown in Figure 1. Three different void patterns within each sub-die shall be used: semi-dense, isolated, and dense, as shown in Figure 2. The Void Wafer shall be etched to a specified depth for the entire wafer, with recommended etch depths ranging from $4\ \text{nm}$ to $1200\ \text{nm}$, as shown in Figure 3. In each BWP, the Cap Wafer shall be unpatterned. The bonding of the wafers, typically silicon, for BWP should be done using an oxide bonding process for silicon wafers and an equivalent process for wafers of other materials.

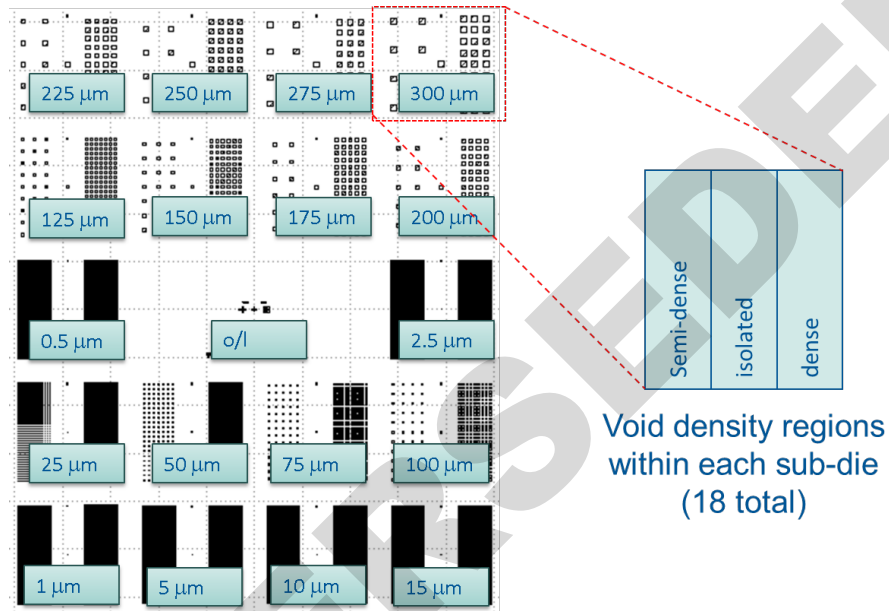


Figure 1
Layout of the Artificial Voids of Different Sizes and Densities in a Die-Sized Array

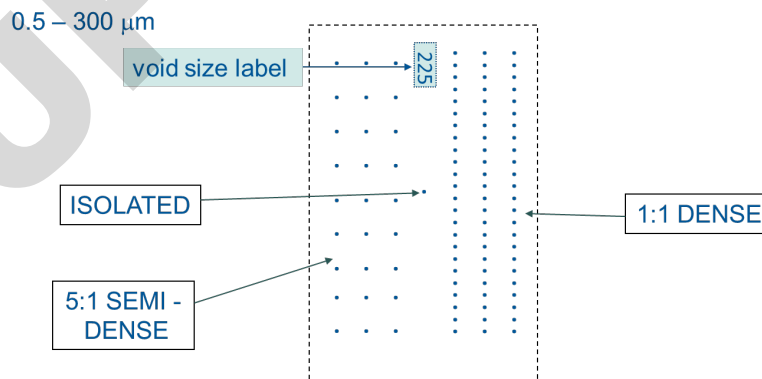


Figure 2
Details of the Arrangement of Artificial Voids at Different Densities (Not Drawn to Scale)

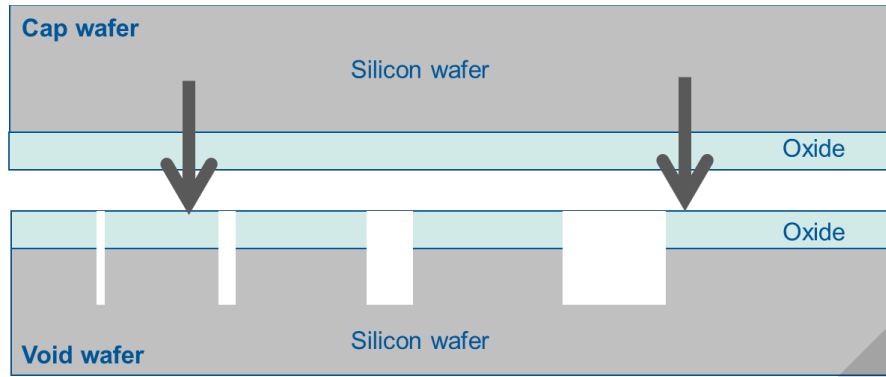


Figure 3
Schematic Diagram Showing Examples of Etched Wells Used to Produce Artificial Voids at the Bonded Interface Between Two Direct Bond Silicon Wafers

6.2 Die-Sized Arrays — Layout Description

6.2.1 As shown in Figure 1, each die-sized array consists of sub-die with void sizes from 0.5 μm to 300 μm wide per the specified pattern. The outer dimensions of each die-size array shall be 25 mm $\times$ 32 mm in the X and Y dimensions respectively. Each die-sized array may have an overlay fiducial located at its center.

6.2.2 *Sub-Die* — The sub-die for each void size consists of three different void patterns within a sub-die shall be used: semi-dense, isolated, and dense within the specified pattern, as shown in Figure 2. Each sub-die region shall also include a void size label indicating the nominal size of the voids within that region.

6.2.3 *Reference Voids* — The artificial reference voids shall be etched into the Void Wafer with the specified semi-dense, isolated and dense voids of the same size for each sub-die region, as shown in Figures 1 and 2. Each void in a sub-die region shall be etched with a square pattern with each side of the square having the same dimension in the X and Y orientations of the Void Wafer. Reference voids of the following dimensions (X and Y) shall be etched; 0.5, 1.0, 2.5, 5.0, 10.0, 15.0, 25.0, 50.0, 75.0, 100.0, 125.0, 150.0, 175.0, 200.0, 225.0, 250.0, 275.0, and 300.0 μm . The tolerance of the etched reference 100 μm void size shall be $\pm 0.1 \mu\text{m}$.

6.2.4 *Void Etch Depth* — The etch depth of the artificial reference void can be selected to help determine the sensitivity of an inspection technique to the Z dimension of a void, like is done for the X - Y dimensions. Since the nominal depth of etch is typically consistent over the entire Void Wafer it is common to select one etch of depth per wafer. The recommended etch nominal depths per Void Wafer are; 400, 200, 100 and 50 nm, based on the measured depth (Z) of the 100 μm void size in X and Y dimensions (see Note 1). The actual depth of the void shall be tracked by the Wafer ID of the Void Wafer.

6.2.4.1 The nominal etch depth shall be done by one of the following methods; Etching through the silicon dioxide (SiO_2) layer and into the silicon of the Void wafer to the desired depth (see Note 2) or building up the silicon dioxide (SiO_2) layer to a known thickness and etching through the oxide layer to the silicon (see Note 3).

- Alternative void etch depths can be utilized as needed. The nominal depth of the void etched shall be tracked by the Wafer ID of the Void Wafer.
- If void etch depths are varied for each die-array on a Void Wafer the nominal depth of the void etched shall be tracked by the Wafer ID and the Die Address (X = column # and Y = row #) of the Void Wafer.

NOTE 1: The actual thickness of artificial voids used in the original study at the nominal 40 nm voids ranged from 10 nm to 60 nm during tests run and published as SEMI 3D13 and SEMI AUX032-0715. The depth of etch shall be tracked by the Wafer ID of the Void Wafer.

NOTE 2: The actual etch depth will vary depending on the feature size being etched and the spatial uniformity of the etch tool. As a reference, the 100 μm void size in X and Y dimensions shall be used for measuring the etch depth to determine the nominal etch depth for that wafer.

NOTE 3: The thickness of a silicon dioxide (SiO_2) layer can typically be controlled to $\pm 5\%$ of the desired thickness of 500 Å to 15 μm .