

SEMI 3D18-1018

GUIDE FOR WAFER EDGE TRIMMING FOR 3DS-IC PROCESS

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1 Purpose

- 1.1 3DS-IC wafer edge trimming process is a key step for successful wafer thinning after the wafer bonded in the 3DS-IC process.
- 1.2 This Guide provides a feasible approach to perform the wafer edge trimming.
- 1.3 This Standard provides guidance for specifying edge trimming and resultant particle count to ensure the successful wafer thinning process after the wafer edge trimming.

2 Scope

- 2.1 This Standard covers guidance for specifying wafer edge trimming and resultant particle count to provide a feasible approach in edge trimming process.
- 2.2 The trimming width, depth, and resultant particle size and count are addressed in this Guide. The outcome of this applicable wafer edge trimming approach will be helpful to the subsequent wafer thinning process in the 3DS-IC process.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

- 3.1 This Standard does not specify details of wafer edge trimming procedures.

4 Referenced Standards and Documents

4.1 *SEMI Standards and Safety Guidelines*

SEMI 3D6 — Guide for CMP and Micro-Bump Processes for Frontside Through Silicon Via (TSV) Integration

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *TSV* — through silicon via

6 Guide for Specifying for Wafer Edge Trimming

- 6.1 In the 3DS-IC process, wafers would be bonded together and thinned to protrude through silicon via (TSV) or to proceed to perform the backside via last TSV process.
- 6.2 Before wafer thinning process, one critical process the wafer edge trimming process is needed to prevent the wafer edge from chipping as shown in Figure 1. Because the wafer edge trimming is such a critical process in wafer thinning process, specs for wafer edge trimming are suggested as guides for achieving a better improvement in the wafer thinning process and for enhancing the yields of 3DS-IC products.

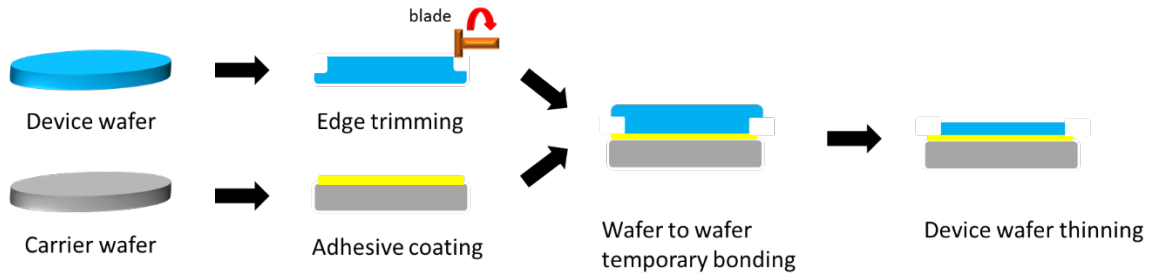


Figure 1
Brief Process Flow of Wafer Edge Trimming, Bonding and Thinning

6.3 Wafer Edge Trimming Width

6.3.1 Large wafer edge trimming width can definitely avoid the wafer edge chipping issue but waste more wafer area (i.e. increase the manufacturing cost). Small wafer edge trimming width can create more dies but has higher possibility in suffering the wafer chipping issue. Therefore, the wafer edge trimming width $0.5 \text{ mm} \pm 10\%$ (as shown in Figure 2) is suggested to have a compromise between manufacturing cost and chipping issue.



Figure 2
Wafer Edge Trimming Width

6.4 Wafer Edge Trimming Depth

6.4.1 The wafer edge trimming depth is dependent on the post-thinning wafer thickness d (i.e., the TSV depth). The deeper the TSV depth, the larger the trimming depth should be reserved. For example, a device wafer with TSVs in depth $100 \mu\text{m}$ which fabricated by via middle process, the wafer edge trimming depth can be set at $150 \mu\text{m} \pm 10\%$. In other words, the wafer edge trimming depth is set to be $d + 50 \mu\text{m}$ so that chipping is prevented and enough margins are reserved for the subsequent uniformity control in TSV protrusion and wafer thickness. The same principle is applied to the device wafers with backside via last TSV process. Although in the backside via last process, the TSV is defined after wafer thinning, this suggested wafer edge trimming depth can provide more uniform wafer thickness after thinning to reduce the TSV etching loading control.

Trimming depth = post-thinning wafer thickness
($d + 50 \mu\text{m}$) $\pm 10\%$



Figure 3
Wafer Edge Trimming Depth