SEMI 3D2-1113
SPECIFICATION FOR GLASS CARRIER WAFERS FOR 3DS-IC APPLICATIONS

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1 Purpose

1.1 This Specification is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure pristine glass carrier wafers to be used in a 3DS-IC process.

2 Scope

2.1 This Specification describes dimensional, thermal, and wafer preparation characteristics for glass starting material that will be used as carrier wafers in a temporary bonded state.

2.2 This Specification describes glass carrier wafers with nominal diameters of 200 and 300 mm, and a thickness of 700 µm, although the wafer diameter and thickness required may vary due to process and functional variation. Such variations shall be clarified in the purchasing order or in the contract.

2.3 Methods of measurements suitable for determining the characteristics in the specifications are indicated.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This Document does not describe dimensions and procedures related to wafers and wafer stacks other than notched, 200 or 300 mm nominal diameter.

3.2 This Specification does not describe interposer material and not any glass substrate for permanent bonding applications.

3.3 This Document does not address issues associated with processing, bonding, or de-bonding.

4 Referenced Standards and Documents

4.1 *SEMI Standards and Safety Guidelines*

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M59 — Terminology for Silicon Technology

SEMI MF533 — Test Method for Thickness and Thickness of Variation of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

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SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and Epi Substrates by Secondary Ion Mass Spectrometry

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T7 — Specification for Back Surface Marking of Double-sided Polished Wafers with a Two-Dimensional Matrix Code Symbol

4.2 *ANSI Standards*[1]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

ANSI 0P1.002-2009 — Optics and Electro-Optical Instruments – Optical Elements and Assemblies – Appearance Imperfections

4.3 *ASTM Standards*[2]

ASTM C623-92(2010) — Standard Test Method for Young's Modulus, Shear Modulus, and Poisson's Ratio for Glass and Glass-Ceramics by Resonance

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specific Precision, the Average for a Characteristic of a Lot or Process

4.4 *ISO Standards*[3]

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence (TXRF) Spectroscopy

4.5 *JEITA Standards*[4]

JEITA EM-3401 — Terminology of Silicon Wafer Flatness

4.6 *JIS Standards*[5]

JIS H 0604 — Measuring of Minority-carrier Lifetime in Silicon Single Crystal by Photoconductive Decay Method

JIS H 0611 — Methods of Measurement of Thickness, Thickness Variation and Bow of Silicon Wafer

JIS H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

JIS Z 8741 — Specular Glossiness – Methods of Measurement

4.7 *MHIA Standards*[6]

CEA 556-C — Outer Shipping Container Bar Code Label Standard

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Terms, acronyms, and symbols associated with silicon wafers and silicon technology are listed and defined in SEMI M59. Many of these terms and acronyms can be applied to wafers in a 3DS-IC process and to glass wafers as carriers.

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[2] ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585; Fax: 610.832.9555; http://www.astm.org

[3] International Organization for Standardization, ISO Central Secretariat, 1 rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland; Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, http://www.iso.ch

[4] Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; http://www.jeita.or.jp

[5] Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: 81.3.3583.8005, Fax: 81.3.3586.2014, http://www.jsa.or.jp

[6] Material Handling Industry of America, 8720 Red Oak Blvd., Suite 201, Charlotte, NC 28217, USA. Telephone: 704.676.1190; Fax: 704.676.1199; http://www.mhia.org

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5.2 *General Definitions*

NOTE 1: Many of these definitions are similar to, but slightly different from, those in SEMI M59. In many cases the definitions in SEMI M59 can be generalized to include 3DS-IC terms, but this is not being done at the present time.

5.2.1 *diameter* — the diameter of the minimum circle that encloses the wafer.

5.2.2 *back surface* — the surface of a wafer upon which the SEMI T7 mark appears.

5.2.3 *carrier wafer* — a glass wafer used for temporarily bonding to a device wafer during one or more process steps. Once a glass wafer remains in the package, it is considered a glass device wafer.

5.2.4 *front surface* — the surface of a wafer opposite to that with the SEMI T7 marking.

5.2.5 *wafer bond* — a process by which two or more wafers are physically attached to each other using chemical and/or thermal and/or mechanical means.

5.2.6 *wafer bond, permanent* — any wafer bond which is intended to remain through the lifetime of the bonded layers.

5.2.7 *wafer bond, temporary* — any wafer bond which is intended to be debonded.

6 Ordering Information

6.1 Purchase orders for glass carrier wafers furnished to this Specification shall include the items identified in Table 1 Part 2 by a ♦ symbol in the left-most column.

6.2 In addition, the purchase order must indicate the test method to be used in evaluating each of those items for which alternate test procedures exist.

6.3 Also, requirements for bulk, front and back surface defects, such as bubbles, scratches, edge chips and indents, and surface contamination requirements together with appropriate test methodology should be included in the purchase order.

6.4 The following items must also be included in the purchase order:

6.4.1 Lot acceptance procedures,

6.4.2 Certification (if required),

6.4.3 Packing and shipping container labeling requirements.

7 Requirements for Standardized Glass Carrier Wafers for Temporary Bonding

7.1 Standard specifications for glass carrier wafers are listed in Table 1 Part 2. All of the parameters listed in the table and marked with a diamond ♦ symbol shall be included in the purchase order or contract.

7.2 Those specifications without a ♦ symbol should be included in the purchase order or contract but are not mandatory.

7.3 Some specifications leave optional values to be specified in the purchase order or contract. Those shall be included in the purchasing order or contract if they are considered mandatory requirements as indicated by a♦ symbol.

7.4 If other types of glass wafers are required for an application or for research purposes, these may be ordered through the use of the glass carrier wafer specification order entry.

Table 1 Order Form for Glass Carrier Wafers for 3D Stacked IC Applications

Part 1 General Information

ITEM		*INFORMATION*	*Date:*
1-1	Customer Name		
1-2	Purchase Order Number		
1-3	Line Number		

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ITEM		INFORMATION	Date:
1-4	Item Number		
1-5	General Specification Number		
1-6	Revision Level		
1-7	Part Number/Revision		

Part 2 Standardized Specifications for 200 mm and 300 mm Glass Wafers for 3DS-IC Applications

		Parameter	*Grades A, B, C*			*Measurement Method*
♦	2-1.1	Glass Type	[ ] Borosilicate or [ ] Aluminosilicate			
♦	2-1.2	Manufacturing Method	[ ] Fusion, [ ] Float, or [ ] Drawn			
♦	2-1.3	Surface Condition	[ ] As-is (pristine) for fusion glass [ ] Polished for float and drawn glass			
♦	2-1.4	Nominal Ground Edge Exclusion	[ ] None [ ] Other: (specify) _____			
♦	2-1.5	Wafer ID Marking	SEMI T7 (required) + optional alphanumeric, on back surface			
♦	2-1.6	Notch Dimensions	[ ] Notch Depth: 1.00 mm +2.50 mm −0.00 mm Notch Angle: 90.0 degrees +5 deg −1 deg [ ] Other: (specify) _____			[ ] SEMI MF1152 (Notch Dimensions) [ ] Other: (specify)_____
♦	2-1.7	Edge Surface Condition	[ ] Polished			
♦	2-1.8	Edge Chamfer	[ ] 200 ± 50 µm (for 300 mm glass wafers); [ ] Other: (specify) _____±_____µm			SEMI MF928: [ ] Method A, [ ] Method B [ ]Other: (specify)_____
♦	2-2.1	Diameter	[ ] 200.0 ± 0.05 mm [ ] 200.4 ± 0.1 mm [ ] 300.0 ± 0.1 mm [ ] 300.4 ± 0.2 mm [ ] Other: (specify) _____±_____mm			[ ] SEMI MF2074 [ ] Other: (specify)_____
♦	2-2.2	Thickness, Center point	700 µm ± 5 µm [ ] Other: (specify) _____			[ ] SEMI MF533 [ ] SEMI MF1530 [ ] JIS H 0611 [ ] Other: (specify)_____
♦	2-2.3	Total Thickness Variation (GBIR)	≤1 µm	≤2 µm	≤5 µm	[ ] SEMI MF533 [ ] JIS H 0611 [ ] SEMI MF657 (partial scan) [ ] SEMI MF1530 (full scan) [ ] Other: (specify)_____
	2-2.4	Bow	≤20 µm	≤30 µm	≤100 µm	[ ] SEMI MF534 [ ] JIS H 0611 [ ] Other: (specify)_____

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