# SEMI 3D6-0913
# GUIDE FOR CMP AND MICRO-BUMP PROCESSES FOR FRONTSIDE THROUGH SILICON VIA INTEGRATION

This Standard was technically approved by the 3DS-IC Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on July 6, 2013. Available at www.semiviews.org and www.semi.org in September 2013.

## 1 Purpose

1.1 In order to speed up volume production of 3DS-IC products, a generic middle-end process flow is needed to communicate the frontend and backend processes. The quality criteria and metrology methodology of the key modules such as through silicon via (TSV), chemical mechanical planarization (CMP), and micro-bump are developed to ensure high-yield of the middle-end process. Therefore, this guide provides a generic middle-end process flow to define acceptable TSV and CMP quality criteria as well as to develop methodology and measuring procedures for micro-bump. The guide will provide criteria and common baselines of the middle-end process for related upstream and downstream manufacturers in fabricating 3DS-IC products.

## 2 Scope

2.1 This Guide proposes a frontside TSV integration scheme as one of the generic middle-end process flow. The flow includes steps such as TSV formation, RDL formation, CMP, temporary carrier bonding, wafer thinning, micro-bump formation, and carrier debonding.

2.2 This Guide define acceptable CMP criteria of TSV in terms of dishing, erosion, and voids. CMP criteria can be determined by metrology technology in both contact methods such as: micro profilometer; 4-points resistivity probes; or non-contact methods (e.g., ultrasonic scan mapping, Coherence Interferometry, or other laser-based light scattering detection schemes). TSV formation and reveal are significantly dependent on the performance of CMP process. The outcome of the high CMP quality yields better TSV connectivity.

2.3 This Guide provides criteria for measurement methodology for micro-bump dimensions, including sampling rate, sampling sites and mapping, reference datum, and survey available metrology tools. The outcome will be an important bridge communication among IC design firms, fabs, and packaging houses. The assumption of wafer-to-wafer (W2W), chip-to-wafer (C2W) and chip-to-chip (C2C) are that testing data is available for known test good die.

**NOTICE:** SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

## 3 Limitations

3.1 This Guide does not describe dimensions and procedures related to wafers and wafer stacks other than notched, 300 mm nominal diameter.

3.2 This Guide does not specify details of the process recipe.

## 4 Referenced Standards and Documents

4.1 *SEMI Standards and Safety Guidelines*

SEMI 3D1 — Terminology for Through Silicon Via Geometrical Metrology

SEMI M59 — Terminology for Silicon Technology

4.2 *JEDEC Standards*[1]

JEP158 — 3D Chip Stack with Through-Silicon Vias (TSVS): Identifying, Understanding and Evaluating Reliability Interactions

[1] Joint Electron Device Engineering Council, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201, USA; Telephone: +1.703.907.7560, Fax: +1.703.907.7583, http://www.jedec.org



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**NOTICE:** Unless otherwise indicated, all documents cited shall be the latest published versions.

## 5 Terminology

NOTE 1: Terms, acronyms, and symbols associated with silicon wafers and silicon technology are listed and defined in SEMI M59 as well as the SEMI Standards Compilation of Terms. Most of these terms and acronyms can be applied to wafers in a 3DS-IC process.

5.1 *Abbreviations and Acronyms*

5.1.1 *BUB* — backside micro-bump

5.1.2 *BVR* — backside via reveal

5.1.3 *EDP* — end-point

5.1.4 *FIC* — frontside interconnect contact

5.1.5 *FRDL* — frontside redistribution layer

5.1.6 *FUB* — frontside micro-bump

5.1.7 *MEOL* — middle end of line

5.1.8 *NU* — non-uniformity

5.1.9 *PR* — photo resist

5.1.10 *Ra* — surface roughness

5.1.11 *Rmax* — max surface roughness variation

5.1.12 *RDL* — redistribution layer

5.1.13 *THK* — thickness

5.1.14 *TTV* — total thickness variation

5.1.15 *UB* — micro bump

5.1.16 *WAT* — wafer acceptance test

## 6 Generic Process Flow for Frontside TSV Formation

6.1 *Process Overview*

Dielectric layers done in the backend-of-line process

Dielectric layers done in this generic process

Cu interconnects done in the backend-of-line

Si

Cu layers done in this generic

Frontside micro-bump

Adhesive

Carrier

Backside micro-bump

Tape

6.1.1 The following figures and descriptions from (a) to (s) are generic frontside via last TSV process steps used for developing CMP and micro bumps criteria.

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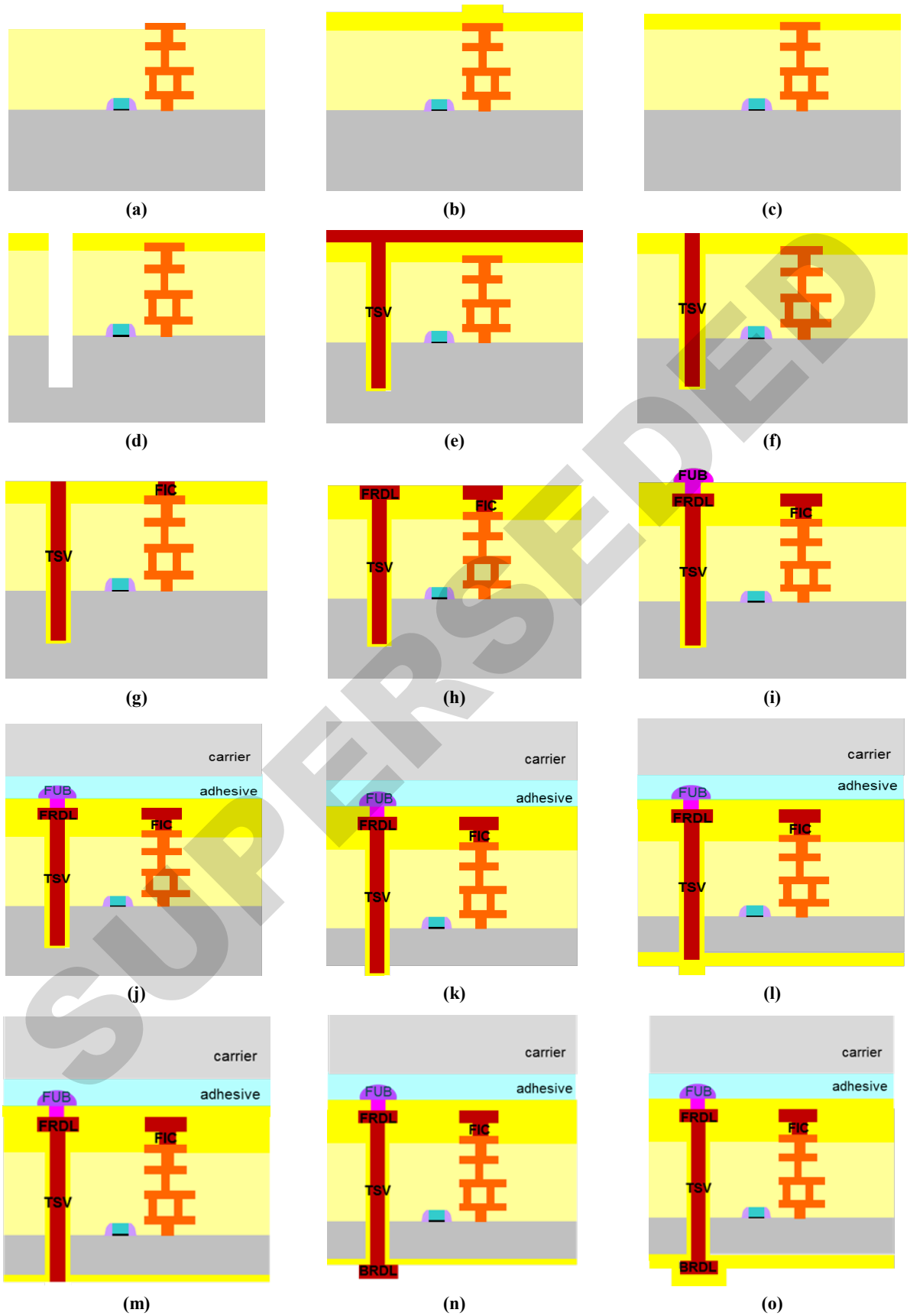


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