

SEMI 3D7-0913 (Reapproved 0219) GUIDE FOR ALIGNMENT MARK FOR 3DS-IC PROCESS

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1 Purpose

1.1 Photo alignment mark configuration is the key to ensure consistent and precise alignment of layers, chips and wafers. Therefore, this Guide provides the alignment mark strategy for chip to chip, chip to wafer, and wafer to wafer stacking. This Guide also addresses the universal alignment mark where the outcome will be a feasible photo alignment standard.

2 Scope

2.1 Define and develop lithography alignment strategy for C2C, C2W and W2W stacking. The alignment mark is preferable to be implemented at frontside final metal and/or backside metal layer masking. This Guide addresses universal alignment mark, including shape, dimension, and location. The outcome of a feasible photo alignment standard will be critical to the C2C, C2W and W2W stacking.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This Guide does not provide details of the alignment procedures.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI MS1 — Guide to Specifying Wafer-Wafer Bonding Alignment Targets

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Abbreviations and Acronyms

5.1.1 C2C — chip to chip

5.1.2 C2W — chip to wafer

5.1.3 W2W — wafer to wafer

6 Alignment Mark Specifications for C2C, C2W, and W2W Stacking

6.1 C2C Alignment Mark Specifications

6.1.1 The C2C alignment marks (blue color as shown in Figure 1) with shapes in square and diamond as a reference are put in the three corners of a die. The two square alignment marks on the same diagonal line should be identical in

shape and dimension. The third alignment mark on another diagonal line should be different in shape. The center of each alignment mark should lie in the diagonal lines (XX' and WW') of the die to ensure the precise stacking of different dies. The C2C alignment marks also called the local alignment marks are put within dies for C2C stacking.

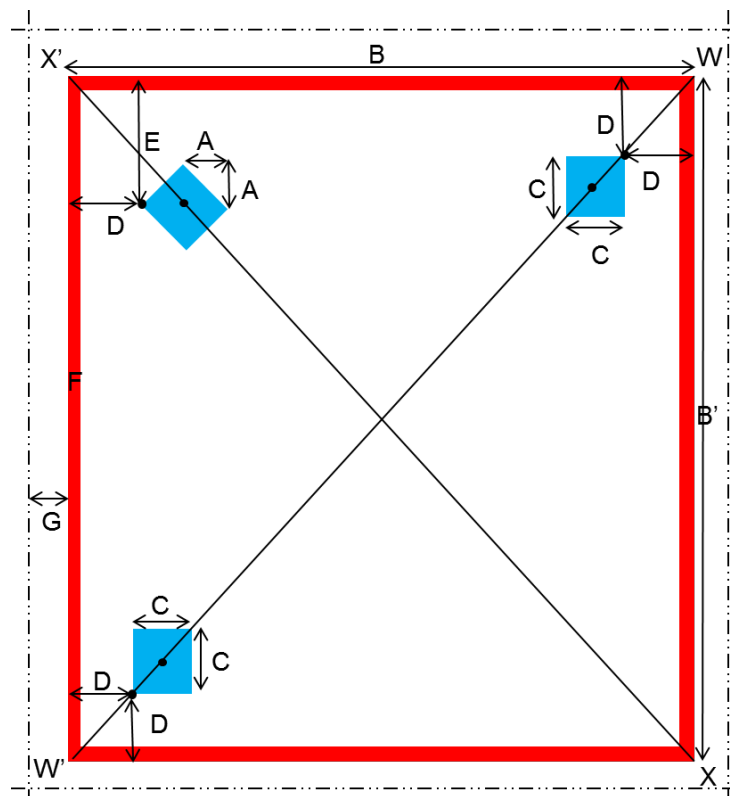


Figure 1
Specifications of C2C Alignment Mark

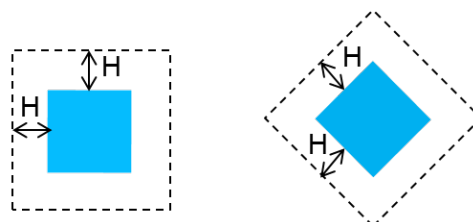


Figure 2
Keep Out Zone of C2C Alignment Mark

A: alignment mark dimension, 50 μm .

B, B': chip dimension, for example at least 3000 μm due to the machine handling constraint.

C: alignment mark dimension, 100 μm .

D: distance from alignment mark to seal ring (F) outer edge, 70 μm .

E: distance from alignment mark to seal ring (F) outer edge, 120 μm .

F: seal ring.

G: scribe line.