

SEMI 3D8-1121

GUIDE FOR DESCRIBING SILICON WAFERS FOR USE AS 300 mm CARRIER WAFERS IN A 3DS-IC TEMPORARY BOND-DEBOND (TBDB) PROCESS

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NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (§) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and §§) the symbols are used to reference more than one section or paragraph, respectively.

NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

1 Purpose

1.1 This Guide is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by defining the items/parameters needed to procure virgin silicon carrier wafers to be used in a 3DS-IC process.

2 Scope

2.1 This Guide defines the items/parameters to acquire silicon wafers to be used as carrier wafers in a temporary bond/debond (TBDB) application.

2.2 This Guide describes silicon wafers with nominal diameter of 300 mm although, for 3DS-IC applications, the actual wafer diameter may differ slightly due to process requirements.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This Guide does not describe dimensions and procedures related to wafers other than notched, 300 mm nominal diameter.

3.2 This Guide currently does not provide recommended ordering information for silicon device wafers for 3DS-IC applications. Refer to SEMI 3D9 and SEMI 3D10.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI 3D9 — Guide for Describing Materials Properties for a 300 mm 3DS-IC Wafer Stack

SEMI 3D10 — Guide to Describing Materials Properties for Intermediate Wafers for Use in a 300 mm 3DS-IC Wafer Stack

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M59 — Terminology for Silicon Technology

4.2 *ANSI® Standards*¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

4.3 *ASTM® Standards*²

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specific Precision, the Average for a Characteristic of a Lot or Process

4.4 *MHIA Standards*³

CEA 556-C — Outer Shipping Container Bar Code Label Standard

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Terms, acronyms, and symbols associated with silicon wafers and silicon technology are listed and defined in SEMI M59. Most of these terms and acronyms can be applied to wafers in a 3DS-IC process.

5.2 *Abbreviations and Acronyms*

5.2.1 *TBDB* — temporary bond/debond

5.3 *Definitions*

NOTE 1: Many of these definitions are similar to, but slightly different from, those in SEMI M59. In many cases the definitions in SEMI M59 can be generalized to include 3DS-IC terms, but this is not being done at the present time.

5.3.1 *back surface* — the surface of a wafer upon which the SEMI T7 mark appears.

5.3.2 *bottom surface* — an arbitrarily defined external surface of a wafer stack.

5.3.3 *carrier wafer* — a silicon or glass wafer used for temporary bonding to another wafer.

5.3.4 *debond* — a process where two bonded wafers are separated.

5.3.4.1 *laser debond* — debond using a laser process.

5.3.4.2 *mechanical debond* — debond using a physical process (i.e., cleaving, etc.).

5.3.4.3 *thermal debond* — debond under an elevated temperature process.

5.3.4.4 *ultraviolet (UV) light debond* — debond using ultraviolet process.

5.3.5 *device wafer* — a silicon wafer on which devices are formed.

5.3.6 *diameter, of a 3D wafer stack* — the diameter of the minimum circle that encloses all wafers.

5.3.7 *front surface* — the surface of a wafer opposite to that with the SEMI T7 marking.

5.3.8 *intermediate wafer* — a wafer which has undergone processing and is intended for use in, or has been included in, a wafer stack.

5.3.9 *top surface* — the external surface, opposite to the Bottom Surface, of a wafer stack.

5.3.10 *wafer bond* — a process by which two or more wafers are physically attached to each other using chemical and/or thermal and/or mechanical means.

5.3.11 *wafer bond, temporary* — a wafer bond which is intended to be debonded.

5.3.12 *wafer stack* — two or more wafers bonded to one another.

¹ American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, <http://www.ansi.org>. ANSI trademark is owned by American National Standards Institute.

² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>. ASTM trademark is owned by ASTM International.

³ Material Handling Industry of America, 8720 Red Oak Blvd., Suite 201, Charlotte, NC 28217, USA; Telephone: +1.704.676.1190; Fax: +1.704.676.1199, <http://www.mhia.org>

6 Ordering Information for Virgin 300 mm Diameter Silicon Wafers for Use as Carrier Wafers in 3DS-IC Applications

6.1 Purchase orders for 300 mm Silicon Carrier Wafers for 3DS-IC Applications should include the following items which are derived from Table 1 of SEMI M1.

- ◆ 2-1.1 Growth Method
- 2-1.2 Use of Refined Polysilicon
- 2-3.6 Hazardous Substances Restrictions
- 2-5.1 Wafer ID Marking
- 2-5.7 Edge Surface Condition
- 2-5.8 Back Surface Condition
- ◆ 2-6.1 Diameter
- ◆ 2-6.2 Notch Dimensions
- ◆ 2-6.3 Orientation of Notch Axis
- ◆ 2-6.6 Edge Profile Specification
- ◆ 2-6.7 Thickness
- 2-6.8 Total Thickness Variation (TTV)
- 2-6.9 Bow
- 2-6.10 Warp
- 2-6.11 Sori
- 2-6.12 Flatness, Global
- 2-8.1 Front Surface Scratches – Macro
- 2-8.5 Front Surface Localized Light Scatterers (LLS)
- 2-8.6 Front Surface Contamination/Area
- 2-8.11 Front Surface Dimples
- 2-8.12 Front Surface Grooves
- 2-8.13 Front Surface Mounds
- 2-8.15 Front Surface Saw Marks
- 2-9.4 Back Surface Contamination/Area
- 2-9.5 Back Surface Saw Marks

NOTE 2: These carrier wafers are specified as polished. In some instances, it may be possible to utilize as-cut or lapped wafers for carrier wafers. See the discussion in ¶ 2.4 of SEMI M1 for guidance in this case. If such wafers are desired they should be ordered as ‘as-cut’ or ‘lapped’ silicon carrier wafers rather than ‘polished’ silicon carrier wafers.

NOTE 3: Due to the variety of processes in use, silicon wafers for use as carriers for 300 mm device wafers may actually be specified to a different diameter than exactly 300 mm. In this Guide, the statement ‘300 mm carrier wafer’ encompasses all such carrier wafers irrespective of actual diameter.

6.2 If the carrier wafer is expected to be used in a stack that will undergo IR imaging of the bond plane from the back of the carrier wafer, the IR transmission should be specified such that the wafer is sufficiently transparent at the desired wavelength. The following line from Table 1 supplements to Table 1 of SEMI M1 and may be added to Table 1 of SEMI M1 in future versions.

2-2.5 IR Transmission