

SEMI 3D9-0914 (Reapproved 0420) GUIDE FOR DESCRIBING MATERIALS PROPERTIES FOR A 300 mm 3DS-IC WAFER STACK

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NOTICE: The section symbol (§) is used to reference a numbered section, paragraph, or header and all subordinate paragraphs, headers, and embedded material (i.e., EXCEPTIONs, lists) therein. The paragraph symbol (§) is used to reference a particular numbered paragraph and embedded material therein. When duplicated (i.e., §§ and §§§) the symbols are used to reference more than one section or paragraph, respectively.

NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

NOTICE: This Standard was reapproved with minor editorial changes.

1 Purpose

1.1 This Guide is intended to address the needs of the 3D Stacked IC (3DS-IC) industry by providing the tools needed to procure wafer stacks to be used in a 3DS-IC process.

2 Scope

2.1 This Guide provides the tools to describe wafer stacks in a 3DS-IC process. A wafer stacking process takes two or more intermediate wafers and forms a stack, which can then be further processed as if it were a single wafer. After bonding the dimensions of the stack will no longer conform to standard thickness and/or diameter.

2.2 This Guide describes wafer stacks with nominal diameter of 300 mm, although the actual stack diameter may differ due to process and functional variation.

2.2.1 The diameters of the different wafers that comprise the stack may differ from each other.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This Guide does not describe dimensions and procedures related to wafer stacks other than notched, 300 mm nominal diameter.

3.2 This Guide does not address issues associated with the bonding of chips to wafers; neither does it address issues associated with bonding of chips to other chips, nor does it describe interposer material.

3.3 This Guide does not address issues associated with processing, bonding, or handling individual diced chips.

4 Referenced Standards and Documents

4.1 SEMI Standards and Safety Guidelines

SEMI 3D4 — Guide for Metrology for Measuring Thickness, Total Thickness Variation (TTV), Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M59 — Terminology for Silicon Technology

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

4.2 *ANSI® Standards*¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

4.3 *ASTM® Standards*²

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, with Specific Precision, the Average for a Characteristic of a Lot or Process

4.4 *JEITA Standards*³

JEITA EM-3501 — Standard Methods for Determining the Orientation of a Semiconductor Silicon Single Crystal

4.5 *JSA Standards*⁴

JIS H 0611 — Methods of Measurement of Thickness, Thickness Variation and Bow of Silicon Wafer

4.6 *MHIA Standards*⁵

CEA 556-C — Outer Shipping Container Bar Code Label Standard

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Most terms, acronyms, and symbols associated with silicon wafers and silicon technology are listed and defined in SEMI M59. Most of these terms and acronyms can be applied to wafers in a 3DS-IC process.

5.2 *Definitions*

NOTE 1: Many of these definitions are similar to, but slightly different from, those in SEMI M59. In many cases the definitions in SEMI M59 can be generalized to include 3DS-IC terms, but this is not being done at the present time.

5.2.1 *back surface* — the surface of a wafer upon which the SEMI T7 mark appears.

5.2.2 *bottom surface* — an arbitrarily defined external surface of a wafer stack.

5.2.3 *carrier wafer* — a silicon or glass wafer used for temporary bonding to another wafer.

5.2.4 *device wafer* — a silicon wafer on which devices are formed.

5.2.5 *diameter, of a 3D wafer stack* — the diameter of the minimum circle that encloses all wafers.

5.2.6 *front surface* — the surface of a wafer opposite to that with the SEMI T7 marking.

5.2.7 *intermediate wafer* — a wafer which has undergone processing and is intended for use in, or has been included in, a wafer stack.

¹ American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, <http://www.ansi.org>. ANSI trademark is owned by American National Standards Institute.

² ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>. ASTM trademark is owned by ASTM International.

³ Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; Telephone: +81.03.5218.1050, Fax: +81.03.5218.1070, <http://www.jeita.or.jp>.

⁴ Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: +81.3.3583.8005, Fax: +81.3.3586.2014, <http://www.jsa.or.jp>

⁵ Material Handling Industry of America (MHIA), 8720 Red Oak Blvd., Suite 201, Charlotte, NC 28217, USA; Telephone: +1.704.676.1190; Fax: +1.704.676.1199, <http://www.mhia.org>

5.2.8 *top surface* — the external surface, opposite to the bottom surface, of a wafer stack.

5.2.9 *wafer bond* — a process by which two or more wafers are physically attached to each other using chemical and/or thermal and/or mechanical means.

5.2.10 *wafer bond, permanent* — a wafer bond which is intended to remain through the lifetime of the bonded layers.

5.2.11 *wafer bond, temporary* — a wafer bond which is intended to be de-bonded.

5.2.12 *wafer stack* — two or more wafers bonded to one another.

6 Wafer Stacks

6.1 Users of this Guide should note that a number of elements in the Wafer Stack Tracking Form have been identified as key to the correct description of wafer stacks for 3DS applications; these elements are indicated by a ♦ symbol in the left-most column of Table 1, Wafer Stack Tracking Form, Parts 1 and 2. Blocks with a ♦ symbol in the left-most column of Table 1 must be at least partially filled for this table to be useful; however, which elements of the block are required for a specific process flow must be negotiated between the supplier and the customer.

6.2 Samples of Table 1, filled out for different stacking configurations and process flows, are shown in Related Information 1.

NOTE 2: The descriptions in this section do not distinguish between bonds that are intended to be temporary and those that are intended to be permanent.

Table 1 Wafer Stack Tracking Form

NOTE 3: This table should evolve with the stack by electronic updates as the parameters change. Not all measurements are required at all process steps. The receiving party is expected to specify its requirements to the sending party. The terms used in this table are defined in §§ 6.3 through 6.10, below.

Part 1: General Information

ITEM	INFORMATION	DATE
Customer Name		
Purchase Order Number		
Line Number		
Item Number		
General Specification Number		
Revision Level		
Part Number/Revision		

Part 2: Stack Description

ITEM	SPECIFICATION	MEASUREMENT METHOD
2-1 STACK INFORMATION (Note that ♦ indicates a required item for which a value or choice must be indicated in order to minimally specify a wafer stack.)		
♦ 2-1.1	Stack ID ^{#1}	
♦ 2-1.2	Project	
♦ 2-1.3	# Wafers	
♦ 2-1.4	Thickness	
♦ 2-1.5	TTV	
♦ 2-1.6	Footprint	
Shape Parameters(2-1.7–2-1.9) use the Shape Decision Tree in SEMI M1, Appendix 2 to determine the appropriate use of these parameters		

ITEM			SPECIFICATION	MEASUREMENT METHOD
◆	2-1.7	Bow	_____ μm	☐ SEMI MF534; ☐ JIS H 0611; ☐ Other: (specify) _____
◆	2-1.8	Warp	_____ μm	☐ SEMI MF657; ☐ SEMI MF1390; ☐ Other: (specify) _____
◆	2-1.9	Sori	_____ μm	☐ SEMI MF1451; ☐ JEITA EM-3401; ☐ Other: (specify) _____
◆	2-1.10	Mass	_____ gm	
2-2 STACK MEASUREMENT CONDITIONS (Specify line number(s) from above/details of measurement. Insert extra lines as needed.)				
	2-2.7	Bow		
	2-2.8	Warp		
	2-2.9	Sori		
	2-2.10	Mass		
2-3 STACK DESCRIPTION (VISUAL)				
◆	2-3.1	Layer Diagram	Cut-and-paste a cross-sectional diagram into the block below, showing all wafers, substrates, bonding layers, underfill, top and bottom surfaces, and other relevant layers. Layers must be in the proper order and marked with the correct layer IDs. ^{#2} Update this diagram after each process step.	
2-4 TOP SURFACE^{#3} DESCRIPTION (Note that ◆ indicates a required item for which a value or choice must be indicated in order to minimally specify a wafer stack.)				
◆	2-4.1	Layer ID ^{#2}		
◆	2-4.2	Topography	☐ Unprocessed ☐ Patterned ☐ Other (specify) _____	
◆	2-4.3	Roughness		
◆	2-4.4	% Coverage		
◆	2-4.5	Outline	☐ Circular ☐ Other (specify) _____	
◆	2-4.6	Diameter, if circular	☐ 300 mm ☐ 300.4 mm ☐ Other (specify) _____ mm	
		Dimensions, if not circular	X dimension _____ mm Y dimension _____ mm	
◆	2-4.7	Material(s), list here and detail below		
◆	2-4.8	Protective Coating	☐ Yes (specify material) _____ ☐ No	
◆	2-4.9	Known Issues ^{#4}		
Material, Thermal, and Electrical Characteristics of Surface Materials. Repeat block additional times as needed. (Note that in this section a ◆ indicates that some of the elements in the block are required items; the specifics must be negotiated between the supplier and the customer.)				
◇	2-4.10	Specify Top Material I _____		
		% Coverage		

ITEM		SPECIFICATION	MEASUREMENT METHOD
		CTE [] $33 \times 10^{-7} \pm 1.5\%$ [] Other: (specify) _____ [] N/A	
		CTE Temperature Range [] $0^{\circ}\text{C}-300^{\circ}\text{C}$ [] Other: (specify range) _____ [] N/A	
		Thermal Conductivity (23°C) [] $0.0109 \text{ W}/(\text{cm K})$ [] Other: (specify) _____ $\text{W}/(\text{cm K})$ [] N/A	
		Bulk Resistivity [] _____ $\Omega \cdot \text{cm}$ [] N/A	
		Bulk Resistivity Tolerance [] $\pm$ _____ $\Omega \cdot \text{cm}$ [] N/A	
		Bulk Resistivity Variation (within wafer) [] _____ $\Omega \cdot \text{cm}$ [] N/A	
		Dielectric Constant [] _____ @ _____ kHz [] N/A	
		Dielectric Breakdown [] _____ MV/cm [] N/A	
		Loss Tangent [] _____ [] N/A	
		Leakage Current [] _____ A/cm ² @1 MV/cm field strength [] N/A	
◇	2-4.11	Specify Top Material II _____	
		% Coverage	
		CTE [] $33 \times 10^{-7} \pm 1.5\%$ [] Other: (specify) _____ [] N/A	
		CTE Temperature Range [] $0^{\circ}\text{C}-300^{\circ}\text{C}$ [] Other: (specify range) _____ [] N/A	
		Thermal Conductivity (23°C) [] $0.0109 \text{ W}/(\text{cm K})$ [] Other: (specify) _____ $\text{W}/(\text{cm K})$ [] N/A	
		Bulk Resistivity [] _____ $\Omega \cdot \text{cm}$ [] N/A	
		Bulk Resistivity Tolerance [] $\pm$ _____ $\Omega \cdot \text{cm}$ [] N/A	
		Bulk Resistivity Variation (within wafer) [] _____ $\Omega \cdot \text{cm}$ [] N/A	
		Dielectric Constant [] _____ @ _____ kHz [] N/A	
		Dielectric Breakdown [] _____ MV/cm [] N/A	
		Loss Tangent [] _____ [] N/A	

ITEM		SPECIFICATION		MEASUREMENT METHOD
		Leakage Current	☐ _____ A/cm ² @1 MV/cm field strength ☐ N/A	
2-5 BOTTOM SURFACE^{#3} DESCRIPTION (Note that ♦ indicates a required item for which a value or choice must be indicated in order to minimally specify a wafer stack.)				
♦	2-5.1	Layer ID ^{#2}		
♦	2-5.2	Topography	☐ Unprocessed ☐ Patterned ☐ Other: (specify) _____	
♦	2-5.3	Roughness		
♦	2-5.4	% Coverage		
♦	2-5.5	Outline	☐ Circular ☐ Other: (specify) _____	
♦	2-5.6	Diameter, if circular	☐ 300 mm ☐ 300.4 mm ☐ Other: (specify) _____ mm	
		Dimensions, if not circular	X dimension _____ mm Y dimension _____ mm	
♦	2-5.7	Material(s), list here and detail below		
♦	2-5.8	Protective Coating	☐ Yes (specify material) _____ ☐ No	
♦	2-5.9	Known Issues ^{#4}		
Material, Thermal, and Electrical Characteristics of Surface Materials. Repeat block additional times as needed. (Note that in this section a ◊ indicates that some of the elements in the block are required item; the specifics must be negotiated between the supplier and the customer).				
◊	2-5.10	Specify Bottom Material I _____		
		% Coverage		
		CTE	☐ $33 \times 10^{-7} \pm 1.5\%$ ☐ Other: (specify) _____ ☐ N/A	
		CTE Temperature Range	☐ 0°C–300°C ☐ Other: (specify range) _____ ☐ N/A	
		Thermal Conductivity (23°C)	☐ 0.0109 W/(cm K) ☐ Other: (specify) _____ W/(cm K) ☐ N/A	
		Bulk Resistivity	☐ _____ Ω·cm ☐ N/A	
		Bulk Resistivity Tolerance	☐ ± _____ Ω·cm ☐ N/A	
		Bulk Resistivity Variation (within wafer)	☐ _____ Ω·cm ☐ N/A	
		Dielectric Constant	☐ _____ @ _____ kHz ☐ N/A	
		Dielectric Breakdown	☐ _____ MV/cm ☐ N/A	

ITEM		SPECIFICATION	MEASUREMENT METHOD
		Loss Tangent [] _____ [] N/A	
		Leakage Current [] _____ A/cm ² @1 MV/cm field strength [] N/A	
◇	2-5.11	Specify Bottom Material II _____	
		% Coverage	
		CTE [] $33 \times 10^{-7} \pm 1.5\%$ [] Other: (specify) _____ [] N/A	
		CTE Temperature Range [] 0°C–300°C [] Other: (specify range) _____ [] N/A	
		Thermal Conductivity (23°C) [] 0.0109 W/(cm K) [] Other: (specify) _____ W/(cm K) [] N/A	
		Bulk Resistivity [] _____ $\Omega \cdot \text{cm}$ [] N/A	
		Bulk Resistivity Tolerance [] $\pm$ _____ $\Omega \cdot \text{cm}$ [] N/A	
		Bulk Resistivity Variation (within wafer) [] _____ $\Omega \cdot \text{cm}$ [] N/A	
		Dielectric Constant [] _____ @ _____ kHz [] N/A	
		Dielectric Breakdown [] _____ MV/cm [] N/A	
		Loss Tangent [] _____ [] N/A	
		Leakage Current [] _____ A/cm ² @ 1 MV/cm field strength [] N/A	

	Layer ID ^{#2}	ORIGINAL SEMI T7 ^{#1}	SHAPE	DIMENSIONS	FUNCTION	EDGE CONDITION
2-6 WAFERS/SUBSTRATES^{#5} (Describe the geometry of each wafer in the stack. Add rows as needed. Note that ♦ indicates a required item for which a value or choice must be indicated in order to minimally specify a wafer stack.)						
♦	2-6.1	SEMI T7 Condition: ☐ Present ☐ Present and Obscured ☐ Removed	☐ Circular ☐ Not Circular (specify) _____	Circular ☐ 300 mm ☐ 300.4 mm ☐ Other: (specify) _____ mm Not Circular X _____ mm Y _____ mm	☐ Interposer ☐ Carrier ☐ Device (specify) ☐ Logic ☐ Interconnect ☐ MEMS ☐ Optical ☐ RF ☐ _____	☐ Square ☐ Beveled ☐ Stepped ☐ Irregular ☐ Other: (specify) _____
♦	2-6.2	SEMI T7 Condition: ☐ Present ☐ Present and Obscured ☐ Removed	☐ Circular ☐ Not Circular (specify) _____	Circular ☐ 300 mm ☐ 300.4 mm ☐ Other: (specify) _____ mm Not Circular X _____ mm Y _____ mm	☐ Interposer ☐ Carrier ☐ Device (specify) ☐ Logic ☐ Interconnect ☐ MEMS ☐ Optical ☐ RF ☐ _____	☐ Square ☐ Beveled ☐ Stepped ☐ Irregular ☐ Other: (specify) _____

1 ST WAFER Layer ID ^{#2}	2 ND WAFER Layer ID ^{#2}	LOCATION ON 1 ST WAFER (x, y OR r, θ)	OFFSET ON 2 ND WAFER (Δx, Δy OR Δr, Δθ)
2-7 WAFER ALIGNMENT (List as many points as needed for each pair of adjacent wafers; add rows as needed.)			

Layer ID ^{#2}	MATERIAL	THICKNESS	TTV	COMMENTS
2-8 LAYERS (Describe all layers shown in the diagram including wafers and substrates. Layers need not be listed in order; this makes it easier to copy and paste when two stacks are merged. Note that ♦ indicates a required item for which a value or choice must be indicated in order to minimally specify a wafer stack.)				
♦				
♦				
♦				
♦				

MATERIAL	COMMENTS
2-9 ADDITIONAL MATERIALS (List any materials present in the stack but not identified in the layer table.)	

2-10 ADDITIONAL NOTES (*Describe any special conditions or issues—adhesive extrusions, alignment of nonadjacent wafers, etc.; add rows as needed.*)

#1 It is assumed that at least one wafer in the stack maintains its original diameter, notch, and (probably) SEMI T7 marking. The stack may inherit its ID from this wafer or be assigned an arbitrary new ID.

#2 Each wafer, substrate, or other layer in the stack is given a unique Layer ID as follows:

- *Wafers/Substrates* — The first two wafers (or substrates) in a stack are named with adjacent uppercase letters. For example, M and N. A wafer bonded to M is named L and so on, back to A; a wafer bonded to N is named O and so on, down to Z. If a wafer or substrate is stripped from the stack its ID is not re-used.
- *Other Layers* — The first layer applied to the face of M is named Mf01; the next layer is Mf02 and so on. The first layer applied to the back of M is Mb01; the next is Mb02 and so on. If a layer is stripped its Layer ID is not re-used.
- *Stacks of Stacks* — If two stacks are bonded together there is the possibility of duplicate wafer/substrate IDs. Therefore, each Layer ID receives a single digit as a prefix. The first two stacks so combined use digits 1 and 2 (assignment is arbitrary). For example, layer Mb02 in one stack becomes layer 1Mb02, and layer Mf01 in the other stack becomes 2Mf01.

#3 Each stack has two surfaces, defined as ‘top’ and ‘bottom’ by the stack diagram.

#4 Known Issues for each surface should include defects, particles, etc.

#5 Each unstacked wafer has a front side and a back side, as defined in § 6 of this Standard, with a SEMI T7 marking on the back side. After a wafer is incorporated into a stack, ‘f’ and ‘b’ will refer to the original front and back of that wafer. A wafer that is edge-trimmed or thinned will lose its SEMI T7 marking, but a reference to that marking will be retained in 2-6 of this Standard.

6.3 Stack Information

6.3.1 *Stack ID* — Typically an unobscured SEMI T7 marking on either the top or bottom wafer of the stack. Preference should be given to a SEMI T7 mark least likely to be removed or obscured during additional processing.

6.3.2 *# Wafers* — The count of full or partial thickness wafers bonded together into a stack.

6.3.3 *Thickness* — The measured thickness of the stack. For guidance on measuring dimensional parameters on a wafer stack, see SEMI 3D4.

6.3.4 *Footprint* — A description of the x - y - θ geometry of the wafer stack; typically circular.

6.3.5 *Shape* — The shape decision tree in SEMI M1, Appendix 2 fully describes the various shape parameters that can be specified.

6.3.5.1 *Warp* — There are two forms of warp, one corrected for gravitational sag and the other not so corrected. For guidance on measuring dimensional parameters on a wafer stack, refer to SEMI 3D4.

6.3.5.2 *Bow* — A sign may be included in the specification to denote convex (positive) or concave (negative) curvature of the median surface of the wafer stack with the top surface facing up. If no sign is included in the specification, bow may vary between $-a$ and $+a$, where ‘ a ’ is the specified maximum magnitude of bow. For guidance on measuring dimensional parameters on a wafer stack, refer to SEMI 3D4.

6.3.5.3 *Sori* — Although similar to warp, sori is measured on a different plane. For guidance on measuring dimensional parameters on a wafer stack, see SEMI 3D4.

6.3.6 *Mass* — Should be specified.

6.4 *Stack Description (visual)* — A graphical representation of a cross-section of the stack.

6.5 Top Surface Description/Bottom Surface Description

6.5.1 These sections describe the exposed material(s) that make up the top and bottom surfaces of the stack.

6.5.2 *Topography* — This line is included to indicate whether the surface is unprocessed or if it is patterned, or otherwise modified.

6.5.3 *Roughness* — A measure of short wavelength variation of the surface.

6.5.4 *% Coverage* — Describe the surface layer area as a percentage of the total diameter of the stack, not the material(s) which make up this layer; such material(s) is(are) described below.

6.5.5 *Outline* — Indicate whether the layer is circular or some other shape.

6.5.6 *Diameter/Dimensions* — Provide the exact diameter or *x-y* dimensions of the surface layer.

6.5.7 *Materials* — List all materials on the wafer stack surface except passivation layer(s) as defined below.

6.5.8 *Passivation* — Describe any material deposited on the surface intended to protect the surface from physical damage or to prevent chemical reaction during shipping or storage.

6.5.9 *Known Issues* — This line should include any properties or the materials or any issues that would be useful to the receiving party that are not otherwise described in the table.

6.5.10 *Material, Thermal, and Electrical Characteristics of Surface Materials*

6.5.10.1 The purpose of this section is to describe the characteristics of each material that appears on the surface of the wafer. If the surface is patterned, or if different materials are present on different regions, fill in as many blocks as necessary to identify all materials present.

6.5.10.2 *% Coverage* — If the surface is patterned with multiple materials, put the approximate percentage of the surface area covered by this material.

6.5.10.3 Indicate, if applicable, the CTE, CTE temperature range, thermal conductivity, bulk resistivity, bulk resistivity tolerance, bulk resistivity variation, dielectric constant, loss tangent, and leakage current.

6.6 *Wafers/Substrates* — Describe the wafers that compose the stack including the original SEMI T7 codes, the condition of the original SEMI T7 codes, and the wafers' outlines, dimensions, functions, and edge conditions.

6.7 *Wafer Alignment* — The measured alignment between adjacent wafers in the stack.

6.8 *Layers* — All wafers as well as all layers related to the bonding. Do not include layers that were processed onto any wafers before bonding if these play no part in the bonding process.

6.9 *Additional Materials* — Materials that are present on the wafer, but not listed elsewhere; for example, in non-surface layers.

6.10 *Additional Notes* — Any special conditions or issues.

7 Sampling

7.1 Unless otherwise specified, ASTM E122 should be used to define the sampling plan. When so specified, appropriate sample sizes should be selected from each lot in accordance with ANSI/ASQ Z1.4. Each quality characteristic should be assigned an acceptable quality level (AQL) or lot tolerance percent defective (LTPD) value in accordance with ANSI/ASQ Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels should be agreed upon between the supplier and the purchaser.

8 Test Methods

8.1 Measurements should be made or certifiable to one of the SEMI, ASTM, JEITA, or JIS standard test methods for the item as selected from Specification Ordering Table and specified in the purchase order.

NOTE 4: Although they are no longer supported nor supplied by DIN, DIN silicon standards are also listed in this section and may be used if available to the testing lab and agreed upon between supplier and customer. English translations of most of these standards are published in Volume 10.05 of the 1993 *Annual Book of ASTM Standards*, which may be available to some organizations. Titles of these standards are given in the Referenced Standards and Documents section.

8.2 If several different standard test methods for an item are commonly used within a region, it is particularly important that the applicable method of test be identified in the purchase order.

8.3 If no method of test is specified in the purchase order and if standard test methods from different geographic regions are available, the default method should be a method in common usage for the region of the purchaser of the wafer.

8.4 If no standard test method for an item is available, the test procedure to be used must be agreed upon between supplier and customer.

9 Certification

9.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this Specification, together with a report of the test results, should be furnished at the time of shipment.

9.2 In the interest of controlling inspection costs, the supplier and the customer may agree that the material should be certified as 'capable of meeting' certain requirements. In this context, 'capable of meeting' should signify that the supplier is not required to perform the appropriate tests in § 11. However, if the customer performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Product Labeling

10.1 Wafers supplied following this Guide should be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafer stack will be stored prior to further processing. Identification should include as a minimum the nominal diameter, conductivity type, dopant, orientation, resistivity range, and lot number. The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to wafer manufacture but providing reference to the original lot number, should provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information should be retained on file at the manufacturer's facility for at least one month after that particular lot has been accepted by the customer.

10.2 Wafers supplied following this Guide should be shipped in packages labeled in accordance with SEMI M45.

11 Packing and Shipping Container Labeling

11.1 Special packing requirements should be subject to agreement between the supplier and customer. Otherwise, all wafers should be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination and in accordance with the best industry practices to provide ample protection against damage during shipment.

11.2 Unless otherwise indicated in the purchase order, all outside wafer shipping containers should be labeled in accordance with CEA 556-C.

12 Related Documents

12.1 *SEMI Standards and Safety Guidelines*

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF951 — Test Method for Determination of Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF1391 — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

12.2 *ASTM® Standards*²

ASTM D523 — Standard Test Method for Specular Gloss

12.3 *JSA Standards*⁴

JIS Z 8741 — Specular Glossiness – Methods of Measurement

RELATED INFORMATION 1

SAMPLE WAFER STACK DESCRIPTIONS

NOTICE: This Related Information is not an official part of SEMI 3D9 and was derived from the work of the 3D Packaging and Integration Global Technical Committee. This Related Information was approved for publication by full letter ballot procedures on May 12, 2014.

R1-1 3D Process Flow Illustrations

R1-1.1 This section contains illustrations of three 3D process flows.

R1-1.1.1 The sample flow shown in Figure R1-1 is for a process by which two wafers, only one of which has circuitry and TSVs, are bonded together, the processed wafer thinned, and the pair de-bonded. It also includes an optional extension by which a third wafer can be added before de-bonding. This flow is intended as an example of a temporary bonding process.

R1-1.1.2 The sample flow shown in Figure R1-2 is for a process by which four wafers, each of which has circuitry and TSVs, are bonded together in a stack. This flow is intended as an example of a permanent bonding process.

R1-1.1.3 The sample flow shown in Figure R1-3 is for a process by which three wafers, each of which has circuitry and TSVs, are bonded together in a stack. This flow is intended as an example of a permanent bonding process using C4 bumps and microbumps.

R1-2 Table 9 Examples

R1-2.1 This section contains examples of Table 9 partially filled out for wafer stacks at various stages of the bonding processes described in § R1-1. The data shown illustrate the key points for using this table to communicate the steps of a wafer bond process.

R1-2.1.1 Table R1-1 is a sample of a wafer pair at Step 5 of Figure R1-1 (temporary flow).

R1-2.1.2 Table R1-2 is a sample of a wafer pair at Step 8 of Figure R1-1 (temporary flow).

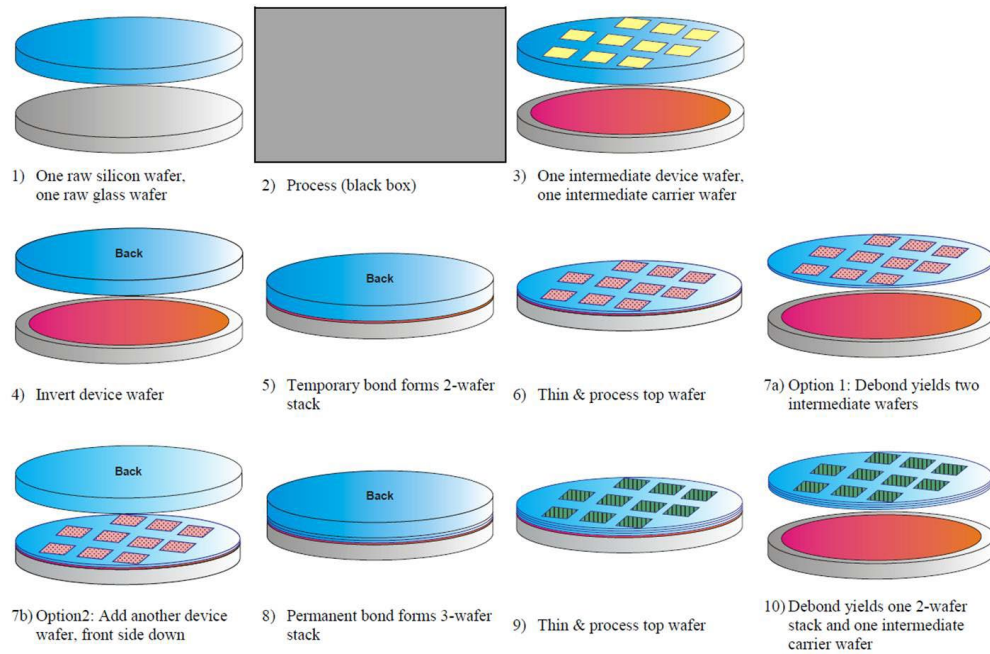
R1-2.1.3 Table R1-3 is a sample of a wafer pair at Step 10 of Figure R1-1 (temporary flow).

R1-2.1.4 Table R1-4 is a sample of a wafer pair at Step 6 of Figure R1-2 (permanent flow).

R1-2.1.5 Table R1-5 is a sample of a wafer pair at Step 8 of Figure R1-2 (permanent flow).

R1-2.1.6 Table R1-6 is a sample of a wafer pair at Step 8 of Figure R1-3 (bumped permanent flow).

Sample flows with temporary bonding



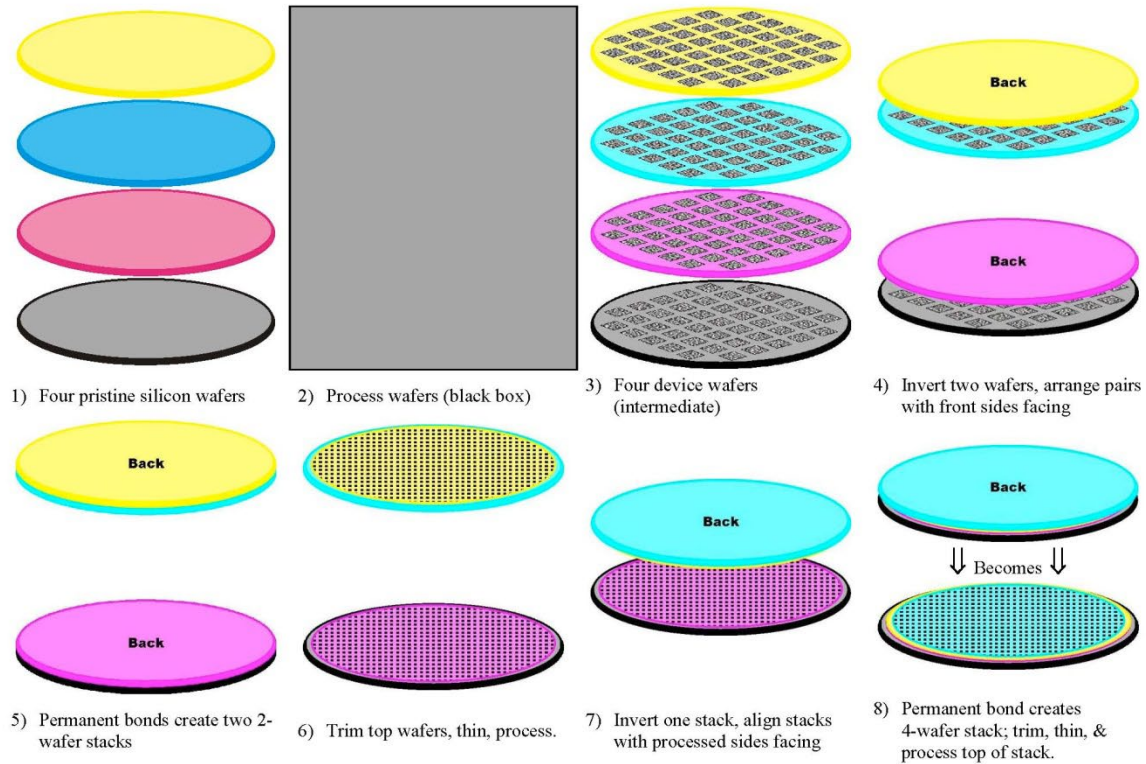
#1 This figure includes an optional extension by which a third wafer could be added to the stack before de-bonding.

#2 This flow is to be used in reference to Tables R1-1, R1-2, and R1-3.

Figure R1-1

Temporary bonding example flow for a process by which two wafers, only one of which has circuitry and TSVs, are bonded together, the processed wafer thinned, and the pair de-bonded.

Sample flow with permanent bonding



#1 This flow is to be used in reference to Tables R1-4 and R1-5.

Figure R1-2
Permanent bonding example flow for a process by which four wafers, each of which has circuitry and TSVs, are bonded together in a stack.