

SEMI E129-0706

GUIDE TO ASSESS AND CONTROL ELECTROSTATIC CHARGE IN A SEMICONDUCTOR MANUFACTURING FACILITY

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1 Purpose

1.1 The purpose of this document is to minimize the negative impact on productivity caused by static charge in semiconductor manufacturing environments. It is a guide for establishing electrostatic compatibility in facilities used for semiconductor manufacturing.

1.2 Electrostatic surface charge causes a number of undesirable effects in semiconductor manufacturing environments. Electrostatic discharge (ESD) damages both products and reticles. ESD events also cause electromagnetic interference (EMI), resulting in equipment malfunctions. Charged wafer and reticle surfaces attract particles (electrostatic attraction or ESA) and increase the defect rate. Charge on products can also result in equipment malfunction or product breakage. Operating problems and additional product defects due to static charge can have a negative impact on the cost of ownership of semiconductor manufacturing equipment (refer to SEMI E35).

1.3 For product and reticle protection or EMI control, the measurement of the ESD risk of an area is defined by the presence and nature of the ESD events that occur. For contamination control by reducing particle attraction, the static risk of an area is defined by the presence and level of static charges.

1.4 While an increasing amount of semiconductor production is done in minienvironments or within the production equipment, product and reticles must still be transported throughout the manufacturing facility. They are both affected by, and the cause of static problems during transport. Moving personnel in the manufacturing facility are also sources of static charge problems. This document addresses the presence of static charge in the entire facility, including the production equipment and minienvironments.

1.5 Static control methods can be incorporated in the factory design to reduce static charge to acceptable levels. This guide is intended for use primarily by semiconductor manufacturers and cleanroom facilities designers during the design of their facilities. Producers of the silicon wafers and photomasks used in semiconductor manufacturing will also find it useful. There are test methods available (see § 7 and Related Information 2 of this guide) to demonstrate the effectiveness of the static control methods. The end user will be able to use the same test methods to verify compliance with a facility design specification after the facility is built or after design changes have been made, and to verify ongoing compliance as a part of factory maintenance procedures.

1.6 Semiconductor process technology will continue to move toward smaller product geometries. Acceptable static charge levels will decrease with product feature size. This document will help to assure that facility static charge limits are appropriate for the product being manufactured.

2 Scope

2.1 The scope of this document is limited to methods of measurement and a guide for the maximum recommended level of static charge on all facility surfaces including:

- Product, photomasks or their carriers,
- Facility construction materials and furniture,
- Personnel,
- Packaging and transport materials, and
- Equipment (through reference to SEMI E78)

2.2 This document references SEMI E78, SEMI E43 and other methods of measuring static charge as well as the performance parameters of static control methods.

2.3 Appendix 1 describes the methodology for determining the maximum recommended static charge levels that are shown in ¶ 12.5 Table 1.

NOTE 1: Related Information 1 discusses device sensitivity measurements, which are the first step in setting recommended static levels in a facility. Related Information 2 describes static control methods commonly used in semiconductor manufacturing. Related Information 3 discusses the relationship between ESD and EMI.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 *Static Measurements* — Measurements of electrostatic quantities such as charge, electric field, voltage, and resistance to ground are difficult to make. The nature of the object (insulator or conductor), its geometry, its surroundings, and the measuring equipment itself, are only a few of the factors affecting the accuracy of an electrostatic measurement. In general, direct measurement of static charge is possible with small, moveable objects. Larger objects, and those fixed in position, will need to be characterized by the electric field that results from the static charge.

3.2 *Location* — The test methods for static charge and maximum recommended levels of static charge on facility surfaces are meant to be applied after the facility has been built. Testing the performance of static control methods may be done before or after construction. It may be difficult to directly relate the performance of the static control method to the static charge level that results in the completed facility. Prior experience of the static control supplier will be a source of this information.

3.3 *Test Methods* — The test methods referenced in this document do not guarantee precise measurements of static charge levels. The maximum static charge levels recommended in this document have large tolerances (see ¶ 15.1).

3.4 *Static Charge Control* — There are a variety of static related issues in a semiconductor manufacturing environment. The issues are complex due to the wide range of electrostatic problems, and device or equipment sensitivities to these problems. This guide contains general recommendations. Users of this document are cautioned that specific static related problems may require or allow different levels of static charge than are recommended in this document.

3.5 Measurements

3.5.1 *Measurements of Very High Static Potentials (>30,000 V)* — Measurements of very high static potentials (>30,000 V) may need to be done at larger distances to avoid exceeding the measurement range of the meter and/or an ESD event to the meter.

3.5.2 *Measurements on Moving Objects or Surfaces* — Care should be taken, when attempting to read electrostatic charges on moving objects or surfaces, to maintain correct distance and avoid any contact; this is to ensure "good" readings with no mechanical damage or personal injury.

4 Referenced Standards and Documents

4.1 SEMI Standards

SEMI E10 — Specification for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM)

SEMI E33 — Specification for Semiconductor Manufacturing Facility Electromagnetic Compatibility

SEMI E35 — Guide to Calculate Cost of Ownership (Coo) Metrics for Semiconductor Manufacturing Equipment

SEMI E43 — Guide for Measuring Static Charge on Objects and Surfaces

SEMI E78 — Guide to Assess and Control Electrostatic Discharge (Esd) and Electrostatic Attraction (Esa) for Equipment

4.2 ESD Association Standards and Advisories¹

ANSI ESD S1.1 — Evaluation, Acceptance, and Functional Testing of Wrist Straps

ANSI ESD STM2.1 — Resistance Test Method for Electrostatic Discharge Protective Garments

ANSI ESD STM3.1 — Ionization

ANSI ESD S4.1 — Worksurfaces – Resistance Measurements

ANSI ESD STM4.2 — Worksurfaces – Charge Dissipation Characteristics

¹ Electrostatic Discharge Association, 7900 Turin Road, Building 3, Suite 2, Rome, NY 13440-2069, USA. Telephone: 315.339.6937; Fax: 315.339.6793; Website: www.esda.org

- ANSI ESD STM5.1 — Electrostatic Discharge Sensitivity Testing – Human Body Model
- ANSI ESD STM5.2 — Electrostatic Discharge Sensitivity Testing – Machine Model
- ANSI ESD STM5.3.1 — Charged Device Model (CDM) – Component Level
- ANSI ESD S6.1 — Grounding – Recommended Practice
- ANSI ESD STM7.1 — Floor Materials – Resistive Characterization of Materials
- ANSI ESD S8.1 — ESD Awareness Symbols
- ANSI ESD STM9.1 — Resistive Characterization of Footwear
- ESD SP10.1 — Automated Handling Equipment
- ANSI ESD STM11.11 — Surface Resistance Measurement of Static Dissipative Planar Materials
- ANSI ESD STM11.12 — Volume Resistance Measurement of Static Dissipative Planar Materials
- ANSI ESD S11.31 — Evaluating the Performance of Electrostatic Discharge Shielding: Bags
- ANSI ESD STM12.1 — Seating – Resistive Characterization
- ANSI ESD S20.20 — Standard for the Development of an ESD Control Program
- ANSI ESD STM97.1 — Floor Materials and Footwear – Resistance Measurement in Combination with a Person
- ANSI ESD STM97.2 — Floor Materials and Footwear Voltage Measurement in Combination with a Person
- ESD AVD1.0 — Glossary of Terms
- ESD TR55.0-01-01 — Electrostatic Guidelines and Considerations for Cleanrooms and Clean Manufacturing
- ESD TR20.20 — ESD Handbook
- ESD ADV53.1 — ESD Protective Workstations
- 4.3 *IEC Documents*²
 - IEC 61000-4-2 — Electromagnetic compatibility (EMC) Part 4.2: Testing and measurement techniques — Electrostatic discharge immunity test, Transient Immunity Standard, International Electrotechnical Commission (IEC).
 - IEC EN 61340-5-1 — Electrostatics – Part 5.1: Protection of electronic devices from electrostatic phenomena — General Requirements.
- NOTE 2: This replaces CENNELEC 100015-1 — Elements of a Static Control Program
- IEC EN 61340-5-2 — Electrostatics – Part 5.2: Protection of electronic devices from electrostatic phenomena — Users' Guide – Elements of a Static Control Program
- 4.4 *JEDEC Documents*³
 - JESD22-A114 — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
 - JESD22-A115 — Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)
 - JESD22-C101 — Field-Induced Charged-Device Model Test Methods for Electrostatic Discharge Withstand Thresholds of Microelectronic Components
 - JESD625 — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- 4.5 *Other Documents*
 - 89/336/EEC — Directive on Electromagnetic Compatibility – European Commission⁴
 - BS EN 50082-2 — Electromagnetic Compatibility (EMC). Generic Immunity Standards. Immunity for Industrial Environments, British Standards Institution (BSI)⁵
- ITRS 2005 — International Technology Roadmap for Semiconductors – ITRS⁶

2 International Electrotechnical Commission, 3, rue de Varembe, Case Postale 131, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.919.02.11; Fax: 41.22.919.03.00; Website: www.iec.ch

3 JEDEC Solid State Technology Association (aka the Joint Electron Device Engineering Council), 2500 Wilson Boulevard, Arlington, VA 22201-3834, USA. Telephone: 703.907.7560; Fax: 703.907.7583; Website: www.jedec.org

4 European Commission, Rue de la Loi, Wetstraat 200, B-1049 Brussels, Belgium; Website: www.europa.eu.int

5 BSI, 389 Chiswick High Road, GB - LONDON W4 4AL; Website: www.BSI-global.com

6 ITRS Global Communication Center, SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, USA; Website: <http://public.itrs.net>

MIL-STD 883 — Test Method Standard – Microcircuits (Method 3015.7 – Electrostatic Discharge Sensitivity Classification), Defense Supply Center Columbus⁷

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Definitions

5.1.1 *carrier* — a device for holding wafers, dies, packaged integrated circuits, or reticles for various processing steps in semiconductor manufacturing (from SEMI E78).

5.1.2 *electromagnetic interference (EMI)* — any electrical signal in the non-ionizing (sub-optical) portion of the electromagnetic spectrum with the potential to cause an undesired response in electronic equipment.

5.1.3 *electrostatic attraction (ESA)* — the force between two or more oppositely charged objects.

NOTE 3: The result is increased deposition rate of particles onto charged surfaces, or movement of charged materials.

5.1.4 *electrostatic compatibility* — charge control adequate to allow the manufacturing of products and the inter-equipment transfer of products, reticles, and carriers without electrostatic problems.

5.1.5 *electrostatic discharge (ESD)* — the rapid spontaneous transfer of electrostatic charge induced by a high electrostatic field.

NOTE 4: Usually the charge flows in a spark between two objects at different electrostatic potentials.

5.1.6 *ESD simulator* — an instrument providing a specified electrostatic discharge current waveform when discharged directly to a product or equipment part.

5.1.7 *facility electrostatic levels* — acceptable static charge levels related to the major technology nodes of product and reticle feature sizes.

5.1.8 *minienvironment* — a localized environment created by an enclosure to isolate the product from contamination and people.

5.1.9 *product* — any unit intended to become a functional semiconductor device.

6 Establishing Requirements

6.1 The following sections contain test methods that can be used to establish static damage thresholds for product, reticles, or equipment. They also contain test methods to determine the levels of static charge and electrostatic fields that result on product, reticles, and equipment during the manufacturing process.

6.2 As an alternative to determining actual static charge sensitivity levels for product, reticles, and equipment, the end user may establish requirements based on the year and technology node of the manufacturing process. Recommendations for acceptable facility electrostatic levels are found in ¶ 12.5 Table 1.

6.3 *Measurement Methods and Instrumentation* — No single method of testing for static charge can determine a “safe” level. The amount of static charge, the distribution of static charge on an object, and the nature of the static discharge will all interact to determine if the charge level is safe. It will be difficult to determine levels that *guarantee* static related problems are totally eliminated. The goals of this guide are to assist the user in identifying static charge levels likely to cause problems in the semiconductor manufacturing facility, and to direct the user to static control methods appropriate to mitigate these problems. This guide is intended to provide the user with enough insight to define test methodologies for measuring static charge and for evaluating the methods to control it.

6.4 ESD Damage — Direct Discharge

6.4.1 When considering direct ESD damage to an object (e.g., product, reticle, or equipment), the important parameter is the current accompanying the charge transfer to or from the object. The charge may be transferred from facility and furniture surfaces, personnel, equipment parts, carriers, packaging materials, or anything else that contacts the object.

6.4.2 Established test methods exist for determining the threshold of damage to a particular object. When testing packaged devices, ESD simulators of various types are used. Refer to ESD Association standards ESD STM5.1, ANSI ESD STM5.2, and ANSI ESD STM5.3.1; JEDEC JESD22-A114, JESD22-A115, and JESD22-C101; or MIL-STD 883 for further information concerning device testing. There are no established standards for ESD simulator testing of wafers, reticles, or unpackaged semiconductor devices. ESD damage thresholds for these items may be significantly different than for packaged devices.

⁷ Defense Supply Center Columbus, P.O. Box 3990, Columbus, OH 43216-5000, USA; Website: www.dscc.dla.mil

6.4.3 Once the damaging current level for a product is determined using an appropriate ESD simulator, the corresponding amount of charge is known from the ESD simulator operating parameters.

6.4.4 In the manufacturing facility, it is important to know the charge on any objects that might directly contact the product. Charge measurement methods using a coulombmeter and Faraday Cup are described in SEMI E78 and SEMI E43 for isolated conductors (including personnel), or small and moveable objects. The measurement methods of SEMI E43 can be used to establish that the charge levels on these objects will pose a hazard to products or reticles from a direct ESD event.

6.4.5 Electric field measurements on large and fixed objects, or insulators are less useful in estimating whether or not a damaging direct ESD event will occur. On objects that cannot be conveniently measured with a coulombmeter, Electrostatic Fieldmeter measurements can be useful in estimating the ESD threat, even though the measurement may be less quantitative than the coulombmeter measurement.

6.5 ESD Damage — Induced Charge

6.5.1 Charge may be induced on an object that results in ESD damage. Part of a product (e.g., epoxy package) or reticle (e.g., quartz substrate) may become charged and *induce* charge separation to occur on another part of the product (e.g., lead pins) or reticle (e.g., chrome traces). ESD will occur if the lead pins or chrome traces contact ground. Using a coulombmeter or Faraday Cup and the methods of SEMI E43, the end user should test product or reticles to determine the level of static charge at which ESD damage occurs.

6.5.2 Alternatively, either the product or reticles may be handled in proximity to another charged object. The field from this charged object induces charge on product or reticles, and ESD can result if the product or reticle contacts ground while in the presence of the field. Using an electrostatic fieldmeter and the methods of SEMI E43, the end user should test products and reticles to determine the acceptable levels of electric field from static charge.

6.5.3 It has been shown that a changing electric field causes ESD damage to reticles without ground contact occurring. A changing electric field can result at the reticle when an object in proximity to the reticle acquires a charge, the reticle or a charged object are in motion with respect to each other, or grounding conditions change the field between a charged object and the reticle (e.g., due to robot handling). See references in Related Information 2. In areas of the manufacturing facility that produce or handle reticles, electric field from any charged object will need to be limited to levels that do not cause reticle ESD damage. Test methods for electric field are contained in SEMI E43. There are currently no industry standards for determining the electric field sensitivity of reticles, but test methods do exist.

6.5.4 Finally, there is increasing anecdotal evidence that the *presence* of static charge on wafer surfaces is becoming an ESD hazard as gate oxide thicknesses become thinner. In the future, there may need to be further limits on allowable static charge on wafer surfaces to prevent ESD-related gate oxide damage during front-end semiconductor manufacturing. Further research is needed in this area.

6.6 Particle Attraction

6.6.1 Electrostatic attraction (ESA) of particles can occur due to the electrostatic field created by the charge on the surface of an object. Refer to SEMI E78 and SEMI E43 for an analysis of this effect and its measurement methods.

6.6.2 Particles may be attracted to charged facility surfaces, or directly to charged products or reticles. Subsequently, they may be dislodged from facility surfaces and transfer to products or reticles. Once on products or reticle surfaces they may cause either random or repeating defects.

6.6.3 Electrostatic particle deposition velocity depends only on electric field, particle size and particle charge. However, the number of particles deposited on a surface also depends on the particle concentration in the area and the length of the exposure time during which particle deposition occurs. SEMI E78 contains information to relate allowable electric field to ambient particle concentration and exposure time.

6.6.4 The measurement methods of SEMI E43 can be used to establish that the electric field from any facility surface meets the requirements of this document.

6.6.5 Charge is difficult to evaluate on large objects, especially insulators. Electric field measurements on these objects may be useful in estimating the risk that a damaging direct ESD event might occur. However, electric field measurements on insulators are highly qualitative and only provide a figure of merit as to the threat that these charges may represent to the ESD-sensitive device.

6.7 Equipment ESD

6.7.1 Equipment ESD immunity has been established at levels considerably higher than those that result in damage to product and reticles. If facility static charge limits shown in ¶ 12.5 Table 1 are used to protect product and reticles, they will provide sufficient protection for the equipment.

6.7.2 Equipment ESD immunity is addressed, in general, through a number of international standards including IEC 61000-4-2, BS EN50082-2 for European CE compliance, and the guidelines in SEMI E33. Measurements are made using an ESD simulator, which is described in these standards.

7 Apparatus

7.1 *ESD Damage* — For measuring the charge generated on product, reticles, or carriers, the Faraday Cup test method is shown in Figure 1. Additional information on this test method is contained in SEMI E43.

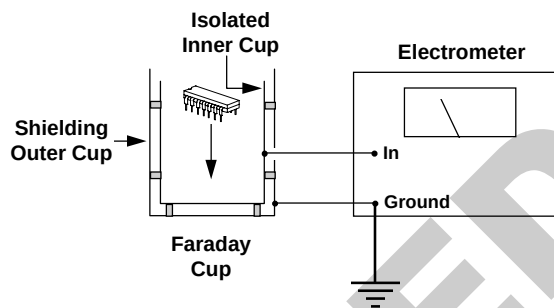


Figure 1
Faraday Cup Charge Measurement

7.2 When the object whose charge is to be measured is conductive, a nanocoulombmeter may be used. Additional information on this test method is contained in SEMI E43.

7.3 The instrument used for making electrostatic field measurements on large objects or surfaces is known as an electrostatic fieldmeter. Instructions concerning its use should be obtained from the instrument manufacturer and SEMI E43. The measurement configuration is shown in Figure 2.

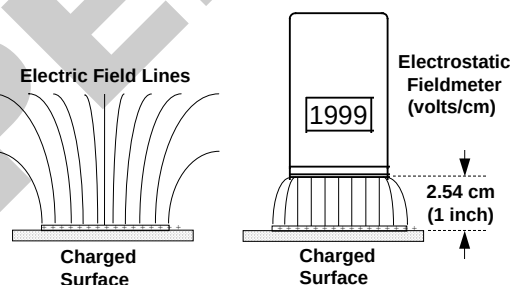


Figure 2
Electrostatic Field Measurement

7.4 For small objects or surface areas, an electrostatic voltmeter is appropriate.

8 Safety Precautions

8.1 *Personnel* — Static charges can create safety hazards during some semiconductor production processes.

8.1.1 ESA, ESD, and EMI events that result in the jamming or breakage of product in high-speed equipment may create a personnel hazard.

8.1.2 ESD events that produce sparks must be prevented in areas that use flammable or explosive chemicals or gases.

8.1.3 ESD events to personnel are usually not harmful, but they may result in an unwanted reflex, or “startle” reaction. This reflex may create a personnel hazard, particularly in the vicinity of moving equipment or where caustic chemicals are in use.

8.1.4 EMI resulting from ESD events may cause unpredictable behavior of robotics or other moving equipment that put personnel at risk.

8.1.5 It may be necessary to use additional static charge control methods, beyond those used inside the equipment, to minimize these personnel hazards.

8.2 *Measurement Safety* — Users should exercise caution while making static charge measurements in the vicinity of moving parts of production equipment, or in areas where static potentials on ungrounded conductors may exceed 30,000 V. Refer to SEMI E43 for additional measurement safety considerations.

9 Test Specimen

9.1 The user, material supplier, facility designer/builder, and equipment manufacturer should agree upon and document:

- Type(s) of testing to be performed
- Location of the testing (e.g., in a test chamber or in the actual use location)
- Who will do the testing
- Number and type of test samples
- Number of measurements
- Acceptable test results

9.2 The user, material supplier, facility designer/builder, and equipment manufacturer should agree upon and document all appropriate environmental conditions (e.g., temperature, humidity, dew point, airflow).

9.3 The user, material supplier, facility designer/builder, and equipment manufacturer should agree upon and document the operating history of equipment prior to, or during testing (e.g., warm-up time, type of carrier, number of products processed, operating speed).

10 Preparation of Apparatus and Sample

10.1 Depending on the type of testing to be done, consult the appropriate testing document for apparatus and sample preparation (see § 4).

11 Calibration and Standardization

11.1 Depending on the type of testing to be done, consult the appropriate testing document for apparatus calibration and verification (see § 4).

12 Procedures

12.1 See §§ 6 and 7 and the appropriate test methods of § 4.

12.2 ESD Damage

12.2.1 Users should establish product damage thresholds for their products. Measurement methods for integrated circuits are described in SEMI E78 Related Information 1 and the documents contained in § 4. Appropriate measurement methods for ESD damage to wafers, reticles, and other items may be adapted from the instrumentation used in these test methods.

12.2.2 In place of using the test methods referenced in ¶ 12.2.1, users may decide to follow the recommendations for acceptable electrostatic levels contained in ¶ 12.5 Table 1, which are based on product and reticle geometry. See Appendix 1 for more information.

12.2.3 Measurements of ESD damage levels are made in units of coulombs, or more conveniently in nanocoulombs ($\text{nC} = 10^{-9}$ coulombs).

12.2.4 The Faraday Cup method is used to determine the static charge levels on products, carriers and equipment parts. See ¶ 7.1. Each item should be transported to the Faraday Cup in a way that does not alter its charge level. Consult the measurement equipment manufacturer’s instructions for recommendations on how to achieve this.

12.3 Electrostatic Field

12.3.1 Users should work with cleanroom designers, material suppliers, equipment manufacturers and reticle suppliers to determine ambient particle levels, product exposure times during processing, and reticle damage levels due to electric field.

12.3.2 Electrostatic field measurements should be made at a minimum on all surfaces within the facility that will come within 30.5 cm (12 inches) of ESD sensitive items. Typical surfaces to measure would include construction materials, furniture, personnel, products, carriers, and equipment surfaces.

12.3.3 Measurements should be made in at least three different locations on any item. Locations should be separated by approximately three times the distance between the measuring instrument and the measurement location. For most electrostatic fieldmeters measuring at 25.4 mm (1 inch), the measurement locations will be 76.2 mm (3 inches) apart. Refer to SEMI E43 for additional measurement considerations.

12.3.4 Measurements of electrostatic field are expressed in V/cm or V/inch. Typically, five measurements should be sufficient to demonstrate compliance with the selected electrostatic level.

12.4 All elements of the semiconductor factory, including but not limited to construction materials, furniture, equipment, personnel, product, reticles, carriers, and transport and packaging materials, should meet the following electrostatic levels shown in ¶ 12.5 Table 1 for protection from problems caused by static charge.

Table 1 Recommended Facility Electrostatic Levels

Year Node	Electrostatic Discharge nC	Electrostatic Field, V/cm V/inch	
2000 180 nm	2.5–10	200	500
2002 130 nm	2.0	150	375
2004 90 nm	1.0	100	250
2006 70 nm	0.6	80	200
2007 65 nm	0.5	70	175
2009 50 nm	0.3	55	140
2010 45 nm	0.25	50	125
2013 32 nm	0.125	35	88
2015 25 nm	0.08	28	70
2018 18 nm	0.04	20	50

12.5 It is desirable in this document to avoid confusion with SEMI E78 recommended equipment electrostatic levels, as well as to synchronize with the major technology nodes in the International Technology Roadmap for Semiconductors (ITRS). Recommendations for acceptable facility electrostatic levels are listed in Table 1 and given for the major technology nodes of the ITRS 2005, which relate to the size of the features on the wafer. Semiconductor manufacturing facilities should meet the levels shown in Table 1 for protection from problems caused by static charge.

12.5.1 Since many decisions to use static control materials will result in the permanent installation of these materials, users may want to consider the eventual use of their semiconductor facility in selecting the acceptable

electrostatic level. For example, at startup the facility may be processing at 180-nm geometry, but in five years it is anticipated to be at 90-nm. The facility may need to be designed for the limits recommended for the 90-nm use.

12.5.2 The levels in Table 1 assume that the manufacturing facility is processing silicon semiconductors. Manufacturers of specialized components may need to choose lower levels. Examples are manufacturers of gallium arsenide semiconductors or magneto-resistive (MR) disk drive read heads, those experiencing significant losses due to contamination, or those using specialized equipment.

12.6 The levels listed in Table 1 have been determined as the result of an analysis of working conditions, or experiments done in operating semiconductor facilities. Justifications for these levels are found in Appendix 1. The actual levels to be used for any production area may be decided by agreement between the user and designer/builder of the facility.

12.7 Other levels may be appropriate under specific operating conditions and for specific devices.

13 Calculations

13.1 A series of five measurements should be made. The average of the five measurements should not exceed the recommended level. No measurement should exceed two times the recommended level.

14 Reporting Results

14.1 Data records should contain the following information:

- Description of the materials or equipment under test including model and serial numbers,
- Description of the factory operating conditions and environment,
- Measurement equipment and last calibration date,
- Description of objects measured and measurement locations,
- Humidity, temperature, and dew point at measurement location when measurements were made,
- Results of measurements,
- Personnel making the measurements, and
- Any other relevant comments.

15 Test Method Precision and Accuracy

15.1 The test methods referenced in this document do not guarantee precise measurements of static charge levels. Similarly, maximum static charge levels recommended in this document are not stated as precise requirements. Accuracy of approximately $\pm 20\%$ is acceptable in all measuring instrumentation. At low static charge levels, or for more accurate measurements, alternative instrumentation and test methods may be needed.

15.2 To evaluate low levels of electric field strength or the voltage on an object, use an electrostatic fieldmeter or electrostatic voltmeter with the resolution and accuracy required. Under appropriate conditions, electrostatic voltmeters exhibit a high degree of accuracy and stability that is independent of the distance from the charged object. The electrostatic voltmeter probe can be located very close to a charged surface without arc-over, and it is able to resolve the field from a small charged object.

APPENDIX 1

DEVELOPING THE RECOMMENDATIONS FOR ELECTROSTATIC LEVELS

NOTICE: The material in this appendix is an official part of SEMI E129 and was approved by full letter ballot procedures on May 16, 2006.

A1-1 Recommended Levels

A1-1.1 The recommended charge and electrostatic field levels in this guide are not based on specific protection thresholds for individual devices or process tools. Rather, their aim is to classify the types of ESD events or static levels that are likely to be of concern. Facility designers and users should determine the types of events that are of most concern to their products and processes, to apply this guide to their needs. Information on specific device damage thresholds is best determined on an individual basis.

A1-2 Justification of Guide Recommendations in § 12.5 Table 1

A1-2.1 Recommendations for ESD Damage

A1-2.1.1 An analysis of the recommended levels to protect semiconductor devices is found in Appendix 1 of SEMI E78. Related Information 1 of SEMI E78 discusses test methods for determining ESD damage thresholds for semiconductor devices. Devices are qualified according to the highest ESD stresses they can withstand without measurable change in their operating parameters. This section attempts to develop guide recommendations for minimizing ESD damage based on those discussions in SEMI E78.

A1-2.1.2 The information contained in SEMI E78 was developed with respect to semiconductors handled by equipment. It was current when published in 1998. Device damage thresholds continue to decrease as geometries get smaller, and although the classification systems discussed in SEMI E78 have not changed, more devices are falling into the more sensitive classifications.

A1-2.1.3 It is desirable to harmonize this document with SEMI E78 and the ITRS to avoid confusion with SEMI E78 recommended equipment electrostatic levels, as well as to synchronize with the technology nodes in the ITRS. Recommendations for acceptable static charge levels are listed in ¶ 12.5 Table 1 and given for the major technology nodes of ITRS 2005, which relate to the size of the features on the wafer.

A1-2.2 Charge Levels for ESD Damage

A1-2.2.1 Related Information § R1-1 discusses test methods for determining ESD damage thresholds for semiconductor devices. Devices are qualified according to the highest ESD stresses they can withstand without measurable change in their operating parameters. This section attempts to develop guide recommendations for minimizing ESD damage based on the discussion in Related Information § R1-1.

A1-2.2.2 As discussed in Related Information ¶ R1-1.3, ESD Simulator testing uses different capacitances for each model. For Human Body Model (HBM) it is 100 pF, for Machine Model (MM) it is 200 pF, and for Charged Device Model (CDM) it depends on the capacitance of the actual device being tested. In any case, it is charge (charge = voltage × capacitance) that damages the device. It would seem appropriate, therefore, that the guide recommendations in ¶ 12.5 Table 1 be stated in units of charge (e.g., nC).

A1-2.2.3 Based on industry testing reflected in device data sheets, there appears to be a wide range for ESD immunity in semiconductor devices, and it depends on the type of ESD simulator used. HBM-type ESD discharges are due to personnel handling and not likely to occur within equipment. Charged equipment parts contacting devices (i.e., MM) and charged devices contacting machine parts (i.e., CDM) are the most likely causes of ESD damage to devices in equipment.

A1-2.3 Industry Device Damage Levels

A1-2.3.1 The recommended electrostatic levels are based on the following industry classifications. Each of the test methods, (i.e., HBM, MM, and CDM) have a set of qualification levels defined. These are contained in Tables A1-1, A1-2, and A1-3 below.

A1-2.4 Guide Recommendations

A1-2.4.1 At the 180 nm technology node for the year 2000, it is assumed that devices (although some may withstand higher levels of ESD) pass testing at HBM Class 0 (250 V × 100 pF = 25 nC), MM Class M1 (100 V × 200 pF = 20 nC), and CDM Class C3 (500 V × 10 pF device capacitance = 5.0 nC).