SEMI F47-0706
SPECIFICATION FOR SEMICONDUCTOR PROCESSING EQUIPMENT VOLTAGE SAG IMMUNITY

This standard was technically approved by the global Facilities Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on May 16, 2006. It was available at www.semi.org in June 2006. Originally published September 1999; Previously published February 2000.

NOTICE: This document was completely rewritten in 2006. This document replaces SEMI F47-0200 *and* SEMI F42-0600.

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1 Purpose

1.1 Semiconductor factories require high levels of power quality due to the sensitivity of equipment and process controls. Semiconductor processing equipment is especially vulnerable to voltage sags. This specification defines the voltage sag immunity required for semiconductor processing, metrology, and automated test equipment. This specification strikes a balance between voltage sag immunity and increased equipment cost.

NOTE 1: The requirements and recommendations in this international specification were developed to satisfy semiconductor industry needs. While differing from other generic requirements, this industry-specific set of requirements and recommendations is not in conflict with known generic equipment regulations from other regions or generic equipment specifications from other organizations.

NOTE 2: To minimize design effort and testing, this revision aligns SEMI F47 test methods with applicable IEC standards, while retaining the previous SEMI F47 test levels. It also incorporates knowledge gained in the first five years of experience with this specification.

2 Scope

2.1 This specification sets minimum voltage sag immunity requirements for equipment used in the semiconductor industry. Immunity is specified in terms of voltage sag depth (in percent of nominal voltage remaining during the sag) and voltage sag duration (in cycles or seconds). This specification also sets procurement requirements, test methods, pass/fail criteria, and test report requirements.

2.2 The primary focus of this specification is semiconductor processing equipment including but not limited to the following types:

- Etch equipment (Dry & Wet)
- Film deposition equipment (CVD & PVD)
- Thermal equipment
- Surface prep and clean equipment
- Photolithography equipment (Scanner, Stepper & Tracks)
- Ion Implant equipment
- Metrology equipment
- Automated test equipment
- Chemical Mechanical Polishing/Planarization equipment

2.2.1 The secondary focus of this specification is subsystems and components that are used in the construction of semiconductor processing equipment, including but not limited to:

- Power supplies
- Radio frequency generators and matching networks
- Ultrasonic generators
- Computers and communication systems
- Robots and factory interfaces
- AC Contactor coils and AC relay coils
- Chillers and cryo pumps

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- Pumps and blowers
- Adjustable speed drives

2.3 This specification applies to semiconductor processing equipment to include the equipment mainframe and all subsystems whose electrical power is directly affected by the operation of the equipment's EMO (emergency off) system.

2.4 *Grandfather Clause* — Equipment, subsystems, and components that were tested or certified under the previous version of this specification, prior to the publication date of this specification, do not require re-testing or re-certification until hardware or software design changes that could affect voltage sag immunity are implemented.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 Not included in this set of requirements and recommendations are over-voltage conditions (voltage swells), high frequency impulse events, and other power disturbances. If necessary, the Information Technology Industry Council (ITIC) curve contained in IEEE 1100 and SEMI E51 can be used to specify additional requirements outside the scope of this specification.

3.2 This specification does not address wafer quality variations that may be caused by voltage sags. It is recommended that equipment manufacturers consider the effects of voltage sags on their equipment processes. If voltage sags that are shallower and/or shorter than those in Table 1 can result in known wafer quality problems, it is recommended (but not required) that a power quality sensor coupled to a notification scheme be included in the equipment design.

3.3 This specification addresses voltage sag immunity of semiconductor processing equipment. Voltage sag immunity of factory systems, and electric utility voltage sag performance, are covered in other related standards.

3.4 This is a performance specification. It does not address design issues related to safety, which are covered elsewhere in SEMI Standards (see SEMI S2).

3.5 Safety-related systems may require voltage sag immunity for conditions up to and including full power failure. Further, if hazards could result from voltage sags deeper and/or longer than those considered in this specification, provision should be made to negate or eliminate such hazards.

3.6 Conflicts between this specification and safety requirements (such as SEMI S2) that cannot be otherwise resolved shall be decided in favor of safety requirements.

3.7 This specification does not pre-empt or override international, national, and local codes that may apply in different facility locations. Such codes, regulations, and laws should be consulted to ensure that equipment meets regulatory requirements in each location.

4 Referenced Standards and Documents

4.1 *SEMI Standards*

SEMI E51 — Guide for Typical Facilities Services and Termination Matrix

SEMI S2 — Environmental, Health, and Safety Guideline for Semiconductor Manufacturing Equipment

4.2 *IEEE Standards*[1]

IEEE 1100 — IEEE Recommended Practice for Powering and Grounding Sensitive Electronic Equipment (IEEE Emerald Book)

IEEE 1250 — IEEE Guide for Service to Equipment Sensitive to Momentary Voltage Disturbances

4.3 *IEC Standards*[2]

IEC 61000-4-11 — Testing and Measurement Techniques – Voltage Dips, Short Interruptions and Voltage Variations Immunity Tests (for equipment rated at 16 amps per phase or less)

1 Institute of Electrical and Electronics Engineers, IEEE Operations Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, New Jersey 08855-1331, USA. Telephone: 732.981.0060; Fax: 732.981.1721, Website: www.ieee.org

2 International Electrotechnical Commission, 3, rue de Varembé, Case Postale 131, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.919.02.11; Fax: 41.22.919.03.00, Website: www.iec.ch

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IEC 61000-4-34 — Testing and Measurement Techniques – Voltage Dips, Short Interruptions and Voltage Variations Immunity Tests for Equipment with Input Current more than 16 A per Phase.

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *assist* — a response to an unplanned stoppage that occurs during an equipment cycle in which all three of the following conditions apply:

- The stopped equipment cycle is resumed through external intervention (e.g., by an operator or user), and
- There is no replacement of a part, other than specified consumables, and
- There is no further variation from specification of equipment operation.

5.2 *failure* — any unplanned stoppage or variance from the specification of equipment operations other than assists.

5.3 *interrupt* — any equipment assist or equipment failure.

5.4 *voltage sag immunity* — the ability of equipment to withstand momentary electric power interruptions or sags [IEEE 1250 ride-through capability].

5.5 *voltage sag* — an rms reduction in the ac voltage, at the power frequency, for durations from a half cycle to a few seconds [IEEE 1100].

NOTE 3: The IEC terminology for this phenomenon is voltage dip.

6 Using this Specification for Procurement

6.1 Semiconductor manufacturers may use this document to specify voltage sag immunity requirements to semiconductor process equipment manufacturers.

6.2 Semiconductor process equipment manufacturers may use this document to specify voltage sag immunity requirements to their subsystem and component suppliers.

6.3 Orders for semiconductor processing equipment should specify:

a) This document number and date of publication.

b) (Optional) The requirement for a Certificate per ¶ 7.9 of this document.

c) (Optional) The requirement for a Test Report per ¶ 7.10 of this document.

d) (Optional) Whether a third-party Certificate is required, or if self-certification is acceptable.

6.4 Orders for subsystems and components should specify:

a) This document number and date of publication.

b) One of the pass/fail criteria from ¶ 7.8.2 of this document – see ¶ R1-6 for advice.

c) (Optional) The requirement for a Test Report per ¶ 7.10 of this document.

d) (Optional) Whether a third-party Certificate is required, or if self-certification is acceptable.

7 Requirements

7.1 *Required Voltage Sag Immunity* — Semiconductor processing equipment, subsystems, and components are required to be immune to the voltage sag levels and durations set forth in Table 1.

Table 1 Required Voltage Sag Immunity

Sag depth[#1]	*Duration at 50 Hz*	*Duration at 60 Hz*
50%	10 cycles	12 cycles
70%	25 cycles	30 cycles
80%	50 cycles	60 cycles

#1 Sag depth is expressed in percent of remaining nominal voltage. For example, during a 70% sag on a 200 volt nominal system, the voltage is reduced during the sag to 140 volts (not 60 volts).

7.2 *Sag Immunity Test Methods* — Semiconductor processing equipment, subsystems, and components shall be tested for voltage sag immunity according to the methods set forth in IEC 61000-4-11 (for equipment rated at

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