

SEMI G1-96

SPECIFICATION FOR CerdIP PACKAGE CONSTRUCTIONS

This Standard was technically approved by the Assembly & Packaging Global Technical Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee. Available at www.semi.org in 1996; originally published in 1990.

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1 Purpose

1.1 This Specification defines the materials and acceptance criteria for the components (bases, window frames, and caps) or sub-assemblies (leadframes mounted in a sandwich between bases and window frames) used for CerDIP package constructions.

NOTE 1: Materials and acceptance criteria for leadframes, purchased separately for these constructions, are described in SEMI G2.

2 Scope

2.1 This Specification applies to all CerDIP (dual-in-line) packages which have either:

- A leadframe sandwiched between two ceramic pieces—the base and a window frame—and sealed by a solder glass layer, and a cap with a similar seal; or,
- A leadframe mounted into a solder glass layer on a ceramic base, and a cap with a similar glass seal layer.

NOTE 2: The base, leadframe, and, if required, the window frame may be purchased as separate components or as a subassembly.

2.2 Order of Precedence

2.3 To avoid conflicts, the order of precedence when ordering components or subassemblies for CerDIP packages shall be as follows:

- Purchase Order
- User’s Package Drawings
- This Specification
- Reference Standards and Documents
- Related Documents

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Units

3.1 This Specification uses U.S. Customary (inch pound) units as the prime unit.

4 Referenced Documents

4.1 SEMI Standards and Safety Guidelines

SEMI G2 — Specification Metallic Leadframes for CerDIP Packages

SEMI G20 — Specification Lead Finishes for Plastic Packages (Active Devices only)

SEMI G23 — Test Method Measuring the Inductance of Package Leads

SEMI G24 — Test Method Measuring the Lead-to-Lead and Loading Capacitance of Package Leads

SEMI G25 — Test Method Measuring the Resistance of Package Leads

SEMI G30 — Test Method Junction-to-Case Thermal Resistance Measurements of Ceramic Packages

4.2 ANSI Standards¹

ANSI Y14.5M — Dimensioning and Tolerancing

4.3 JEDEC Publications²

JEDEC Publication 95 — Registered and Standard Outlines for Semiconductor Devices

4.4 Military and Federal Specifications³

MIL-STD-105D — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

MIL-STD-1835 — Microcircuit Case Outlines

MIL-I-38535 — General Specifications for Microcircuits

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Definitions

5.1.1 *blister (bubble) metallization* — an enclosed, localized separation of the metallization from its base material (such as ceramic or other metallization layer component) that does not expose the underlying layer.

5.1.2 *burr* — an adherent fragment of parent material at a component edge. In leadframes, the metal burr, due to the stamping operation, may be in the horizontal or vertical direction to the surface. In ceramic packages, this type of characteristic is called a fin.

5.1.3 *camber (ceramic)* — arching of a nominally flat ceramic body.

5.1.4 *chip* — a region of material missing from a component (e.g., ceramic from a package, or solder from a preform). The region does not progress completely through the component and is formed after the component is manufactured. Chip size is defined by its length, width, and depth from a projection of the design planform. Also called chipout. (Refer to Figure 1.)

¹ American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, <http://www.ansi.org>

² Joint Electron Device Engineering Council, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201, USA; Telephone: +1.703.907.7560, Fax: +1.703.907.7583, <http://www.jedec.org>

³ United States Military Standards, Available through the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120-5099, USA; Telephone: +1.215.697.3321.

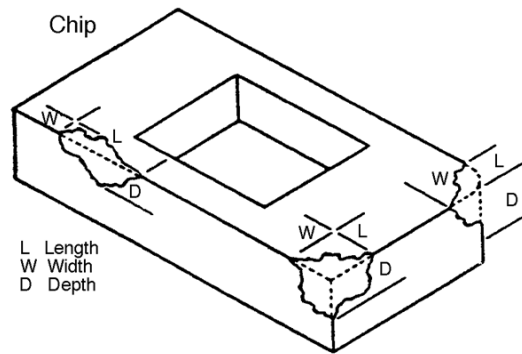


Figure 1

5.1.5 *crack* — a cleavage or fracture that extends to the surface of a semiconductor package or solder preform. The crack may or may not pass through the entire thickness of the package or preform.

5.1.6 *critical seal area* — on a semiconductor package, the area bounded by the shortest nominal design distance from the largest cavity, usually the wire bond cavity, to the edge of the package or ceramic layer forming the seal area. (Refer to Figure 2.)

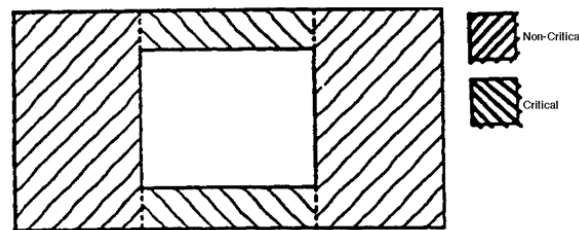


Figure 2
Critical and Non-Critical Seal Area

5.1.7 *fin* — on a ceramic package or cap, a fine feathery-edged projection of parent ceramic material on the corner of the ceramic body.

5.1.8 *foreign material* — an adherent particle that is not parent material of the component. Adherence means that the particle cannot be removed by an air or nitrogen blast at 20 psi.

5.1.9 *glass flow* — on a semiconductor package or cap, the heating process which just removes all the screen printing mesh marks in the sealing glass when viewed at 10× magnification.

5.1.10 *glass void* — the absence of a sealing glass layer from a designated area.

5.1.11 *metallization void* — the absence of a clad, evaporated, plated, or screen-printed metal layer or braze from a designated area.

5.1.12 *non-critical seal area* — on a semiconductor package that uses a lid, cap, or cover to effect the seal, the area of the sealing surface outside the critical sealing area. (Refer to Figure 2.)

5.1.13 *overhang* — on a semiconductor package, the horizontal extension of the sealing glass past the vertical wall of a cavity cut into the ceramic layer on which the glass is printed. (Refer to Figure 3.)

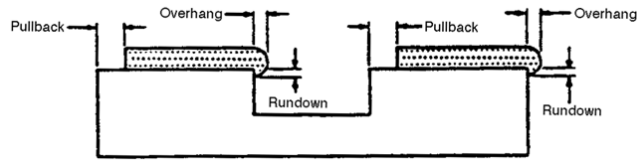


Figure 3
Glass Misalignment

5.1.14 *peeling (flaking)* — any separation of a plated, vacuum-deposited, or clad metal layer from the base metal of a leadframe, pin heatsink, or seal ring, from an underplate or from a refractory metal on a ceramic package. Peeling exposes the underlying metal.

5.1.15 *projection* — on a semiconductor package (plastic or ceramic) leadframe or preform, an irregularly raised portion of a surface indigenous to the parent material.

5.1.16 *pullback* — on a semiconductor package, the linear distance between the edge of a cavity cut into a ceramic layer and the first measurable glass or metallization layer interface coated onto the top surface of that layer. The total pullback may be the result of the high-temperature processing required to manufacture the package or to coat the surface. It may also be the result of design considerations. (Refer to Figure 3.)

5.1.17 *rundown* — on a semiconductor package, the linear distance from the upper surface of a ceramic cavity layer to the bottom point of the overhang into the cavity, of a sealing glass or metallization layer that has been screened onto that surface. (Refer to Figure 3.)

5.1.18 *seal area* — on a semiconductor package, the area designated for sealing a cover or lid to a cofired ceramic package, to a cap to a cer-pack base.

5.1.19 *void* — an absence of metallization or glass from a designated metallized or glassed area on a ceramic surface.

6 Ordering Information

6.1 Purchase orders for CerDIP components or sub-assemblies furnished to this Specification shall include the following items:

6.2 Current drawing revision detailing:

6.2.1 All dimensions and tolerances per ANSI Y14.5M practices

6.2.2 Type and color of ceramic

6.2.3 Type and thickness of glass

6.2.4 Type and thickness of die pad metallization

NOTE 3: If subassemblies are purchased, the leadframe details shall be as described in SEMI G2. In some cases, unlike the frames described in SEMI G2, the leadframes may also have a die-attach pad. If required, the external lead plating requirements for these sub-assemblies shall also be specified. (Refer to SEMI G20 for general details of lead finishes.) If sub-assemblies are purchased, leadframe inspection shall follow the requirements detailed in § 9.

6.3 *Incoming Inspection and Functional Tests* — Refer to §§ 9 and 10.

6.4 *Incoming Sampling Procedures* — Refer to § 11.

6.5 *Packaging and Marking Requirements* — Refer to § 12.

6.6 *Vendor Certification Requirements* — Refer to § 13.

6.7 Any additions to, or variations from, this Specification.

7 Dimensions

7.1 The components or sub-assemblies described in this Specification shall produce packaged devices that conform to the outline dimensions and lead numbering for CerDIP package constructions detailed in:

- JEDEC Publication 95 and
- MIL-STD-1835.

7.2 Package manufacturing tolerances shall be agreed upon between user and supplier and detailed in the drawings.

7.3 Typical dimensions and tolerances for standard bases and caps are shown in the Appendices at the end of this Specification.

8 Materials

8.1 The definitions defect criteria and functional tests described in this Specification relate to package components made with the following materials:

8.2 Bases, Window Frames, and Caps

8.2.1 *Material* — Ceramic with 90% alumina, minimum content.

8.2.2 *Color* — Black, dark brown, or dark violet.

8.3 Sealing Material

8.3.1 *Material* — Solder glass designed to seal metal (typically Iron-Nickel-Cobalt alloy per MIL-M-38150, Type A or Iron-Nickel alloy per MIL-M-38150 Type B) to ceramic.

8.4 Die-Attach Pad

8.4.1 *Material* — Thick film gold or other specified material.

8.5 Leadframe

8.5.1 Leadframes, whether purchased as component or in sub-assemblies, shall conform to the requirements of SEMI G2 as required.

9 Defect Limits

9.1 The following defects shall be cause for rejection if the limits shown are exceeded:

NOTE 4: The criteria apply to purchased components and pre-assemblies, as applicable, or, where applicable, to units assembled by the user to process conditions agreed upon between the user and supplier.

9.2 Ceramic Components

9.2.1 *Cracks* — Any crack.

9.2.2 *Chips* — Refer to Figures 1 and 2.

9.2.2.1 *Corner Chips* — 0.030 in. (0.762 mm) × 0.030 in. (0.726 mm) × 25% of the package element thickness.

9.2.2.2 *Edge Chips* — 0.100 in. (2.54 mm) × 0.030 in. (0.726 mm) × 25% of the package element thickness.

9.2.2.3 *Critical Seal Area* — Chips shall not reduce the critical seal path, at any point, more than 30%. No more than four chips are allowed in this area, regardless of loss of seal length.

9.2.3 Burrs, Projection (Fins), and Blisters

9.2.3.1 *Bases, Caps, and Window Frames* — 0.005 in. (0.127 mm) maximum allowable dimension in the plane of the component, or greater than 0.003 in. (0.076 mm) in height.

9.2.3.2 *Die-Attach Surface (on Base Ceramic)* — 0.005 in. (0.127 mm) dimension in the plane of the component, or greater than 0.001 in. (0.254 mm) above the surface of the metallization excluding a zone, 0.010 in. (0.254 mm) wide, around the periphery of the cavity.

9.2.4 *Camber* — Shall be agreed upon between user and supplier and specified on the component or subassembly drawing. Standard limits shall be 0.003 in. (0.003 mm), maximum, with a minimum allowable camber of 0.002 in. (0.051 mm).

9.2.5 *Foreign Material* — 0.020 in. (0.508 mm) maximum allowable surface dimension or 0.005 in. (0.127 mm) in height. No more than three sites allowed and a minimum separation of 0.030 in. (0.762 mm) between sites.

9.3 Glass Sealant

9.3.1 *Chips and Voids* — 0.010 in. (0.025 mm) maximum allowable dimension. In the critical seal, there shall be no more than four acceptable chips or voids. In critical and non-critical seal areas, there shall be no voids after a glass flow cycle.

9.3.2 *Glass Misalignment* — After glass flow on components, refer to Figure 3, or on subassemblies.

9.3.2.1 *Glass Overhang* — 0.015 in. (0.381 mm) maximum extension from the ceramic edge.

9.3.2.2 *Glass Rundown* — 50% of the package element thickness.

9.3.2.3 *Glass Rundown into the Die-Attach Cavity* — 0.010 in. (0.254 mm) maximum extension from the ceramic surface into the cavity.

9.3.2.4 *Glass Pullback (After Glass Flow)* — Refer to Table 1 and Figure 3.

Table 1 Maximum Allowable Pullback

<i>Area of Package</i>	<i>Package Row Spacing</i>	<i>Package Row Spacing</i>
	0.300 in. (7.500 mm) and 0.400 in. (10.16 mm)	0.600 in. (15.24 mm) and larger
Side external (critical seal area)	0.010 in. (0.254 mm)	0.015 in. (0.381 mm)
Side external (non-critical seal area)	0.015 in. (0.381 mm)	0.015 in. (0.381 mm)
End external	0.020 in. (0.508 mm)	0.020 in. (0.508 mm)
Side cavity	0.010 in. (0.254 mm)	0.015 in. (0.381 mm)
End cavity	0.010 in. (0.254 mm)	0.015 in. (0.381 mm)
Maximum allowable critical seal length reduction on any one side, as measured between the cavity and the external side	0.015 in. (0.381 mm)	0.020 in. (0.508 mm)

#1 Regardless of the maximum criteria noted in Table 1, the critical seal length at any point shall not be reduced any more than 30%.

9.3.2.5 *Foreign Material* — 0.020 in. (0.508 mm) maximum allowable surface dimension in the plane of the glass, but 0.010 in. (0.254 mm) in the critical seal area, with no more than three sites allowed and a minimum separation of 0.030 in. (0.762 mm) between sites.

9.4 *Die-Attach Cavity Metallization (On Ceramic Base)* — Excluding a 0.010 in. (0.254 mm) wide zone around the periphery of the cavity, the following criteria shall apply:

9.4.1 *Foreign Material, Including Glass Splatters* — 0.005 in. (0.130 mm) maximum in the plane of the metallization or greater than 0.001 in. (0.025 mm) in height with no more than three sites allowed and a minimum separation of 0.030 in. (0.763 mm) between sites.

9.4.2 *Metallization Nodules* — No more than three allowed. If the metallization is gold and gold-silicon eutectic die attach is to be used, the bumps may not exceed 0.010 in. (0.254 mm) in the surface dimension or 0.005 in. (0.130 mm) in height. If silver glass or resin bonding is to be used, the nodules shall be treated as foreign material per § 9.3.

9.5 Leadframe

NOTE 5: The criteria described in this section generally apply to leadframe inspection for purchased subassemblies. Where appropriate, the criteria may be used for sub-assemblies manufactured in-house with purchased components. For information on the criteria for leadframes purchased separately, refer to SEMI G2.

9.5.1 *Lead Bond Areas* — The minimum lead bond area on the lead tip is defined in Figure 4.