

SEMI G22-1296

SPECIFICATION FOR CERAMIC PIN GRID ARRAY PACKAGES

This Standard was technically approved by the Assembly & Packaging Global Technical Committee.

NOTICE: This Standard or Safety Guideline has an Inactive Status because the conditions to maintain Current Status have not been met. Inactive Standards or Safety Guidelines are available from SEMI and continue to be valid for use.

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1 Purpose

1.1 This Specification defines the acceptance criteria for cofired ceramic pin grid array packages.

2 Scope

2.1 This Specification includes the visual, dimensional, and functional requirements for the ceramics PGA package.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *United States Military Standards*¹

MIL-G-45204 — Gold Plating, Electrodeposited

MIL-PRF-38535 — Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

MIL-STD-1835 — Interface Standard for Microcircuit Case Outlines

MIL-STD-7883 — Brazing

QQ-N-290A — Nickel Plating

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Definitions

4.1.1 *blister (bubble) ceramic* — any separation within the ceramic which does not expose underlying ceramic material.

4.1.2 *blister (bubble) metal* — any localized separation within the metallized or between the metallization and ceramic which does not expose underlying metal or ceramic material.

4.1.3 *braz*e — an alloy with a melting point equal to or greater than 450°C.

¹ United States Military Standards, Available through the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120-5099, USA; Telephone: +1.215.697.3321.

4.1.4 *burr* — an adherent fragment of excess parent material, either horizontal or vertical, adhering to the component surface.

4.1.5 *chip* — a region of ceramic missing from the surface or edge of a package which does not go completely through the package. Chip size is given by its length, width, and depth from a projection of design plan form. (Refer to Figure 1.)

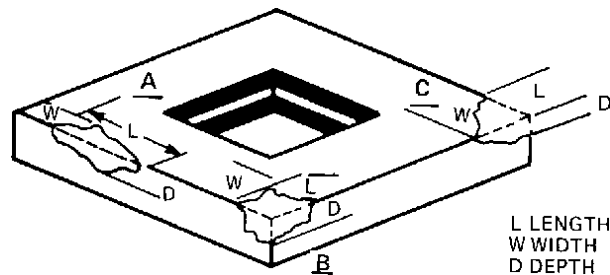


Figure 1
Chip Illustration

4.1.6 *cofired* — a process or technology for manufacturing products in which the ceramic and refractory metallizations are fired simultaneously.

4.1.7 *contact pad* — that metallized pattern that provides mechanical or electrical connection to the external circuitry.

4.1.8 *crack* — a cleavage or fracture that extends to the surface of a package. It may or may not pass through the entire thickness of the package.

4.1.9 *delamination* — the separation of the individual layers of the ceramic.

4.1.10 *die attach area* — a dimensional outline designated for die attach.

4.1.11 *discoloration* — any change in the color of the package plating or metallization as detected by the unaided eye which normally appears after the application of heat per ¶ 8.7.1.

4.1.12 *flatness* — the allowable deviation of a surface from a reference plane. The tolerance zone is defined by two parallel planes within which the surface must lie.

4.1.13 *footprint* — pin pattern.

4.1.14 *foreign material* — an adherent particle other than parent material of that component.

4.1.15 *isolation gap* — metal-free space between conductive areas.

4.1.16 *layer* — a dielectric sheet with or without metallization that performs a discrete function as part of the package.

4.1.17 *peeling (flaking)* — any separation of metallization from the base material that exposes the base material.

4.1.18 *pit* — any unspecified depression in the package.

4.1.19 *projection* — an adherent fragment of excess parent material on the component surface.

4.1.20 *pullback* — a dimension covering the linear distance between the edge of the ceramic and the first measurable metallization. (Refer to Figure 2.)

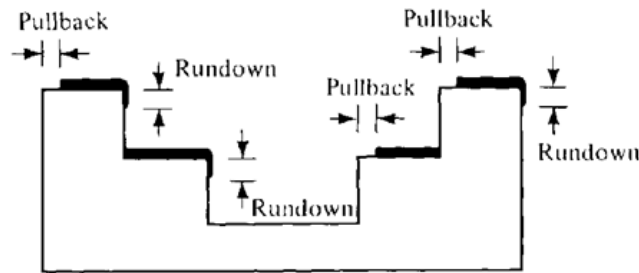


Figure 2
Metallization Misalignment

4.1.21 *rundown* — the linear distance down a vertical surface from the top to the point of maximum metallization overhang. (Refer to Figure 2.)

4.1.22 *seal area* — a dimensional outline area designated for either metallization or bare ceramic to provide a surface area for sealing.

4.1.23 *seating plane* — as defined by the standoff features or the package base plane if no standoff is used. (Refer to Figure 3.)

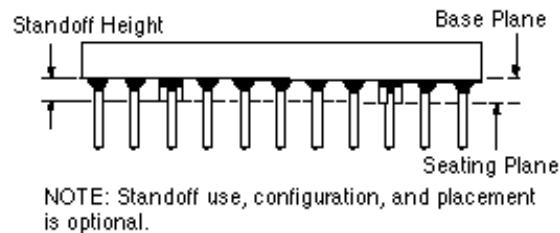


Figure 3
Seating Plane

4.1.24 *standoff* — the designed separation between the base plane and the seating plane created by a physical feature. Standoff use, configuration, and placement is optional. (Refer to Figure 3.)

4.1.25 *terminal* — metallization at the point of electrical contact to package internal circuitry.

4.1.26 *voids* — an absence of refractory metallization, braze, or plating material from a designated area greater than 0.051 mm (0.002 in.) in diameter.

5 Ordering Information

5.1 Purchase orders for pin grid array packages furnished to this Specification shall include the following items:

5.1.1 Drawing number and revision level

5.1.2 Certification requirements

5.1.3 Quantity

5.1.4 Reference to this Standard

5.1.5 Any exceptions to print or specifications

6 Dimensions and Permissible Variations

6.1 The dimensions of the pin grid array package shall conform to the SEMI Standards or to the customer drawing and be within the outline of the appropriate JEDEC standard. Refer to MIL-PRF-38535 and MIL-STD-1835.