

SEMI G42-0996 (Reapproved 1104) SPECIFICATION FOR THERMAL TEST BOARD STANDARDIZATION FOR MEASURING JUNCTION-TO-AMBIENT THERMAL RESISTANCE OF SEMICONDUCTOR PACKAGES

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1 Purpose

1.1 This document provides the requirements for a standard thermal resistance test board to be used in junction- to-ambient thermal resistance measurement of a semiconductor package under still- and forced-air condition as a referee method.

2 Scope

2.1 This document describes the thermal resistance test board for measurement of the following packages:

- Dual-In-Line Packages (DIP),
- Plastic Chip Carrier Package (PCC),
- Quad Flat Package (QFP),
- Pin Grid Array Package (PGA), and
- Ball Grid Array Package (BGA).

2.2 This document uses SI units.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 Information regarding the methods for measuring junction-to-ambient thermal resistance, the proper design and use of thermal test chips, and material specifications for printed circuit boards, can be found in the applicable documents listed below.

3.2 SEMI Standards

SEMI G32 — Guideline for Unencapsulated Thermal Test Chip

SEMI G38 — Test Method for Still- and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of Integrated Circuit Packages

3.3 Military Specifications¹

MIL-P-13949 — Material Specification for NEMA Grade G-10 Printed Circuit Board Material

MIL-STD-883C — Method 1012.1, Thermal Characteristics

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Definitions

4.1.1 *junction temperature, T_J* — in degrees Celsius is used to denote the temperature of the semiconductor junction in the microcircuit in which the major part of the heat is generated. Usually the measured junction temperature is only indicative of the temperature in the immediate vicinity of the element used to sense the temperature.

4.1.2 *junction-to-ambient thermal resistance, $R_{\theta JA}$* — in degrees Celsius/watt is the temperature difference between the junction and the ambient, divided by the power dissipation P_H .

4.1.3 *power dissipation, P_H* — in watts is the heating power applied to the device causing a junction-to-reference point temperature difference.

4.1.4 *temperature sensitive parameter, TSP* — is the temperature dependent electrical characteristic of the junction under test which can be calibrated with respect to temperature and subsequently used to detect the junction temperature of interest.

5 Ordering Information

5.1 The material required for making the thermal test board can be ordered through any electronic supply store.

¹ United States Military Standards, Available through the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120-5099, USA. Telephone: 215.697.3321

6 Requirements

6.1 General requirements regarding the materials used for test board, the specified physical dimensions of the test board and other necessary conditions are described in the following paragraphs:

6.1.1 Material Requirements

6.1.1.1 The test board material should be NEMA Grade G-10 or equivalent.

6.1.1.2 The conductor traces on the board must be copper and the total amount of copper should not exceed 20% of the surface area of the board.

6.1.1.3 The vias should be plated through.

6.1.1.4 External wire connections from the package leads to edge connector leads must be made with 24-gauge copper wire.

6.1.2 *Thermal Test Board Physical Dimensions and Layout* — Five separate boards are designed for the purpose of thermal measurements of different types of semiconductor packages.

6.1.2.1 Physical Dimensions

6.1.2.1.1 *Length* — 114.3 mm $\pm$ 0.254 (4.50 inches $\pm$ 0.01)

6.1.2.1.2 *Width* — 76.2 mm $\pm$ 0.254 (3.00 inches $\pm$ 0.01)

6.1.2.1.3 *Thickness* — 1.524 – 1.651 mm $\pm$ 0.127 mm (0.060 – 0.065 inches $\pm$ 0.005 inches)

6.1.2.2 Layout

6.1.2.2.1 *Dual-in-Line Packages or Sockets* (See Figure 1.)

- The vias shall be located on 2.54 mm (0.10 inch) centers $\pm$ 0.076 mm (0.003 inches) non-accumulative.
- The diameter of the vias shall be 1.143 mm (0.045 inches) $\pm$ 0.076 mm (0.003 inches).
- The location of the vias on the board shall be as shown in Figure 1.

6.1.2.2.2 *Chip Carrier Packages* (See Figure 2.)

- The copper traces shall be laid out on the PC board as shown in Figure 2. The traces are drawn on 1.27

mm (0.050 inch) centers $\pm$ 0.127 mm (0.005 inch) non-accumulative.

- The vias at the end of the copper traces shall be located on the 2.54 mm (0.10 inch) centers $\pm$ 0.076 mm (0.003 inch) non-accumulative.

6.1.2.2.3 *Quad Flat Packages (0.3, 0.4, 0.5, and 0.65 mm lead pitch) or sockets* (See Figures 3–6.)

- The copper traces shall be laid out on the PC board as shown in Figures 3–6. The traces are drawn in accordance with pitch and width as shown in Table 1.

Table 1 Trace Pitch and Width for QFP Package Boards

<i>Package Lead Pitch (mm)</i>	<i>Trace Pitch (mm)</i>	<i>Trace Width (mm)</i>
0.65	0.65 $\pm$ 0.05	0.35
0.5	0.5 $\pm$ 0.05	0.25
0.4	0.4 $\pm$ 0.04	0.2
0.3	0.3 $\pm$ 0.03	0.15

6.1.2.2.4 *Pin Grid Array Packages or Sockets* (See Figure 7.)

- The vias shall be located on 2.54 mm (0.10 inch) centers $\pm$ 0.076 mm (0.003 inches) non-accumulative.
- The diameter of the copper lead shall be 1.2 mm $\pm$ 0.046 mm and the hole shall be 0.95 mm $\pm$ 0.046 mm.
- The location of the vias on the board shall be as shown in Figure 7-1.

6.1.2.2.5 *Ball Grid Array Packages (1.5, 1.27, and 1.0 mm Ball Pitch)* (See Figure 8.)

- The copper traces shall be laid out on the PC board as shown in Figure 8-1. The traces and vias are drawn in accordance with configuration and dimension as shown in Table 2.
- The board shall be covered by resist as shown in Figure 8-2. The back side of the board shall not be covered by resist.

Table 2 Trace Dimension for BGA Package Boards

<i>Pad Pitch (mm)</i>	<i>Trace Radius, R (mm)</i>	<i>Solder Mask Opening Diameter Ø1 (mm)</i>	<i>Hole Diameter Ø 2 (mm)</i>	<i>Number of Pads</i>
1.5	0.9	0.6	0.2	33 x 33
1.27	0.8	0.6	0.35	39 x 39
1.0	0.6	0.45	0.3	49 x 49

6.1.2.2.6 Equivalent boards for other packages should follow guidelines similar to those described in Sections 6.1.2.2.1–6.1.2.2.5.

6.1.2.2.7 *Multi-Layer Board* — When measuring thermal resistance using a multi-layer board, the layer shall be constructed as shown in Figure 9. The inner pattern should have the clearance as shown in Figure 10 to isolate with via holes.

6.1.3 Mounting Guidelines

6.1.3.1 Example of package mounting on the boards is shown in Figures 11 and 12. Packages should be mounted such that the center line of the test board is coincidental with the center line of the package.

6.1.3.2 For DIP and CCP, the longer edge of the package should be closest to the long edge of the board.

6.1.3.3 For QFP, PGA, and BGA package board, the package should be mounted in the center of the board.

6.1.3.4 Packages must be mounted such that the standoff height above the board is as per JEDEC guidelines. In the case of a new package without such information available, a minimum of 0.127 mm (5 mil) air gap between the bottom surface of the package and the thermal test board is acceptable.

6.1.4 Mounting the Test Board for Still-Air $R_{\theta JA}$ Measurement

6.1.4.1 The test board should be mounted on a clamp as shown in Figure 13 through a suitable edge connector clamp.

6.1.4.2 The test board and the edge connector clamp are placed in a 0.0283 m³ (one cubic foot) enclosure as shown in Figure 13. The edge connector clamp height must be adjusted to ensure positioning of the package in the center of the chamber.

6.1.4.3 The electrical wire connections from the package are routed out of the one cubic foot enclosure

either through an edge connector or through small diameter holes in the box.

6.1.5 *Mounting the Test Board for Forced-Air $R_{\theta JA}$ Measurement* — Forced air $R_{\theta JA}$ measurements are performed in a wind tunnel whose diameter is 203.2 mm (8.00 inches). Details of the wind tunnel are given in SEMI G38.

6.1.5.1 The test board should be mounted inside the wind tunnel on an edge connector clamp as shown in Figure 14.

6.1.5.2 The test board is placed in the wind tunnel such that the longer edge of the package is in a vertical position (see Figure 14).

6.1.5.3 The longer edge of the package should face the direction of air flow.

6.1.5.4 The longer side of the package must meet the air front first, as shown in Figure 14.

6.1.5.5 Air may be forced through the wind tunnel by either blowing from one end or by suction. (Suction being preferred.)

6.1.5.6 The test board and the edge connector clamp are placed in the wind tunnel as shown in Figure 14. The edge connector clamp height must be adjusted to ensure positioning of the package in the center of the wind tunnel.

6.1.6 *Thermal Resistance Measurement Methods* — Methods for measuring $R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) of IC packages using thermal test chips have been described in SEMI G32 and SEMI G38, respectively. These methods or equivalent methods such as the use of switching techniques, as described in MIL-STD-883C, Method 1021.1, should be used for making thermal resistance measurements of IC packages using thermal test chips or IC devices.

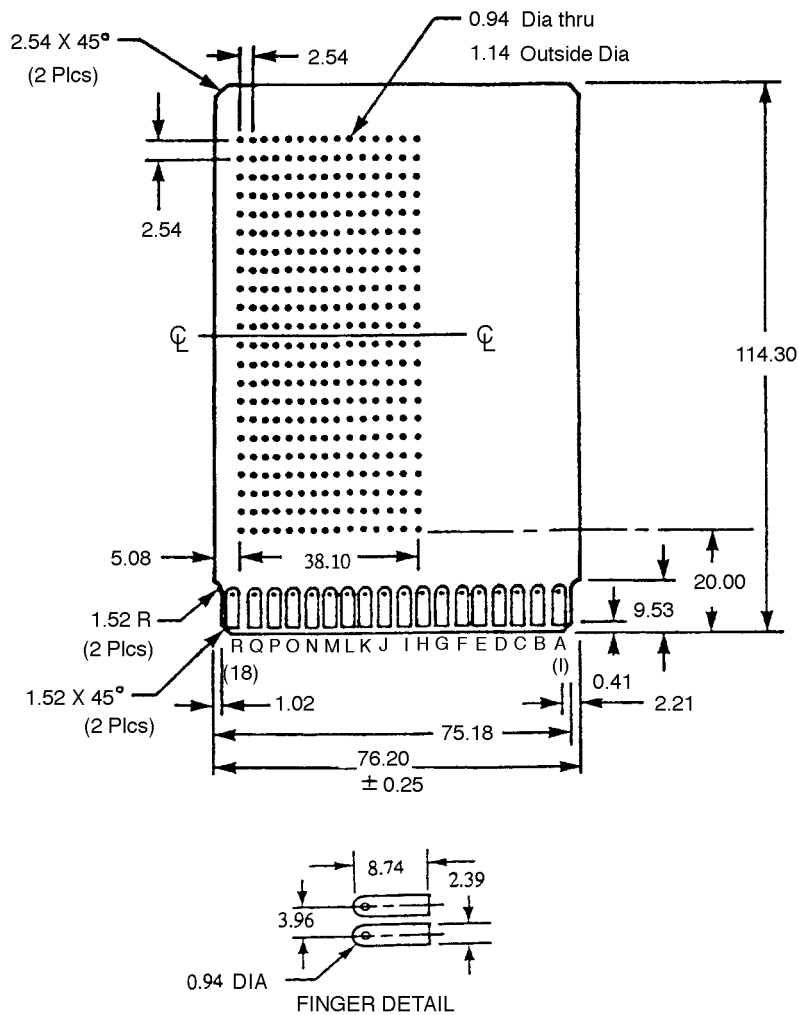


Figure 1
Thermal Test Board — Dual In-Line Package

(Unit: mm)

1. Material — Epoxy Glass 1.52–1.65 mm thickness, FR-4 (Green). Copper Clad. 28.3 g (1 Oz.) 1/1
2. Gold-Plated Fingers — 0.8 μ m Min. Thickness, 18 on Each Side
3. Fabricate — IPC-D-320, Class III
4. Tolerance — ± 0.1 mm (Unless noted)
5. Fingers on Component Side of Board — Designed as A thru R, Fingers on Solder Side of Board — Designated as 1 thru 18 (with 18 at Right When Viewing Face of Board)
6. All Holes Plated Thru
7. Mates with Dale Connector Part Number EB 7D-A18GFX or Equivalent

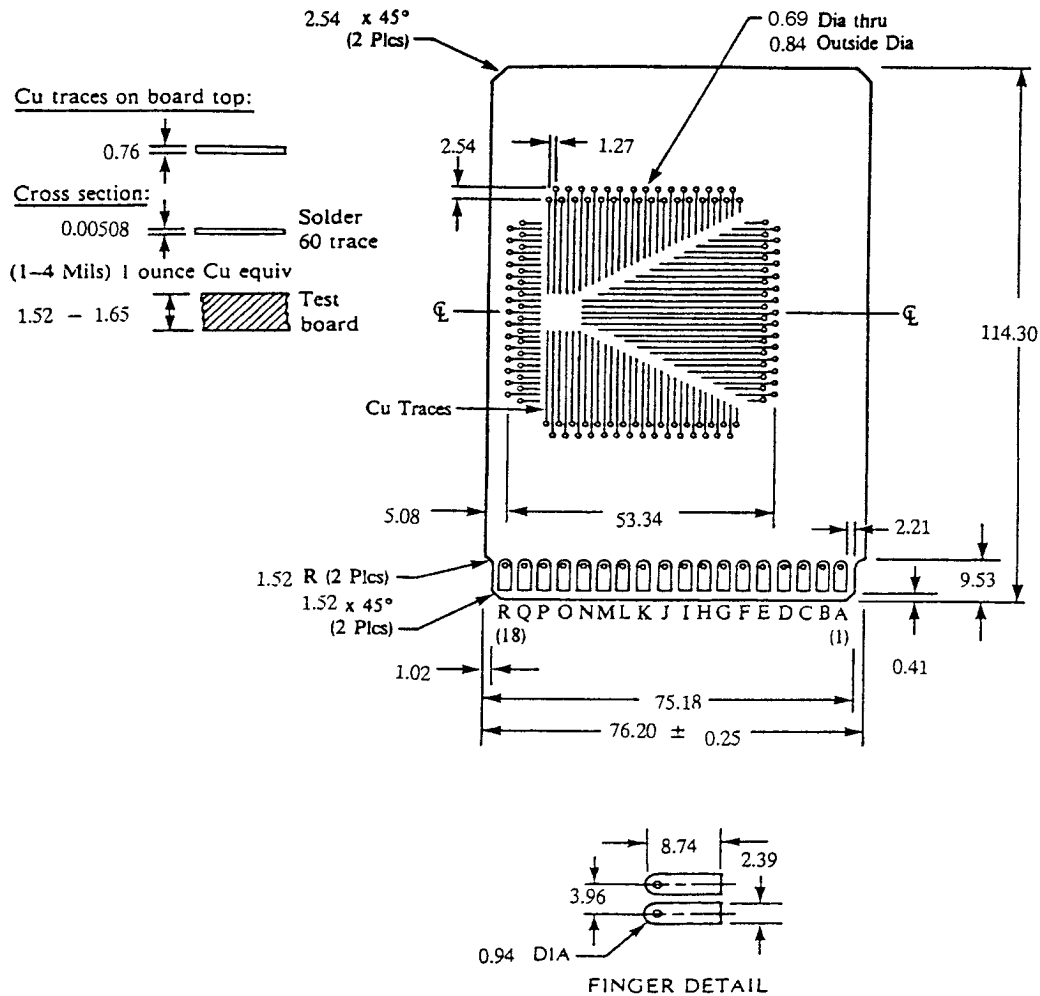


Figure 2
Thermal Test Board — PCC Packages

Unit: mm

1. Material — Epoxy Glass 1.52–1.65 mm thickness, FR-4 (Green). Copper Clad. 28.3 g (1 Oz.) 1/1
2. Gold-Plated Fingers — 0.8 µm Min. Thickness, 18 on Each Side
3. Fabricate — IPC-D-320, Class III
4. Tolerance — ± 0.1 mm (Unless noted)
5. Fingers on Component Side of Board — Designed as A thru R, Fingers on Solder Side of Board — Designated as 1 thru 18 (with 18 at Right When Viewing Face of Board)
6. All Holes Plated Thru
7. Mates with Dale Connector Part Number EB 7D-A18GFX or Equivalent