

SEMI G46-88

TEST METHOD FOR THERMAL TRANSIENT TESTING FOR DIE ATTACHMENT EVALUATION OF INTEGRATED CIRCUITS

1 Introduction

1.1 *Purpose* — Evaluation of semiconductor die attachment integrity using the thermal transient techniques as implemented by the Electrical Test Method on either thermal test chips or active devices.

1.2 *Rationale* — Steady state thermal response (or thermal resistance) and thermal transient response of discrete semiconductor devices and integrated circuits are sensitive to the presence of voids in the die attachment material between the semiconductor chip and package. These voids impede the flow of heat from the chip to the substrate (package). Due to the difference in the thermal time constants of the chip and package, the measurement of transient thermal response can be made more sensitive to the presence of voids than can the measurement of steady state thermal response. This is because the chip thermal time constant is generally several orders of magnitude shorter than that of the package. Thus, the heating power pulse width can be selected so that only the chip and the chip to substrate interface are heated during the pulse by using a pulse width somewhat greater than the chip thermal time constant, but less than that of the substrate. Heating power pulse widths ranging from 10 to 400 milliseconds have been found to satisfy this criterion. This enables the detection of voids to be greatly enhanced, with the added advantage of not having to heat sink the device under test. Thus, the transient thermal response technique is less time consuming than the measurement of thermal resistance for use as a manufacturing screen, process control or incoming inspection measure for die attachment integrity evaluation.

1.3 *References* — The following documents are recommended reading for reference and test method standard description purposes:

SEMI G32 — Unencapsulated Thermal Test Chip

MIL-STD-883C¹ — Method 1012, Thermal Characteristics

2 Definitions

The following symbols and terminology shall apply for the purpose of this test method.

2.1 V_F — the forward biased voltage of the diode junction within the Device-Under-Test (DUT) used for junction temperature sensing.

2.2 V_{Fi} — the initial V_F value before application of heating power.

2.3 V_{Ff} — the final V_F value after application of heating power.

2.4 ΔV_F — the change in the temperature sensitive parameter, V_F , due to the application of heating power to the DUT.

2.5 V_H — the voltage applied to the DUT during the heating time in order to cause power dissipation.

2.6 I_H — the heating current resulting from the application of V_H to the DUT.

2.7 P_H — the heating power pulse magnitude; product of V_H and I_H .

2.8 t_H — the duration of P_H (applied to the DUT).

2.9 I_M — the measurement current used to forward bias the temperature sensing diode junction for measurement of V_F .

2.10 t_{MD} — measurement delay time can be defined in one of two ways:

2.10.1 the time from the start of heating power (P_H) removal to the completion of the final V_F measurement; or

2.10.2 the time from the start of heating power (P_H) removal to the start of the final V_F measurement time, referred to as t_{SW} .

2.11 t_{SW} — sample window time during which final V_F measurement is made; applicable only if t_{MD} definition 2.10.2 is used.

2.12 K — the temperature-sensitive parameter temperature coefficient measured at I_M in °C per millivolt.

2.13 CU — the comparison unit consisting of ΔV_F divided by I_H , that is used to normalize the transient thermal response for variations in power dissipation; in units of mV/A.

2.14 T_J — the device-under-test junction temperature.

2.15 ΔT_J — the change in T_J caused by the application of P_H for a time equal to t_H .

¹ Military Standards, Naval Publications and Form Center, 5801 Tabor Avenue, Philadelphia, PA 19120

2.16 σ_{Δ} — the standard deviation if the ΔV_F results for a given test condition.

2.17 σ_{CU} — the standard deviation of the CU results for a given test condition.

3 Test Operation

The following paragraphs describe in conceptual detail the operation of the test for integrated circuit thermal response.

3.1 *Set-Up* — Shown in Figure 1 is the set-up required for testing either active devices or thermal test chips. Figure 1a is used for those cases in which the TSP is the junction isolation diode forward biased voltage. Thermal test chips and test IC's for which the junction isolation diode is either not available, or desirable for temperature sensing, can be handled by the set-up shown in Figure 1b.

3.2 *Apparatus* — To implement either version of Figure 1 requires the following apparatus:

3.2.1 A constant voltage source capable of adjustment to the desired value of V_H and able to supply the I_H value drawn by the DUT.

3.2.2 A constant current source to supply I_M with sufficient voltage compliance to turn the TSP junction fully on.

3.2.3 An electronic switch capable of switching between the heating period conditions and measurement conditions in a time frame short enough to avoid DUT cooling during the transition; this typically requires switching in the microsecond range.

3.2.4 A voltage measurement circuit capable of accurately making the V_H measurement within the t_{MD} (or t_{MD} plus t_{SW} , depending on the definitions stated previously) time frame with millivolt resolution.

3.3 *Operation and Waveforms* — The test begins with the adjustment of I_M and V_H to the desired values. Then with the electronic switch in position 1, the value of V_F is measured. The switch is then moved to position 2 for a length of time equal to t_H and the value of I_H is measured. Finally, at the conclusion of t_H , the switch is again moved to position 1 and the V_F value is measured within a time period defined by t_{MD} (or t_{MD} plus t_{SW} , depending on the definitions stated previously). The voltage and current sources are then turned off at the completion of the test.

The voltage and current waveforms for the two versions of Figure 1 are shown in Figure 2.

4 Test Procedure

The procedures below describe how to set up the test conditions and determine the acceptance limits for implementing the transient thermal test for die attachment evaluation using the apparatus and definitions stated above.

4.1 *Initial Device Testing Procedure* — The following steps describe in detail how to set up the apparatus described previously for proper testing of various integrated circuit devices.

Step 1 — From a 10 to 15 piece sample of the integrated circuits to be tested, pick any one device to start the set-up process. Set up the test apparatus as follows:

$V_H = 5.0$ V (Or some other desired value near the device under tests (DUT's) normal operating voltage.)

$t_H = 200$ ms

$t_{MD} = 15$ μ s

$I_M = 1.0$ mA (Or some other value appropriate for the specific device under test; typically in the range of 80 μ A to 9.9 mA.)

Step 2 — Insert device into the apparatus test fixture and initiate a test.

(For best results, a test fixture that offers some form of heat sinking would be desirable.)

Step 3 — If ΔV_F is in the 20 to 40 mV range, then proceed to the next step. This range corresponds to a junction temperature change of roughly 10°C to 20°C and is sufficient for initial comparison purposes.

If ΔV_F is less than 20 mV, return to Step 1 and increase heating power into device by increasing V_H , or by reconfiguring the DUT connections for greater power dissipation, or a combination of both.

If ΔV_F is greater than 80 mV, corresponding to a junction temperature change greater than 40°C, it would probably be desirable to reduce the heating power by returning to Step 1 and reducing V_H , or by reconfiguring the DUT connections to reduce power dissipation, or a combination of the two. Reducing V_H is the preferable approach.

Because two different devices can show the same rise in junction temperature, even if the value of P_H is different, a comparison of the devices is best accomplished using the CU value. As defined in Section 2 above, CU provides a comparison unit that takes into account different device I_H values for a given V_H test condition.

Step 4 — Test each of the sample devices and record the ΔV_F and CU data as shown in Figure 3.

Step 5 — Select out the devices with the highest and lowest values of CU and put the remaining devices aside.

The ΔV_F values can be used instead of CU if the measured values of I_H are very tightly grouped around the average value.

Step 6 — Following the Heating Time (t_H) sequence shown in Figure 4, read and record the ΔV_F and CU data values for each of the two devices of Step 5.

Step 7 — Using the data from the previous step, prepare heating curves for the two devices in a manner similar to the examples shown in Figure 5.

Step 8 — Interpretation of the heating curves is the next step. Realizing that the thermal characteristics of identical chips should be the same if the heating time (t_H) is less than or equal to the thermal time constant of the chip, the two curves should start out the same for the low values of t_H . Non-identical chips (i.e., thinner or smaller in cross section) will have completely different curves, even at the smaller values of t_H . As the value of t_H is increased, thereby overcoming the chip thermal constant, heat will have propagated through the chip into the die attachment region. Since the heating curve devices of Step 5 were specifically chosen for their difference, the curves of Figure 5 diverge after t_H reaches a value where the die attachment variance has an effect on the device junction temperature. Increasing t_H further will probably result in a flattening of the curve as the heating propagates in the device package. If the device package has little thermal mass and/or is not well mounted to a good heat sink, the curve will not flatten very much, but will show a definite change in slope. Figure 6 shows the key elements of the heating curve.

Step 9 — Using the heating curve, select the appropriate value of t_H to correspond to the inflection point in the transition region between heat in the chip and heat in the package.

If there are several different elements in the heat flow path—chip, die attachment, substrate, substrate attachment, and package, for example, in a hybrid there will be several plateaus and transitions in the heating curve. Appropriate selection of t_H will optimize evaluation sensitivity to other attachment areas.

Step 10 — Return to the apparatus and set t_H equal to the value determined from Step 9.

Step 11 — Because the selected value of t_H is much less than that for thermal equilibrium, it is possible to significantly increase the heating power without degrading or destroying the device. The increased power dissipation within the device under test will result in high ΔV_F and/or CU values that will make determination of acceptable and non-acceptable devices much easier.

Step 12 — The pass/fail limit, the cutoff point between acceptable and non-acceptable devices, can be established in a variety of ways:

a) Correlation to other die attachment evaluation methods, such as die shear and/or x-ray; while these two methods have little actual value from a thermal point of view, they do represent standardized methods as described in MIL-STD specifications.

b) Maximum allowable junction temperature variation between devices; since the relationship between ΔT_J and ΔV_F is about $0.5^\circ\text{C}/\text{mV}$, the junction temperature spread between devices can be easily determined. The T_J predicts reliability. Conversely, the T_J spread necessary to meet the reliability projections can be translated to a ΔV_F and/or CU value for a Pass/Fail criteria, based on correlation with steady-state thermal equilibrium conditions.

To fully use this approach, it will be necessary to calibrate the devices for the exact value of the $T_J - V_F$ characteristic. The characteristic's slope, commonly referred to as K Factor, is easily measured on a sample basis using a voltmeter, environmental chamber, temperature indicator and a power supply setup for forcing, both active devices and thermal test chips as shown in Figure 7. A simple set of equations yields the junction temperature once K and ΔV_F are known:

$$\Delta T_J = |K| (\Delta V_F)$$

$$T_J = T_A + \Delta T_J$$

Where T_A is the ambient or reference temperature.

c) Statistically from a moderate size device sample; the distribution of ΔV_F or CU values should be a normal one with defective devices out of the normal range. Figure 8 shows a ΔV_F distribution for a sample lot of integrated circuits. Note that the left-hand side of the histogram envelope is fairly well-defined, but the other side is greatly skewed to the right. This comes about because the left-hand side is constrained by the absolutely best heat flow that can be obtained with a given chip assembly material and process. The other side has no such constraints because there is no limit as to how poorly a chip is mounted.