

# SEMI G5-87

## STANDARD FOR CERAMIC CHIP CARRIERS

This Standard was technically approved by the Assembly & Packaging Global Technical Committee.

**NOTICE:** This Standard or Safety Guideline has an Inactive Status because the conditions to maintain Current Status have not been met. Inactive Standards or Safety Guidelines are available from SEMI and continue to be valid for use.

### 1 Scope

1.1 This Specification defines the acceptance criteria for co-fired, ceramic chip carriers both leaded and lead-less.

### 2 Applicable Documents

#### 2.1 SEMI Standards and Safety Guidelines

SEMI G8 — Test Method for Gold Plating Quality

SEMI G25 — Test Method for Measuring the Resistance of Package Leads

SEMI G6 — Test Method for Seal Ring Flatness

#### 2.2 ANSI Specification<sup>1</sup>

SY 14.5 — Dimensioning and Tolerancing

#### 2.3 Federal Specification<sup>2</sup>

QQ-N-290 — Nickel Plating

#### 2.4 JEDEC Specification<sup>3</sup>

Pub. No. 95 — Registered and Standard Outline for Solid State Products

#### 2.5 Military Specifications<sup>4</sup>

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

MIL-STD-7883 — Brazing

MIL-M-38510 — General Specification for Microcircuits

MIL-STD-45204 — Gold Plating, Electrodeposited

### 3 Selected Definitions

3.1 *braz*e — an alloy with a melting point equal to or greater than 600°C.

3.2 *castellation* — that series of ribs and metallized indentations that define edge contact regions (see Figure 1).

3.3 *fired* — a process or technology to manufacture products in which the ceramic and refractory metallization are fired simultaneously.

3.4 *contact pad* — that metallized pattern that provides mechanical or electrical connection to the external circuitry.

3.5 *die attach surface* — see Figure 3.

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<sup>2</sup> United States Military Standards, Available through the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120-5099, USA; Telephone: +1.215.697.3321.

<sup>3</sup> Joint Electron Device Engineering Council, 3103 North 10<sup>th</sup> Street, Suite 240-S, Arlington, VA 22201, USA; Telephone: +1.703.907.7560, Fax: +1.703.907.7583, <http://www.jedec.org>

<sup>4</sup> General Services Administrator, 4th and D Streets, SW, Room 6039, Washington, D.C. 20407, USA.

3.6 *footprint* — contact pad pattern.

3.7 *layer* — a dielectric sheet with or without metallization that performs a discrete function as a part of the package.

3.8 *lead offset* — alignment of leads across the package.

3.9 *pullback* — the linear distance between the edge of the ceramic and the first measurable metallization and/or glass interface (see Figures 4 and 5).

3.10 *rundown* — see Figures 4 and 5.

3.11 *seal-area* — a dimensional outline area designated for either metallization or bare ceramic to provide a surface area for sealing (see Figure 3).

3.12 *terminal* — case outline at point of entry or exit of an electrical contact.

3.13 *TIR* — total indicator reading.

## 4 Ordering Information

4.1 Purchase order for ceramic chip carriers furnished to this Specification shall include the following items:

1. Quantity,
2. *Drawing* — The drawing(s) for ceramic chip carriers shall specify the following information:
  - a. Drawing number and revision level.
  - b. Number of terminals and terminal center line spacing.
  - c. Lead material and dimensions.
  - d. Critical material properties.
  - e. Type and thickness of plating.
  - f. Package dimensions per ANSI Y14.5.
  - g. Internal bonding patterns.
  - h. Minimum exposed metallized bond finger length and width.
  - i. Portion of external footprints connected to die attach area and/or seal ring.
  - j. Terminal #1 position, internal and external.
  - k. Certification (optional).
  - l. Method of test and measurements.
  - m. Electrical, mechanical, environmental requirements.
3. Reference to this Specification,
4. Any exception to print or specification.

## 5 Dimensions and Permissible Variations

5.1 The dimensions of ceramic chip carriers shall conform to those specified in the customer drawing, and be within the outline of JEDEC Publication No. 95.

NOTE 1: A dimensioning scheme and measurement fixture are under task force review.

### 5.2 Critical Material Parameters

#### 5.2.1 Ceramic

5.2.1.1 Alumina, content 90% minimum.

5.2.1.2 *Color* — Dark or white.

### 5.2.2 Metallization

#### 5.2.2.1 Refractory metallization.

#### 5.2.2.2 Plating (if designated) per MIL-M-38510.

#### 5.2.2.3 Nickel per QQ-N-290

#### 5.2.2.4 Gold per MIL-STD-45204, Type III.

#### 5.2.2.5 Gold Plating Quality see SEMI G8.

### 5.2.3 Braze per MIL-STD-7883.

### 5.2.4 Lead per MIL-STD-23011.

#### 5.2.4.1 Iron Nickel Cobalt alloy per MIL-M-38510, Type A.

#### 5.2.4.2 Iron Nickel alloy per MIL-M-38510, Type B.

## 6 Functional Testing

6.1 The following tests are recommended for functional evaluation of ceramic chip carriers. (The conditions of acceptance to be negotiated between the customer and the vendor.)

#### 6.1.1 Die Attach

#### 6.1.2 Pre-Seal Die Shear — (See § 10.1.6.)

#### 6.1.3 Wire Bond

#### 6.1.4 Pre-Seal Bond Pull — (See § 10.1.7.)

#### 6.1.5 Seal

#### 6.1.6 Environmental Test — (See §§ 10.1.1 through 10.1.13.)

#### 6.1.7 Hermeticity — (See § 10.1.14) Lid Torque or Shear (for glass seal parts).

#### 6.1.8 Post-Seal Bond Pull — (See § 10.1.7.)

#### 6.1.9 Post-Seal Die Shear — (See § 10.1.6.)

## 7 Incoming Testing

#### 7.1 Visual — (See § 8.)

#### 7.2 Dimensions

#### 7.3 Functional — (See § 6.)

#### 7.4 Standard Tests

#### 7.4.1 Electrical — (See SEMI G25.)

#### 7.4.2 Gold Plating Quality — (See SEMI G8.)

#### 7.4.3 Trim

#### 7.4.4 Lead Integrity — (See § 10.1.15.)

#### 7.4.5 Solderability — (See § 10.1.16.)

## 8 Visual

### 8.1 Applicable Definitions

8.1.1 *blister (bubble) ceramic* — Any separation within the ceramic which does not expose underlying ceramic material.