

SEMI G50-89

SPECIFICATION FOR CO-FIRED CERAMIC FINE PITCH LEADED AND LEADLESS CHIP CARRIER PACKAGE CONSTRUCTIONS

1 Preface

This specification defines the standard requirements for co-fired ceramic fine pitch chip carrier constructions, including both top brazed leaded and top metallized leadless configurations. These constructions are for hermetic packaging of various devices, (e.g., high speed, digital VLSI silicon devices), and next-level interconnection to printed wiring assemblies and modules by either lead solder attachment or by “leads last” techniques.

2 Applicable Documents

2.1 ANSI Specification¹

ANSI Y14.5 — Dimensioning and Tolerancing

2.2 Federal Specification²

QQ-N-290 — Nickel Plating

2.3 JEDEC Specification³

JEDEC Publication 95 — Registered and Standard Outlines for Solid State Products

2.4 Military Specifications

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

MIL-STD-7883 — Brazing

MIL-I-23011 — Iron Nickel Alloys for Sealing to Glass and Ceramics

MIL-M-38510 — General Specification for Microcircuits

MIL-G-45204 — Gold Plating, Electrodeposited

3 Selected Definitions

blister (bubble) — ceramics — Any separation within the ceramic which does not expose underlying ceramic material.

blister (bubble) — metal — Any localized separation within the metallization or between the metallization

and ceramic which does not expose underlying metal or ceramic material.

bond finger — A region of refractory metallization within the package cavity intended for wirebonding to a microcircuit die pad.

*braz*e — An alloy with a melting point equal to or greater than 600°C.

burr — An adherent fragment of excess parent material at the component edge.

chip-out — A region of ceramic missing from the surface or edge of a package which does not go completely through the package. Chip-out size is given by its length, width, and depth from a projection of the design planform (see Figure 1).

co-fired — A process or technology for manufacturing products in which the ceramic and refractory metallization are fired simultaneously.

contact pad — That metallized pattern to which the leadframe is brazed.

crack — A cleavage or fracture, internal or external.

die-attach surface — A designated dimensional outline area intended for die attach (see Figure 1).

foreign material — An adherent particle other than parent material of that component.

laver — A dielectric sheet with or without metallization that performs a discrete function as part of the package construction.

lead offset — Lead centerlines must be aligned to within 0.254 mm (0.010") of the centerline of corresponding braze pad metallizations.

peeling (flaking) — Any separation from the basis material that exposes the basis material.

projection — An adherent fragment of excess material on the component surface.

pullback — The linear distance between the edge of the ceramic and the first measurable metallization surface (see Figure 3).

rundown — The linear distance down a vertical surface from the top to the point of maximum metallization over-hand (see Figure 3).

1 ANSI, 1430 Broadway, New York, NY 10018

2 Military Standards, Naval Publications and Form Center, 5801 Tabor Ave., Philadelphia, PA 19120

3 JEDEC, 2001 Eye Street, N.W., Washington, D.C. 20006

seal area — A dimensional outline area designated for either metallization or base ceramic to provide a surface area for lid sealing (see Figure 2).

terminal — Metallization at the point of electrical contact to package interior circuitry; also the brazing surface for a lead.

TIR — Total indicator reading; the span of readings, from minimum to maximum, of a given dimension over the total surface it applied to.

voids (ceramics) — An absence of screen printed ceramic from a designated area greater than 0.75 mm (0.003") in diameter.

metal — An absence of refractory metallization, braze, or plating material from a designated area greater than 0.075 mm (0.003") in diameter.

4 Ordering Information

4.1 Purchase orders for co-fired ceramic packaged devices shall specify the following information:

1. Quantity
2. Drawing number and revision level or date
3. Reference to this specification
4. Any exception to drawing or specification

4.2 Drawings for co-fired ceramic packaged devices shall specify the following information:

1. Drawing number and revision level
2. Number of terminals and terminal centerline spacing
3. Lead material, finish, and dimensions, if applicable
4. Ceramic material color and composition; and refractory metal type
5. Type and thickness of plating on both device body and leads, if applicable
6. Dimensioning and tolerancing per ANSI Y14.5
7. Internal bonding pattern
8. Lead number 1 position
9. Method of test and measurements
10. Electrical, mechanical, and environmental requirements

5 Dimensions and Permissible Variations

Packaged device dimensions shall conform to JEDEC JC-11 registered outline dimension drawings for co-

fired ceramic fine pitch leaded and leadless chip carriers, unless otherwise specified.

6 Materials

6.1 Ceramic

6.1.1 Alumina content to be 90% minimum. Beryllia content to be 99% minimum.

6.1.2 Color to be black, dark brown, or dark violet unless otherwise specified.

6.2 *Metals* — External metal surfaces shall be in accordance with MIL-M-38510.

6.3 *Braze* — Copper/silver per MIL-STD-7883.

6.4 *Refractory Metallization* — To be per MIL-M-38510, Type C.

6.5 *Leadframe* — Fully annealed iron nickel cobalt alloy (per MIL-M-38410, Type A) or iron nickel alloy (per MIL-M-38510, Type B).

6.6 *Microcircuit Finishes* — Shall be per MIL-M-38510 unless otherwise specified.

7 Incoming Test Sequence

1. Visual inspection
2. Dimensional check
3. Electrical parameter testing
4. Sampling testing of plating quality, die attach, die shear, wire bond, pull, seal, hermeticity, lead integrity, and solderability

8 Visual Criteria (10× Magnification)

8.1 *Cracks* — None allowed per MIL-STD-883, Method 2009.

8.2 Chips

8.2.1 *Corner* — 0.762 mm (0.030") × 0.762 mm (0.030") × one tape layer thickness, maximum.

8.2.2 *Edge* — 0.54 mm (0.100") × 0.762 mm (0.030") × one tape layer thickness, maximum.

8.3 *Burrs, Projections, and Blisters* — Must fit within outline limit.

Top plane excluding seal area — 0.102 mm (0.004"), maximum

Unmetallized seal area — 0.0762 mm (0.003"), maximum

Metallized seal area — 0.025 mm (0.001"), maximum