

SEMI G58-94 (Reapproved 0811) SPECIFICATION FOR CERQUAD PACKAGE CONSTRUCTIONS

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NOTICE: This Document was reapproved with minor editorial changes.

1 Preface

1.1 *Purpose* — This Specification defines the acceptance criteria for cerquad package components and includes requirements for the base, leadframe, window frame, cap and sealing glass materials.

1.2 *Scope* — This Specification applies to all cerquad packages which have a leadframe sandwich between two ceramic pieces—the base and the window frame—and sealed by glass, and a cap with a similar glass seal.

NOTE 1: The base, leadframe and window frame may be purchased as separate components or as a completed assembly.

1.3 *Units* — U.S. Customary (inch-pound) or metric (SI) units may be used at the customer's discretion. This Specification uses U.S. Customary units as the prime unit.

NOTE 2: In the figures only U.S. Customary units are shown.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

2 Applicable Documents

2.1 *Order of Precedence* — To avoid conflicts, the order of precedence when ordering package components shall be as follows:

1. Purchase Order
2. Customer's Component Drawings
3. This Specification
4. Referenced Standards and Documents

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI G21 — Specification for Plating Integrated Circuit Leadframes

SEMI G23 — Test Method of Inductance for Internal Traces of Semiconductor Packages

SEMI G24 — Test Method for Measuring the Lead-to-Lead and Loading Capacitance of Package Leads

SEMI G25 — Test Method for Measuring the Resistance of Package Leads

3.2 JEDEC Standards¹

JEP95 — Registered and Standard Outlines for Semiconductor Devices

3.3 Military Standards²

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

¹ Joint Electron Device Engineering Council, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201, USA; Telephone: 703.907.7560, Fax: 703.907.7583, <http://www.jedec.org>

² United States Military Standards, Available through the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120-5099, USA; Telephone: 215.697.3321.

MIL-STD-1835 — Microcircuit Case Outlines

MIL-G-45204 — Gold Plating – Electrodeposited

MIL-M-38510 — General Specification for Microcircuits

3.4 Other Documents

SEMI International Standards Compilation of Terms

4 Terminology

4.1 Definitions

4.1.1 *blister (bubble) metallization* — an enclosed localized separation of the metallization from its base material (such as ceramic or another metallization layer component) that does not expose the underlying layer.

4.1.2 *burr* — an adherent fragment of parent material at a component edge. In leadframes, the metal burr, due to the stamping operation, may be in the horizontal or vertical direction to the surface. In ceramic packages, this type of characteristic is called a fin.

4.1.3 *camber (ceramic)* — arching of a nominally flat ceramic body.

4.1.4 *chip* — region of material missing from a component (e.g., ceramic from a package, or solder from a preform). The region does not progress completely through the component and is formed after the component is manufactured. Chip size is defined by its length, width and depth from a projection of the design platform. Also called chipout. (See Figure 1.)

4.1.5 *crack* — a cleavage or fracture that extends to the surface of a semiconductor package or solder preform. The crack may or may not pass through the entire thickness of the package or preform.

4.1.6 *critical seal area* — on a semiconductor package, the area bounded by the shortest nominal design distance from the largest cavity, usually the wire bond cavity, to the edge of the package or ceramic layer forming the seal area. (See Figure 2.)

4.1.7 *fin* — on a ceramic package or cap, a fine feathery-edged projection of parent ceramic material on the corner of the ceramic body.

4.1.8 *foreign material* — an adherent particle that is not parent material of the component. Adherence means that the particle cannot be removed by an air or nitrogen blast at 20 psi.

4.1.9 *glass flow* — on a semiconductor package or cap, the heating process which just removes all the screen printing mesh marks in the sealing glass when viewed at 10× magnification.

4.1.10 *glass void* — the absence of a sealing glass layer from a designated area.

4.1.11 *metallization void* — the absence of a clad, evaporated, plated or screen-printed metal layer or braze from a designated area.

4.1.12 *noncritical seal area* — on a semiconductor package that uses a lid, cap, or cover to effect the seal, the area of the sealing surface outside the critical sealing area. (See Figure 2.)

4.1.13 *overhang* — on a semiconductor package, the horizontal extension of the sealing glass past the vertical wall of a cavity cut into the ceramic layer on which the glass is printed. (See Figure 3.)

4.1.14 *peeling (flaking)* — any separation of a plated, vacuum deposited, or clad metal layer from the base metal of a leadframe, pin, heatsink, or seal ring, from an underplate, or from a refractory metal on a ceramic package. Peeling exposes the underlying metal.

4.1.15 *projection* — on a semiconductor package (plastic or ceramic), leadframe or preform, and irregularly raised portion of a surface indigenous to the parent material.

4.1.16 *pullback* — on a semiconductor package, the linear distance between the edge of a cavity cut into a ceramic layer and the first measureable glass or metallization layer interface coated onto the top surface of that layer. The total pullback may be the result of the high temperature processing required to manufacture the package or to coat the surface. It may also be the result of design considerations. (See Figure 3.)

4.1.17 *rundown* — on a semiconductor package, the linear distance from the upper surface of a ceramic cavity layer to the bottom point of the overhang into the cavity, of a sealing glass or metallization layer that has been screened onto that surface. (See Figure 3.)

5 Ordering Information

5.1 Purchase orders for cerquad packages and caps furnished to this specification shall include the following items:

5.2 Package description,

5.3 Current drawing revision detailing,

- All dimensions
- Type and color of ceramic
- Type and thickness of sealant glass
- Leadframe material type and design
- Type and thickness of metallization in the lead bond area
- Type and thickness of external lead plating, if applicable
- Type and thickness of die attach metalization

5.4 Vendor certification requirements,

5.5 Any additions to, or variations from, this specification.

6 Dimensions

6.1 The component described in this Specification shall produce packaged devices that conform to the outline dimensions and lead numbering for cerquad package constructions detailed in: JEP95; EIAJ; MIL-STD-1835. Package manufacturing tolerances shall be agreed between vendor and customer.

7 Materials

7.1 The definitions, defect criteria, and functional tests described in this Specification relate to package components made with the following materials:

7.1.1 Base, Window Frame, and Cap

7.1.1.1 Material,

7.1.1.1.1 *Alumina* — Content to be 90% minimum, or

7.1.1.1.2 *Beryllia* — Content to be agreed between vendor and customer.

7.1.1.2 Color

7.1.1.2.1 *Alumina* — Black, dark brown, or violet.

7.1.1.2.2 *Beryllia* — White.

7.1.2 *Sealant* — A solder glass suitable for hermetic sealing shall be specified.

7.1.3 *Die Attach Pad Metallization* — Gold or any other suitable material shall be specified.

7.1.4 Leadframe

7.1.4.1 Base Material

7.1.4.1.1 *Thickness* — Shall be specified.

7.1.4.1.2 *Composition* — Iron-Nickel-Cobalt alloy per MIL-M-38510, Type A or Iron-Nickel alloy per MIL-M-38510, Type B shall be specified.

7.1.4.2 *Finish* — Lead bond areas.

7.1.4.2.1 Metallization — Aluminum

7.1.4.2.1.1 Thickness — 100 to 600 microinches (0.0025 to 0.015 mm)

7.1.4.2.1.2 Coverage — Total coverage for a distance of 0.030 inch (0.762 mm) minimum as measured from the lead tip. Maximum length is defined by the lead bond cavity size.

7.1.4.2.1.3 Composition — 99.4% minimum for clad aluminum, 99.99% minimum for vapor deposited aluminum.

7.1.4.2.2 Metallization — Gold

7.1.4.2.2.1 Thickness — 50 to 225 microinches (0.0013 to 0.0057 mm)

7.1.4.2.2.2 Coverage — See ¶ 8.4.2.1.2.

7.1.4.2.2.3 Composition — See SEMI G21 and MIL-G-45204.

7.1.4.3 Leadframe Finish — External areas (if specified).

7.1.4.3.1 Metallization — Gold (see ¶ 8.4.2.2)

8 Defect Limits

8.1 The following defects shall be rejected if the limits shown are exceeded:

NOTE 3: The criteria apply to purchased pre-assemblies or, where applicable, to units assembled by the customer to process conditions agreed between vendor and customer.

8.2 Ceramic Components

8.2.1 Cracks — Not allowed.

8.2.2 Chips — See Figures 1 and 2.

8.2.2.1 Corner Chips — 0.030 inch (0.762 mm) × 0.030 inch (0.762 mm) × 25% of package element thickness.

8.2.2.2 Edge Chips — 0.060 inch (1.524 mm) × 0.030 inch (0.762 mm) × 25% of package element thickness.

8.2.2.3 Critical Seal Area — Chips must not reduce the critical seal path length, at any point, to less than one-half the nominal design dimension. No more than four chips are allowed in this area regardless of loss of seal length.

8.2.3 Burrs, Projections (Fins), and Blisters

8.2.3.1 Base, Window Frame, and Cap — 0.005 inch (0.127 mm) maximum allowable dimension or greater than 0.003 inch (0.076 mm) height.

8.2.3.2 Die Attach Surface — 0.001 inch (0.025 mm) maximum above the metallization surface excluding a zone, 0.010 inch (0.25 mm) wide, around the periphery of the cavity maximum allowable dimension is 0.005 inch (0.127 mm).

8.2.4 Camber — Shall be specified on the component drawing.

8.3 Glass Sealant

8.3.1 Chips and Voids — 0.010 inch (0.254 mm) maximum allowable dimension, with exposed or covered ceramic. No more than four chips or voids are allowed in the critical seal area. These defects must also meet the requirements of Table 1 in ¶ 9.2.2.4.

8.3.2 Glass Misalignment (after glass flow) — See Figure 3.

8.3.2.1 Glass Overhang — 0.15 inch (0.381 mm) maximum extension from the ceramic edge.

8.3.2.2 External Rundown — 50% of component thickness maximum.

8.3.2.3 Rundown into Lead Bond Cavity — 0.010 inch (0.254 mm) maximum extension from the top surface of the cavity.

8.3.2.4 Pullback — See Table 1.