

SEMI G61-94

SPECIFICATION FOR COFIRED CERAMIC PACKAGES

1 Preface

1.1 *Purpose* — This specification defines the materials and acceptance criteria for high-temperature, cofired ceramic packages.

1.2 *Scope* — The criteria detailed in this specification apply to the following package outlines registered with, or specified by JEDEC (see Publication 95), EIAJ, or MIL-STD-1835 specifications:

Chip Carriers (Leadless or Leaded)

Dual-in-Line Packages (Sidebrazed)

Flat Packs (Top or Bottom Brazed)

Grid Arrays (Land/Ball or Pin)

NOTE 1: Packages not meeting these specifications may also use the criteria as appropriate.

This document consolidates the criteria for all cofired packages so that package manufacturing and inspection may be simplified and costs reduced.

1.3 *Units* — U.S. Customary (inch-pound) or metric (SI) units may be used at the customer's discretion. This specification uses U.S. Customary units as the prime unit. In the drawings, only U.S. Customary units are detailed.

2 Applicable Documents

2.1 *Order of Precedence* — To avoid conflicts, the order of precedence when ordering packages shall be as follows:

Purchase Order

Customer's Package Drawings

This Specification

Reference Documents

Related Documents

2.2 Referenced Documents

2.2.1 SEMI Specifications

SEMI G6 — Seal Ring Flatness

SEMI G8 — Gold Plating — Temperature Resistance

SEMI G23 — Measuring the Inductance of Package Leads

SEMI G24 — Measuring the Lead-to-Lead and Loading Capacitance of Package Leads

SEMI G25 — Measuring the Resistance of Package Leads

SEMI G30 — Test Method, Junction-to-Case Thermal Resistance Measurements on Ceramic Packages

SEMI G35 — Test Methods for Lead Finishes on Semiconductor (Active) Devices

2.2.2 ANSI Specifications¹

ANSI Y14.5M — Dimensioning and Tolerancing

2.2.3 ASTM Specifications²

ASTM B 568 — Measurement of Coating Thickness by X-Ray Spectrometry

ASTM E 18 — Test Methods for Rockwell Hardness and Rockwell Superficial Hardness of Metallic Materials

ASTM E 165 — Liquid Penetrant Inspection Method

ASTM E 384 — Test Method for Microhardness of Materials

ASTM F 109 — Surface Imperfections on Ceramics

2.2.4 JEDEC Specifications³

Pub. No. 95 — Registered and Standard Outlines for Semiconductor Devices

2.2.5 Military and Federal Specifications⁴

MIL-STD-7883 — Brazing

MIL-STD-38510 — General Spec. for Microcircuits

MIL-G-45204 — Gold Plating — Electrodeposited

QQ-N-290A — Nickel Plating (Electrodeposited)

2.2.6 EIAJ Specifications

2.3 Related Documents

2.3.1 Military and Federal Specifications

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

1 ANSI, 1430 Broadway, New York, NY 10018

2 American Society of Testing Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959

3 JEDEC, 2001 Eye Street N.W., Washington D.C. 20006

4 Military Standards, Naval Publications and Form Center, 5801 Tabor Avenue, Philadelphia, PA 19120

3 Definition of Terms

3.1 *blister (bubble) ceramic* — an enclosed, localized separation within or between the layers of a ceramic package that does not expose an underlying layer of ceramic or metallization.

3.2 *blister (bubble) metallization* — an enclosed, localized separation of a metallization layer from its base material (such as ceramic or another metal layer) that does not expose the underlying layer.

3.3 *braz* — in semiconductor packages, an alloy used to attach pins, leads, seal rings and heat sinks/studs to the package.

3.4 *burr* — an adherent fragment of parent material at a component edge. In leadframes, the metal burr, due to the stamping operation, may be in the horizontal or vertical direction to the surface. In ceramic packages, this type of characteristic is called a fin.

3.5 *castellations* — metallized semi-circular channels on chip carrier edges which provide contact between internal package metallization traces and the external test pads. These castellations provide for improved solder fillets during attachment to a circuit board (see Figure 1).

3.6 *cavity-down packages* — packages where the die surface faces the mounting board. (See Figure 2 for the pin grid array packages in the cavity-down configuration. It is more usual to refer to the chip carrier mounting surfaces as the seating planes. In this cavity orientation, the seating plane is Seating Plane 2 per JEDEC JC-11.)

3.7 *cavity-up packages* — packages where the die surface faces away from the mounting board (see Figure 2 or Seating Plane 1 for chip carriers).

3.8 *chip* — region of material missing from a component (e.g., ceramic from a package, or solder from a preform). The region does not progress completely through the component and is formed after the component is manufactured. Chip size is defined by its length, width and depth from a projection of the design platform. Also called chipout (see Figure 1).

3.9 *co-fired* — in the manufacturing of some types of ceramic packages, the technology used to join together various ceramic layers and metallization patterns screened onto those layers by simultaneous firing at high temperature.

3.10 *contact pad* — in a leadless chip carrier or land grid array, the metallized areas on the bottom of the package that provide contact point between the internal leads and connecting external circuitry. They are also used for electrical test pads.

3.11 *crack* — a cleavage or fracture that extends to the surface of a semiconductor package or solder preform. The crack may or may not pass through the entire thickness of the package or preform.

3.12 *critical seal area (ceramic)* — on a semiconductor package, the area bounded by the shortest nominal design distance from the largest cavity, usually the wire bond cavity, to the edge of the package or ceramic layer forming the seal area.

3.13 *critical seal area* — metallization or metal ring — The entire area of the seal ring; it applies to plated refractory metal or a metal ring.

3.14 *critical seal path (ceramic)* — on a semiconductor package, the shortest nominal design distance from the largest cavity, usually the wire bond cavity, to the edge of the package or ceramic layer forming the seal area.

3.15 *delamination* — in a co-fired ceramic package, chip carrier, pin grid array, etc., the separation of one ceramic layer from another.

3.16 *element (packaging)* — part of a semiconductor package feature (e.g., package leads have braze paddle/stand-off and contact elements, pins have the nail head/braze area and contact elements).

3.17 *fin* — on a ceramic package or cap, a fine feathery-edged projection of parent ceramic material on the corner of the ceramic body.

3.18 *flatness* — in a ceramic package or leadframe, the allowable deviation of a surface from a defined reference plane. The tolerance zone is defined by two parallel planes within which the surface must lie.

3.19 *foreign material* — an adherent particle that is not parent material of the component. Adherence means that the particle cannot be removed by an air or nitrogen blast at 20 psi.

3.20 *heat exchange area* — a metallized region on one major surface of the package to which heat sinks may be attached by brazing, soldering, or adhesive resin.

3.21 *layer* — on a cofired ceramic package, the body is made from layers of ceramic or metallized ceramic. The layers are defined by their functionality, and several ceramic layers may be described as comprising one functional layer if all are common in plan-form and function (e.g., die attach cavity) (see Figure 4).

3.22 *lead offset* — in brazed lead ceramic packages, the variation in position of the centerline of the lead with reference to the centerline of the braze pad to which it is mounted.

3.23 *lead sweep* — lead movement, measured with respect to a datum, perpendicular to the top or bottom

of the package that passes through the designed mid-point of the lead where the lead is attached to the package (e.g., side-brazed laminates), or where the lead exits the package body (e.g., plastic dual-in-line packages). The movement is viewed from the side of the package, not the ends.

3.24 lead-to-lead separation — the distance between adjacent leads when measured from their centerlines at the point of connection to the package.

3.25 lead tweeze — lead movement, measured with respect to a datum, perpendicular to the top or bottom of the package that passes through the designed mid-point of the lead where the lead is attached to the package (e.g., side-brazed laminates), or where the lead exits the package body (e.g., plastic dual-in-line packages). The movement is viewed from the ends of the package, not the side and the lead movement is from the edges of the package in toward the centerline of the package.

3.26 metallization void — the absence of a clad, evaporated, plated or screen-printed metal layer or braze from a designated area. Also called metal or plating void.

3.27 peeling (flaking) — any separation of a plated, vacuum-deposited, or clad metal layer from the base metal of a leadframe, pin heatsink, or seal ring, from an underplate, or from a refractory metal on a ceramic package. Peeling exposes the underlying metal.

3.28 pin offset — the variation in position from the centerline of the pin to the centerline of the braze pad to which it is mounted.

3.29 pin sweep — pin movement, measured with respect to a datum, perpendicular to the top or bottom of the package that passes through the designed mid-point of pin where the pin is attached to the package (e.g., pin grid arrays). The movement is viewed from the side of the package, not the ends.

3.30 pin-to-pin separation — the distance between adjacent pins when measured from their centerlines at the point of connection to the package.

3.31 pin tweeze — pin movement, measured with respect to a datum, perpendicular to the top or bottom of the package that passes through the designed mid-point of pin where the pin is attached to the package (e.g., pin grid arrays). The movement is viewed from the ends of the package, not the side and the pin movement is from the edges of the package in toward the centerline of the package.

3.32 pit — in semiconductor packages, plastic or ceramic, or in the leadframes, a shallow depression or crater. The bottom of the depression must be visible in

order for the term to apply. A pit is formed during component manufacture (see Figure 3).

3.33 porous surface — an uncompacted ceramic surface often showing fine pits.

3.34 projection — on a semiconductor package (plastic or ceramic), leadframe or preform, and irregularly raised portion of a surface indigenous to the parent material.

3.35 pullback — on a semiconductor package, the linear distance between the edge of a cavity cut into a ceramic layer and the first measurable glass or metallization layer interface coated onto the top surface of that layer. The total pullback may be the result of the high temperature processing required to manufacture the package or to coat the surface. It may also be the result of design considerations (see Figure 5).

3.36 rundown — on a semiconductor package, the linear distance from the upper surface of a ceramic cavity layer to the bottom point of the overhang into the cavity, of a sealing glass or metallization layer that has been screened onto that surface (see Figure 5).

3.37 scrape — the irregular removal of a deposited layer from a base material by a shearing action from another surface such that the base material is exposed over an extended area. It can also apply to the removal of surface layers from a material. The material removed from the scraped area may build up at the edges of the scrape. The deposited layer may be a metal or glass.

3.38 seal area — on a semiconductor package, the area designated for sealing a cover or lid to a cofired ceramic package, or a cap to a cer-DIP or cer-pack base. In the case of a co-fired ceramic package the seal area may be either bare ceramic for glass sealing or a metallized area for solder sealing. The metallized seal area may be a plating over refractory metallization or a metal ring, usually iron-nickel-cobalt or iron-nickel alloys, brazed to the refractory metal.

3.39 seating plane — in plug-in packages such as dual-in-line (side-brazed or cer-DIP) or pin grid arrays, the plane defined by the three lowest stand-off features on the lead or pins as measured from the bottom of the package, or in the absence of these features, by the package base or mounting plane (see Figure 6). The features, such as shoulders or projections, hold the package off the circuit board to which it is mounted. This gap allows solder flux and residues to be cleaned after soldering the device and, in some cases, to allow for sufficient cooling air flow around the device. A prescribed force is used to hold the device in the mounting holes when the seating plane is to be measured.

3.40 *side-to-side misalignment* — the offset of the center lines of corresponding leads or pins from one side of the package to another side.

3.41 *stand-off* — the separation between the base plane and the seating plane that is created by physical features that are usually formed into the pins or leads (see Figure 6). The features may also be called stand-offs.

3.42 *TIR* — total Indicator Reading.

4 Ordering Information

Purchase orders for packages furnished to this specification shall include the following items.

4.1 *Current Drawing Revision Detailing*

4.1.1 All dimensions and tolerances per ANSI Y14.5M practices.

4.1.2 Internal metallization trace pattern.

4.1.3 Type and color of ceramic.

4.1.4 *Pin or Lead Material and Hardness* — If applicable.

4.1.5 *Heat Sink/Stud Material and Hardness* — If applicable.

4.1.6 Type, hardness, and thickness of plating in the die and wire bond areas and contact pads.

4.1.7 *Type, Hardness, and Thickness of Plating on Pins or Leads and Heat Sink/Stud* — If applicable.

4.1.8 *Lead Number 1 Identification* — (See Figure 7.)

4.2 Vendor certification requirements.

4.3 Reference to this specification.

4.4 Any additions to, or variations from, this specification.

4.5 Quantity.

5 Dimensions

Package dimensions and lead numbering shall conform to the outlines registered with or specified by JEDEC (see Publication 95), EIAJ or MIL-STD-1835, as appropriate. Package manufacturing tolerances shall be agreed between user and supplier.

6 Materials

The definitions, defect criteria, and functional tests described in this specification relate to packages made with the following materials.

6.1 *Ceramic Body*

6.1.1 *Material* — Alumina, beryllia, aluminum nitride, or mullite as specified on the package drawing.

6.1.1.1 *Alumina* — Content to be 90% minimum.

6.1.1.2 *Beryllia* — Content to be 99% minimum. (Packages shall be marked BeO.)

6.1.1.3 *Aluminum nitride* — Content to be agreed between user and supplier.

6.1.1.4 *Mullite* — Content to be agreed between user and supplier.

6.1.2 *Color*

6.1.2.1 *Alumina* — White, black, dark brown, or violet.

6.1.2.2 *Beryllia* — White.

6.1.2.3 *Aluminum Nitride* — White, black, dark brown, or violet.

6.1.2.4 *Mullite* — White, black, dark brown, or violet.

6.2 *Die Attach Pad, Wire Bond Fingers, Contact Pads, and Circuit Trace Metallization*

6.2.1 *Base Material* — Refractory tungsten per MIL-M-38510, Type C. Thickness shall be 0.0003" (0.0076 mm) minimum.

6.2.2 *Finish* — Shall meet the requirements of MIL-M-38510.

6.2.2.1 *Nickel Under Plate (if specified)* — Shall be per QQ-N-290A. Thickness shall be 50 – 350 micro-inches (0.0013 – 0.0089 mm).

6.2.2.2 *Gold Plate* — Shall be per MIL-G-45204, Type III. Thickness shall be 50 – 225 micro-inches (0.0013 – 0.005715 mm).

6.3 *Pins, Leads, and Seal Ring*

6.3.1 *Base Material* — Iron-nickel-cobalt alloy per MIL-M-38150, Type A or iron-nickel alloy per MIL-M-38150, Type B shall be specified on the package drawing.

6.3.2 *Hardness* — 70–85 Rockwell-B for Type A material, 60–80 Rockwell-B for Type B material.

6.3.3 *Finish* — Shall meet the requirements of MIL-M-38510 per Section 6.2.2.

6.4 *Heat Sink/Stud*

6.4.1 *Material*

6.4.1.1 *Heat Sink* — (Forming at least part of the package base and the die attach area) tungsten-copper (composition to be defined on the drawing), iron-nickel (cobalt) alloy per Section 6.3.1 or molybdenum as specified on the package drawing.

6.4.1.2 *Stud* — (Brazed to a metallized area of the ceramic base layer or the heatsink of the package) — copper, tungsten-copper, or kovar as specified on the package drawing.

6.4.2 *Hardness* — Shall be specified on the drawing by agreement between user and supplier.

6.4.3 *Finish* — Shall meet the requirements of MIL-M-38510 per Section 6.2.2.

6.5 Braze

6.5.1 *Material* — Silver/copper (72%/28%) or equivalent shall meet the general requirements of MIL-STD-7883.

6.5.2 *Finish* — Shall meet the requirements of MIL-M-38510 per Section 6.2.2.

7 Defect Limits

Inspection shall be carried out at 10× magnification with vertical lighting.

The following conditions are cause for rejection.

7.1 Ceramic Components

7.1.1 *Cracks* — Any crack is cause for rejection.

7.1.2 *Chips* — See Figure 3.

7.1.2.1 *Corner Chips* — Chip sizes exceeding the limits shown in Table 1. No chip may be deeper than 50% of the package element (the ceramic functional layer) thickness.

Table 1

Package Dimension inch (mm)	Maximum Corner Chip Dimensions (either direction) inch (mm)
≤0.250 (≤6.35)	0.020 (0.508)
>0.250 – ≤0.500 (>6.35 – ≤12.7)	0.040 (1.016)
>0.500 – ≤1.000 (>12.7 – ≤25.4)	0.080 (2.032)
>1.000 (>25.4)	0.100 (2.54)

7.1.2.2 *Edge Chips* — Chip sizes exceeding the limits shown in Table 2. No chip may be deeper than 50% of the package element (the ceramic functional layer) thickness.

Table 2

Package Dimension in which Chip Occurs inch (mm)	Maximum Chip Length and Width inch (mm)
≤0.250 (≤6.35)	0.020 (0.508)
>0.250 – ≤0.500 (>6.35 – ≤12.7)	0.040 (1.016)
>0.500 – ≤1.000 (>12.7 – ≤25.4)	0.080 (2.032)
>1.000 (>25.4)	0.100 (2.54)

7.1.2.3 Chips exposing a buried metallized area excluding the plating buses which are exposed when packages are separated from the manufacturing arrays.

7.1.2.4 *Critical Seal Area (ceramic)* — Any chip reducing the critical seal path length, at any point, by more than 30% of the nominal design dimension.

No more than three chips, each of which reduces the seal path length by more than 10% but less than 30%, are allowed in this area. Each chip's length shall not exceed the limits shown in Table 3.

Table 3

Seal Ring Dimension in which Chip Occurs inch (mm)	Maximum Chip Length inch (mm)
≤0.250 (≤6.35)	0.020 (0.508)
>0.250 – ≤0.500 (>6.35 – ≤12.7)	0.040 (1.016)
>0.500 – ≤1.000 (>12.7 – ≤25.4)	0.080 (2.032)
>1.000 (>25.4)	0.100 (2.54)

7.1.3 Ceramic Projections — (bumps and blisters)

7.1.3.1 *Body (non-critical surfaces)* — Any projection, including fins, exceeding 0.005" (0.127 mm) in height, or exceeding 0.002" (0.051 mm) in height and with a surface dimension greater than 0.010" (0.254 mm).

NOTE 2: On surface mount packages, the bottom of the package shall not have any projections exceeding 0.002" (0.051 mm) in height.

7.1.3.2 *Die Attach Areas* — (bare ceramic or screen printed metal area) — Excluding a zone, 0.015" (0.381 mm) wide, around the periphery of the cavity, any projection exceeding 0.001" (0.025 mm) in height or a surface dimension of 0.010" (0.254 mm).

NOTE 3: Exclusion zones around the periphery of die attach areas may be wider on larger packages or when a metal heat sink or stud is brazed to the package and forms the die attach area (Section 7.3). The width of such zones shall be defined on the package drawing by agreement between user and