

SEMI G80-0200

TEST METHOD FOR THE ANALYSIS OF OVERALL DIGITAL TIMING ACCURACY FOR AUTOMATED TEST EQUIPMENT

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1 Purpose

1.1 This procedure will define a standard process whereby any logic integrated circuit (IC) ATE system can be evaluated for parameters that makeup an AC timing accuracy specification.

1.2 Application of this procedure will simplify ATE comparisons, reduce specification ambiguity, simplify user acceptance procedures, simplify ATE performance monitoring, and provide a common validation criteria for ATE suppliers.

2 Scope

2.1 This procedure is intended for analysis of timing accuracy specifications for all semiconductor automatic test equipment (ATE) capable of digital functional testing. The extent of the analysis includes overall timing accuracy and the primary components of overall timing accuracy as defined in the definition section of this document.

2.2 This procedure does not include analysis of the following parameters associated with ATE timing accuracy:

- minimum driver pulse width,
- comparator bandwidth,
- I/O round trip delay,
- test fixturing errors,
- device insertion errors,
- time measurement unit (TMU) accuracy, and
- ATE capability or performance beyond AC timing accuracy.

2.3 Application of this procedure can reduce equipment acceptance time resulting in savings for both the end-users and ATE suppliers.

2.4 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Limitations

3.1 The following limitations are inherent to this procedure:

3.1.1 The tolerances of each measurement used in the procedure are listed in each test, where appropriate.

3.1.2 The verification methods do not include varying environmental conditions, so results may not reflect performance at environmental limits.

3.1.2.1 Due to execution time limits, the verification procedure does not represent an exhaustive analysis. The number of data points analyzed is intended to provide a minimum representative assessment of AC timing accuracy parameters in a practical amount of time.

3.1.3 This method uses only edge compare mode and non-multiplexed operation in providing a minimum representative assessment of AC timing accuracy.

3.1.4 This method does not determine the effects that duty cycle variations have on AC timing accuracy.

3.1.5 Not being an exhaustive analysis this method avoids comprehensive testing as might be expected for complex AC timing functions such as on-the-fly (OTF) timing. This method was defined with the intention of keeping the data gathering practical such that meaningful results are obtained in a reasonable amount of time. In the case of timing-on-the fly a routine is contained in this method and can be used as a reference parameter for comparative purposes when systems with on-the-fly timing are analyzed. Thus only the most fundamental AC timing results are produced and OTF timing is not included as part of the overall timing accuracy (OTA) results.

3.1.6 Discretion is advised when interpreting OTA results obtained from this method. Self-analysis cannot allow for all error components to be isolated. Thus good (compliant) method results should be viewed with caution as potentially compliant. On the other hand, poor (non-compliant) method results are a strong indication that the system under evaluation is questionable regarding its accuracy and most likely non-compliant.

4 Referenced Standards

4.1 SEMI Standard

SEMI G79 — Specification for Overall Digital Timing Accuracy

5 Terminology

5.1 Abbreviations and Acronyms

- 5.1.1 1^1 — tester output driver high level
- 5.1.2 0^2 — tester output driver low level
- 5.1.3 ATE — automated test equipment
- 5.1.4 DUT — device under test
- 5.1.5 H^3 — tester input comparator expect high level.
- 5.1.6 L^4 — tester input comparator expect low level.
- 5.1.7 n — highest pin/channel number, and Pin 1 — refers to the lowest pin/channel number.
- 5.1.8 NR — non-return signal format
- 5.1.9 RTO — return to one signal format.
- 5.1.10 RTZ — return to zero signal format.
- 5.1.11 SBC — surround by complement signal format.
- 5.1.12 Z — tester output driver high impedance (“off”) state.

5.2 Definitions

- 5.2.1 *device insertion errors* — error influenced by device-input capacitance and/or terminations.
- 5.2.2 *edge* — time delay created by an ATE delay generation resource.
- 5.2.3 *high bandwidth oscilloscope* — digital sampling oscilloscope with > 10 GHz bandwidth, using probes with > 1 GHz bandwidth, 500 ohm input impedance, $2.5\text{pF} \pm 0.5\text{pF}$ input capacitance and < 0.125" ground lead.
- 5.2.4 *pin* — tester channel
- 5.2.5 *performance board* — printed circuit board used to interface the tester channels to the device under test.
- 5.2.6 *test fixturing errors* — error influenced by mismatched signal path lengths, impedance discontinuities, lumped capacitance/inductance elements, and high frequency loss due to skin effect or interconnects.

5.2.7 *window compare* — monitor device continuously during a time interval.

5.2.8 *zero_reference_measurement* — oscilloscope measurement of the midpoint of a 0–3v NR signal rising edge with delay = 0s. This is an arbitrary reference signal selected by the user of this method. The method user is free to choose a convenient reference signal that will allow consistent use of that signal for making edge placement timing measurements during tests described in level 2 of this procedure.

6 Summary of Method

6.1 This procedure provides a hierarchical, generic method of analyzing ATE timing accuracy. The hierarchy supports two levels of specification analysis. Broad, composite net results are available by using the ATE for self-analysis in Level 1.

6.2 At this level, a large amount of data can be efficiently collected, representing the net conformance to overall timing accuracy specifications. This technique, however, precludes isolation and detailed analysis of specific accuracy components. Therefore, a second level of analysis, incorporating external instruments is included. While the first level provides efficient, broad analysis, the second level provides less efficient, detailed analysis.

6.3 Results from the analyses are saved in a standard format to facilitate further use for application specific data reduction. The minimum format is:

test #, channel #, min value, max value

6.3.1 Verification Procedure Summary

6.3.1.1 Level 1 ATE Self-Analysis

- Highly Efficient
- Broad Scope
- Moderate Error Observability
- Drive Input to Compare Output Tests
 - 3 Voltages
 - 2 Pin Directions
 - 503 Test Cycles⁵
 - 503 Pulse Widths
 - 12 Transitions⁶
 - 4 Formats
- Extended Delay Tests

¹ This convention is not universal. Sometimes a “H” is used.

² This convention is not universal. Sometimes a “L” is used

³ This convention is not universal. Sometimes a “1” is used.

⁴ This convention is not universal. Sometimes a “0” is used.

⁵ Reference Figure 3.

⁶ Reference Figure 2.

- Drive Z-State Tests
- Multiple Period Tests

6.3.1.2 Level 2 External Measurements

- Inefficient w/o Automation
- Focused Scope
- Good Error Observability
 - Drive (input) Timing Test
 - Compare (output) Timing Test
 - Driver Rise Time Test
 - Drive (input) Timing Cycle Jitter Test
 - High Speed Clock Test

7 Requirements

7.1 Acceptance Tests — Before initiating the test process, the ATE under evaluation is to be certified by a representative of the manufacturer or end-user to be fully operational.

7.2 Personnel Qualification — The individual(s) operating the ATE under evaluation must be certified or otherwise qualified to operate this equipment, and be familiar with the procedures for performing the analysis called-out in this document.

7.3 Supplemental Equipment — The following equipment is required: A digital sampling oscilloscope with > 10 GHz bandwidth, probes with > 1 GHz bandwidth, 500 ohm input impedance, 2.5 pF $\pm$ 0.5pF input capacitance, and < 0.125" ground lead. It is important that this equipment requirement step be met. Tolerances called-out in various steps of this procedure were chosen to be consistent with the general equipment specified in this equipment specification requirement.

7.4 This Procedure — It is highly recommended that the user of this method read this document (SEMI G80) in its entirety.

7.5 System — Test system usage will be available on a continuous basis and uninterrupted during the allotted time needed to perform this timing analysis procedure.

7.6 Application Program — It is required that an application program be written to perform the steps called-out in this procedure. That program will act as a means of reliable and consistent interaction between the tester and supplemental equipment. In so executing, that program will also facilitate the data collection process that will ultimately lead to the timing analysis conclusions this procedure produces.

7.7 The Method — The recommended procedure, contained primarily in Section 10 of this document, is generically written and will serve as a guide in producing the required program, written in the test application software language of the system under evaluation.

7.8 ATE System Performance (Load) Boards — To collect data two performance/load boards will be required. For one of these performance boards it is recommended that adjacent tester channels be shorted together with minimum and equal length interconnections. This board will facilitate the data collection process for Level 1 and in part for Level 2. The second board is to have an open driver to comparator connection and will be used for Level 2 drive input timing tests. Reference Figures 1 and 4.

7.9 Exceptions — It is expected that the user of this method execute the procedures as described in this document. If the method user should choose to deviate from the procedures recommended in this document it is expected that an appropriate description of that deviation be entered in the EXCEPTIONS PAGE provided in Appendix 3.

8 Test Conditions

8.1 Environmental — It is a requirement that the procedure called-out in this document be executed within the intended environmental operating conditions specified by the equipment supplier. Operating temperature requirements specified by the equipment supplier must be maintained.

8.2 Optional Execution — The user of this procedure may consider rerunning this procedure at environmental (temperature) extremes other than nominal.

8.3 Warm-up Period — It is essential that all equipment used or under evaluation be allowed to warm-up in accordance with the manufacturer's specified requirements for equipment stabilization.

8.4 Optional Data Collection — Data may be taken immediately after equipment calibration. However, the user of this procedure may wish to take additional data at subsequent time intervals, but within the known good calibration window for the system under evaluation.

9 Preparation of Apparatus

9.1 Equipment Configuration — The equipment under evaluation must be configured for its normal and intended operation. No special considerations such as additional cooling or removal of equipment skins are to be undertaken.

9.2 Equipment Calibration — The equipment under evaluation must be fully calibrated before this procedure is executed. No special calibration is to be

performed and the equipment is to be configured for normal and intended operation.

9.3 *Supplemental Equipment Calibration* — External equipment used for level 2 data collection in this procedure must be verified for proper calibration.

10 Test Method Procedure

10.1 The procedure is comprised of Level 1 tests and Level 2 tests. Any ATE capability described in the following tests that is not available on the ATE under analysis is not required for compliance to the procedure, but should be noted in the verification results Table 1 and Table 2.

10.2 Each test system is different; thus this procedure is generic. Regardless, it will provide comprehensive results when the specific application is created using this procedure as a guide. Per the requirements, a load board and application program written to accommodate the procedure should be in place when the procedure is executed. This procedure is to be executed per the requirements outlined in Section 7 of this document. When these requirements are met, the following steps will comprise the step by step process for execution of this Test Method:

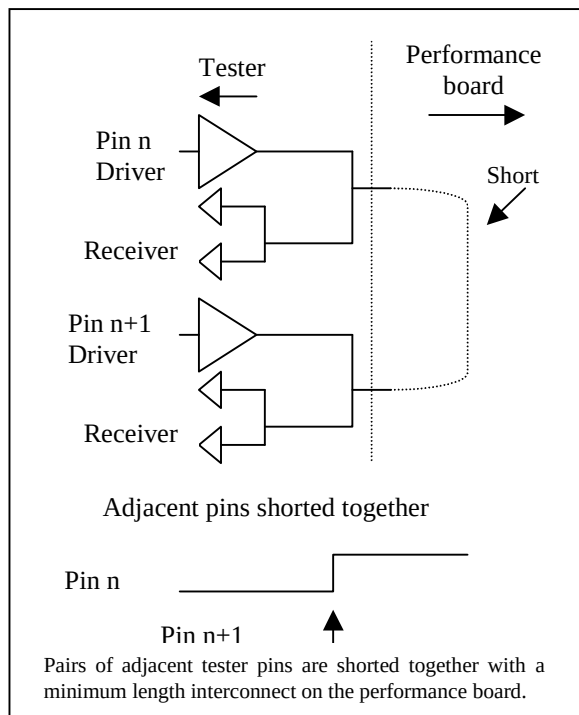


Figure 1
Level 1 Verification

1. Install the performance board.

2. Power up the system and supplemental equipment, allow adequate time for stabilization.

3. Load the appropriate application program that represents the embodiment of the procedure called out in Sections 10.3.1, 10.3.4, 10.3.5, and 10.3.6 for Level 1 as well as Sections 10.4.1, 10.4.2, 10.4.3, 10.4.4, 10.4.5, and 10.4.6 for Level 2.

4. Execute the method to completion. The application program can capture the data for Level 1 and Level 2 and store that for later analysis.

5. This procedure calls for various time measurements to be made at specified voltage points or signal levels. The user is encouraged to maintain these values to keep the method results constants when system to system comparisons are being made. Regardless, he is free to adjust these measurement points or levels to accommodate specific integrated circuit technology requirements important to that product and the system being analyzed. When that occurs documentation of those procedure variations must be entered in Appendix 3 (Exceptions Page).

6. Best results from this procedure are achieved if a consistent measurement methodology is maintained. This is important when making time measurements relative to a particular transition point on a signal edge. This method recommends that when signal measurements are specified at a particular transition point, i.e., 50%, that this point on the edge be determined relative to the 0% or 100% steady state levels displayed on the oscilloscope, after any aberrations due to the transition have expired. A tester reference channel, the lowest channel, should be used to set the measurement point(s) and then consistently used as the basis for subsequent measurements for the remaining tester channels.

7. *Data Analysis* — Analyze the captured data and make the appropriate data entries to Table 1, provided in this method document.

8. When this method execution is complete, document all method exceptions in the EXCEPTIONS section of this document (Appendix 3).

9. *Results* — Data entry to Table 2. Make the appropriate data entries to Table 2, provided in this method document and supplemented with examples contained in Appendix 2.

10.2.1 Level 1 requires no external equipment for completion, whereas Level 2 does require use of external equipment. The user is free to implement this procedure through total manual intervention. On the other hand, the user may choose to apply an automated or robotic approach to data collection for Level 2. Regardless, the user is advised that tester and external

equipment interaction accommodated by the application program is necessary for data collection at Level 2.

10.3 Level 1 Tests — Level 1 tests are intended to efficiently gather a large amount of data by taking advantage of the self-analysis ability of the ATE. This is accomplished by shorting adjacent tester channels together on a performance board with minimum, equal length interconnections, and using one channel to test the other. Reference Figure 1. Execution speed and system resource coverage are of primary importance for Level 1. Level 1 is intended to analyze specification conformance as opposed to diagnose system failures. All measurements are normalized to “zero” in order to facilitate subsequent data reduction/analysis. Level 1 is intended to collect data only. Data reduction and processing are to be done off-line in order to maximize data collection efficiency.

10.3.1 Timing Linearity Test — This test is used to establish drive input to compare output timing accuracy by “stretching” the test cycle in minimum cycle programming increments while using fixed percentage delays and pulse widths as the method sweeps through various timing conditions. The test pattern should be written to switch all even or odd pins simultaneously, and for all transitions and associated strobes to occur at least 100 times for each data point.

10.3.2 For clarification all drive edges are detected in parallel in pairs. The intention is to sweep the compare edge and detect the earliest occurrence of a drive edge with the latest compare edge, as well as detect the latest occurrence of a drive edge with the earliest compare edge.

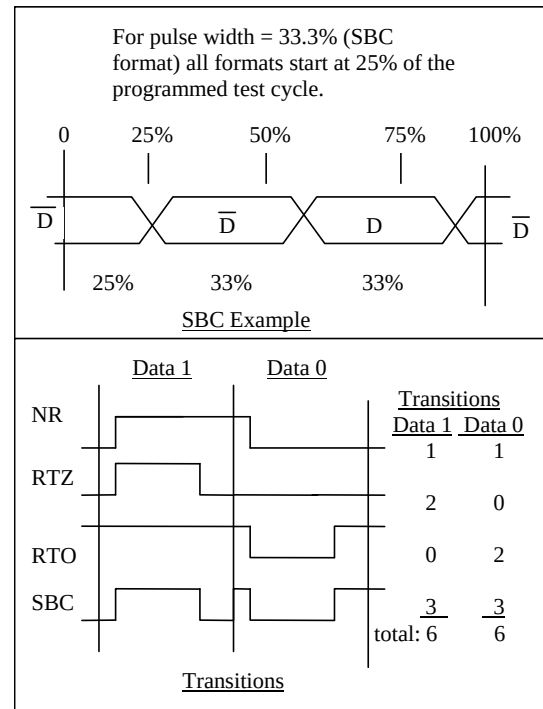


Figure 2
SBC Example and Transitions

10.3.3 The following Test Cycle Example and nested loop outline describes the test flow:

```

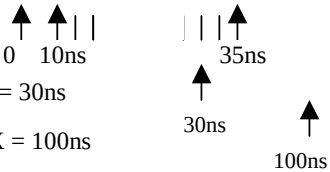
for amplitude = 1V, 3V, 5V
  for direction =
    odd_pins_drive_&_even_pins_compare to
    even_pins_drive_&_odd_pins_compare
  for test_cycle = min_cycle to [min_cycle +
    500*cycle_resolution] by
    cycle_resolution, 3x min_cycle, 10x min cycle
  for pulse width = 50% (RTZ/RTO formats)
    = 33.3% (SBC format)
    = don't care (NR format)
  for format = NR, RTZ, RTO, SBC (NOTE 1: all
    formats start at 25% of the programmed test
    cycle)
  for all format transitions (pattern data 0 and 1)
    detect earliest occurrence of format
      transition midpoint with the latest
      compare pin
    detect latest occurrence of format transition
      midpoint with the earliest compare pin
    error = (latest occurrence - earliest
      occurrence)
  end transitions
  end format
  end pulse width
  end test_cycle
  end direction
end amplitude
  
```

For test_cycle = min_cycle to [min_cycle + 500*cycle resolution] by cycle_resolution, 3Xmin_cycle, 10x min_cycle.

Example:

Minimum Period Cycle: 10ns
Period resolution: 50ps

10ns to (10ns + 25ns) by 50ps

- 501 cycles: 
- 1 cycle: 3X = 30ns
- 1 cycle: 10X = 100ns

Total of 503 cycles. The intention of the last two cycles is to define a period that is far beyond the minimum period.

Figure 3
Test Cycle Example

10.3.4 Extended Delay Test — This test is used to establish drive input to compare output timing accuracy when timing generator delay values are programmed beyond the length of the test cycle. Driver input delays are programmed to occur in subsequent test cycles and detected with compare delays originating in the corresponding subsequent test cycle. The intention is the same as Section 10.3.1 with the exception that edges are programmed into a subsequent cycle. Conditions such as formats and voltages have been reduced to keep the amount of data collected down to a reasonable level.

10.3.4.1 The following nested loop outline describes the test flow:

```

for amplitude = 3V
  for direction =
    odd_pins_drive_&_even_pins_compare to
    even_pins_drive_&_odd_pins_compare
    for test_cycle = min to 10*min by 0.1*min
      for format = NR
        for format_delay = test_cycle to max_delay by
          0.25*test_cycle (max delay is beyond the cycle
            boundary)
          detect earliest occurrence of format
            transition midpoint with the latest
            compare pin using pattern expect
            data shifted into the appropriate cycle
          detect latest occurrence of format transition
            midpoint with the earliest compare pin
            using pattern expect data shifted into
            the appropriate cycle
          error = (latest occurrence - earliest
            occurrence)
          end delays
        end format
      end test_cycles
    end directions
  end amplitude

```

10.3.5 Driver Z State Test — This test verifies the timing accuracy of tester driver transitions from Z to 1/0 and from 1/0 to Z. Driver inputs are programmed to transition to and from Z and 1/0 while being loaded with 50 ohms terminated to drive 1 for Z to 0 and 0 to Z, and 50 ohms terminated to drive 0 for Z to 1 and 1 to Z⁷ (reference load C). The following nested loop outline describes the test flow:

```

for amplitude = 3V
  for direction =
    odd_pins_drive_&_even_pins_compare to
    even_pins_drive_&_odd_pins_compare
    for test_cycle = 5*min_cycle
      for format_delay = 50%
        for format = NR
          detect earliest occurrence of Z to low tran-
            sition at scaled midpoint with compare pins
          detect latest occurrence of Z to low tran-
            sition at scaled midpoint with compare pins
          error=(latest occurrence - earliest occurrence)
          detect earliest occurrence of Z to 1 tran-
            sition at scaled midpoint with compare pins
          detect latest occurrence of Z to 1 transition
            at scaled midpoint with compare pins
          error = (latest occurrence - earliest occur-
            rence)
          detect earliest occurrence of 0 to Z transition
            at scaled midpoint with compare pins
          detect latest occurrence of 0 to Z transition at
            scaled midpoint with compare pins
          error = (latest occurrence - earliest occur-
            rence)
          detect earliest occurrence of 1 to Z tran-
            sition at scaled midpoint with compare pins
          detect latest occurrence of 1 to Z transition
            at scaled midpoint with compare pins
          error = (latest occurrence - earliest occur-
            rence)
        end format
      end format_delay
    end test_cycle
  end direction
end amplitude

```

10.3.6 Multiple Period Test⁸ — This is an optional test to be run only if the ATE supports dynamic (or “on-the-fly”) time set switching. This test intention is similar to Section 10.3.1 and 10.3.4 (timing linearity and extended delay tests) except that the test period and delay changes are generated dynamically within a

⁷ Tying two drivers together or connecting a resistor to a logic point is acceptable. Note: Load “C”: 50 ohms to low for driver z to high and high to z transitions. And 50 ohms to high for driver z to low and low to z transitions.

⁸ This algorithm requires 64 time sets. If the equipment does not have 64 time sets, adjust the algorithm to accommodate the amount available and note the differences on the exception page, Appendix 3.

single test pattern burst. The following nested loop outline describes the test flow:

for amplitude = 1V, 3V, 5V

for direction =

odd_pins_drive_&_even_pins_compare to

even_pins_drive_&_odd_pins_compare

execute single pattern with the following

dynamic changes:

Test Cycle	Drive Format	Format Offset	Pulse Width	Drive Data	Compare Offset	Expect Data
min	SBC	20%	33%	1	53%	H
min	SBC	20%	33%	1	86%	L
min	SBC	20%	33%	0	53%	L
min	SBC	20%	33%	0	86%	H
min	SBC	20%	33%	1	20%	L
.						
min	SBC	20%	33%	0	20%	H
64*min	SBC	20%	33%	1	53%	H
64*min	SBC	20%	33%	1	86%	L
64*min	SBC	20%	33%	0	53%	L
64*min	SBC	20%	33%	0	86%	H
64*min	SBC	20%	33%	1	20%	L
64*min	SBC	20%	33%	0	20%	H
2*min	SBC	20%	33%	1	53%	H
2*min	SBC	20%	33%	1	86%	L
2*min	SBC	20%	33%	0	53%	L
2*min	SBC	20%	33%	0	86%	H
2*min	SBC	20%	33%	1	20%	L
2*min	SBC	20%	33%	0	20%	H
63*min	SBC	20%	33%	1	53%	H
63*min	SBC	20%	33%	1	86%	L
63*min	SBC	20%	33%	0	53%	L
63*min	SBC	20%	33%	0	86%	H
63*min	SBC	20%	33%	1	20%	L
63*min	SBC	20%	33%	0	20%	H
.						
32*min	SBC	20%	33%	1	53%	H
32*min	SBC	20%	33%	1	86%	L
32*min	SBC	20%	33%	0	53%	L
32*min	SBC	20%	33%	0	86%	H
32*min	SBC	20%	33%	1	20%	L
32*min	SBC	20%	33%	0	20%	H

detect earliest occurrence of format transition midpoint with the latest compare pin
 detect latest occurrence of format transition midpoint with the earliest compare pin
 error = (latest occurrence - earliest occurrence)
 end direction
 end amplitude

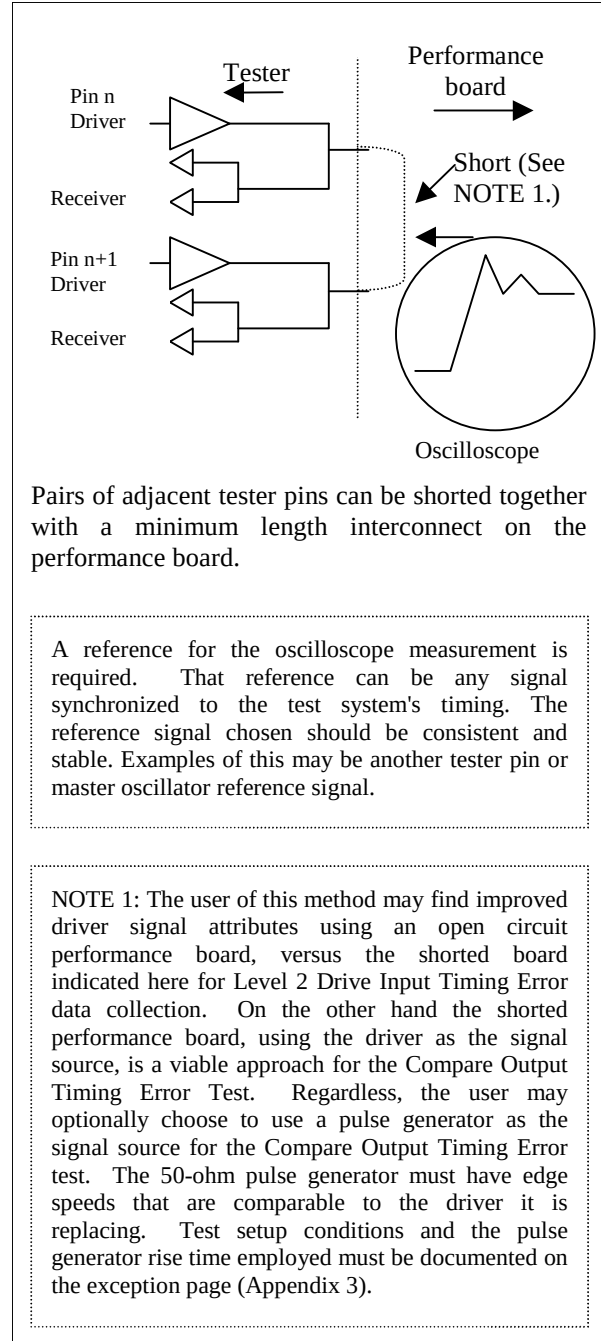


Figure 4
Level 2 Verification

10.4 Level 2 Tests — The efficiency of data collection with Level 1 tests may preclude isolation of certain specification components. The self-analysis procedures may also mask some error terms that contribute to other specification components. Therefore, Level 2 modules are intended to supplement Level 1 results by using external instruments to distinguish individual specification components and provide detailed analysis

of potentially masked results. The use of external instruments facilitates independent observation of individual parameters, but requires physical movement of a probe (unless automated with robotics), which results in less efficient data collection. Reference Figure 4.

10.4.1 Drive Input Timing Error Test — Since the driver input timing error cannot be distinguished from compare output timing error with Level 1 tests⁹ an external instrument must be used to isolate the driver input timing error from compare output timing error. An external instrument is also required to identify pin to pin “skew” beyond adjacent pins, since Level 1 only uses adjacent pin pairs for analysis. This requires independent measurements of representative driver input timing conditions. The reference for measurement of driver input timing error is a high bandwidth-digital sampling oscilloscope. Exhaustive testing of all pins is impractical, so a reduced set of representative conditions is used. A non-binary pin sampling increment is used to ensure that traditional binary architectural boundaries are crossed. The tolerance for the driver input timing error test is $\pm 20\text{ps}$ ¹⁰ due to the tester/instrument interaction using a generic measurement method. The following nested loop outline describes the test flow:

```
for amplitude = 3V
  for pin = 1 to n by 3
    for test_cycle = min, 2*min, 3*min, 10*min
      for format_delay = 50% of test cycle
        for format = NR, RTZ, RTO, SBC
          for all format transitions
            detect midpoint of drive transition with
              oscilloscope (averaging = 8)
            error = (measured_delay - pro-
              grammed_format_edge_time -
              zero_reference_measurement)
          end transitions
        end format
      end format_delay
    end test_cycle
  end pin
end amplitude
```

10.4.2 Compare Output Timing Error Test — Since the compare output timing error cannot be distinguished from driver input timing error with Level 1 tests, an external reference must be used to isolate compare output timing error from driver input timing error. This requires independent measurement of representative

compare timing conditions. Each tester driver is used to provide a synchronous reference signal by shorting adjacent tester channels together on a performance board with minimum, equal length interconnections. The actual delay of the driver signal is verified with a high bandwidth-digital sampling oscilloscope. (See Figure 4.)

NOTE 2: If a signal reflection is present at the midpoint of the observed signal (due to a long distance from the performance board to the tester receiver), then the 25% point of the reference driver waveform should be used, instead of the midpoint - as specified below.

10.4.2.1 Exhaustive testing of all pins is impractical, so a reduced set of representative conditions are used. A non-binary pin sampling increment is used to ensure that traditional binary architectural boundaries are crossed.

10.4.2.2 The following nested loop outline describes the test flow:

```
for amplitude = 3V
  for pin = 1 to n by 3
    for test_cycle = min, 2*min, 3*min, 10*min
      for format_delay = 50% of test_cycle
        for format = NR
          for edge = rising, falling
            detect midpoint of NR drive signal with
              oscilloscope (averaging = 8)
            detect midpoint of drive transition with
              comparator (strobe compare mode)
            error = (measured_delay - pro-
              grammed_compare_delay -
              zero_reference_measurement)
          end edge
        end format
      end format_delay
    end test_cycle
  end pin
end amplitude
```

NOTE 3: Midpoint detection of the NR drive signal should be done via a compare edge sweep technique.

10.4.3 Driver Transition Time Test — Since driver transition time errors can be masked by compare timing errors and comparator bandwidth limitations, an external instrument is required to measure driver transition time errors. The reference used for driver transition time measurements is a high bandwidth-digital sampling oscilloscope.

10.4.3.1 The tolerance for driver transition time measurements is $\pm 150\text{ps}$ ¹¹ due to the tester/instrument

⁹ See APPENDIX 2, Section A2-1.3 and Appendix 2, Examples for an explanation.

¹⁰ When recording measurements, data log all measurements as they are taken from the measurement equipment and show the associated equipment tolerance as a separate entity.

¹¹ This 150ps tolerance has been extended beyond 20ps due to level sensitivities associated with oscilloscopes and typical bandwidth variations in oscilloscope probes rendering transition time measurements less accurate.

interaction using a generic measurement method. The signal measurement should be made with the driver loaded with reference load A (500 ohms in parallel with $2.5\text{pF} \pm 0.5\text{pF}$ of capacitance). The following nested loop outline describes the test flow:

```
for amplitude = 1V, 3V, 5V (optional)
  for pin = 1 to n
    for edge = rising to falling
      measure the 20% to 80% transition time of a
      NR driver signal with test cycle = 10*min,
      delay = 0s using oscilloscope (averaging = 8)
      error = maximum transition time - minimum
      transition time
    end edge
  end pin
end amplitude
```

10.4.3.2 The transition time measurements are to be made between the measured 20% and 80% points of both positive and negative signal edges, i.e., the 20% and 80% points on the signal transition edge relative to a 0% or 100% steady state level displayed on the oscilloscope. Ideally, measurement points chosen should be referenced to a steady state level that results after all aberrations in the transition have expired. Use the lowest tester pin as a reference channel when setting the measurement points for these measurements.

10.4.3.3 ATE systems may use a focused calibration routine for driver pins. That routine is intended to correct edge error due to transition time variations. In the context of executing this method for a machine that has this capability, the user of this method is advised to: 1) Execute the Drive Input Transition Time Variation test regardless, and 2) Enter the test results to the method data summary, Table 2. The entry in Table 2 for transition variation will be a reference parameter. This method as defined is incapable of making drive edge error measurements that exclude transition variation and jitter.

10.4.4 *Driver Input Timing Cycle Jitter Test*¹² — Since driver input timing jitter cannot be determined from Level 1 tests, an external instrument must be used to measure short term, cycle to cycle (or period) instability. This can be done by making period measurements of the driver-input channel under test, with a high bandwidth, digital sampling oscilloscope. A 50-ohm probe should be used to minimize measurement jitter. The tolerance for this test is $\pm$

20ps^{13} (min-max) due to the tester/instrument interaction using a generic measurement method. The measurement results are expressed as RMS. This measurement depends on the jitter distribution being Gaussian. Reference Appendix 4 for additional detail regarding this measurement. If in the application of this method it is determined that the jitter is non-Gaussian, skip this test and make the appropriate notation on the exceptions page (Appendix 3).

10.4.4.1 The following nested loop outline describes the test flow:

```
for pin = 1 to n
  for amplitude = 3V
    for test_cycle = 2*min
      for format = RTZ
        for format_delay = 50%
          for pulse_width = 50%
            for i = 1 to 1000
              meas(i) = measure the period of the pin under test
              end i
              measured signal jitter = RMS spread of meas(1)
              through meas(1000)
              end pulse_width
            end format_delay
          end format
        end test_cycle
      end amplitude
    end pin
    measured instrumentation jitter = RMS spread of
    oscilloscope trigger
    (method described further in Appendix 4)
    actual RMS signal jitter = measured signal jitter -
    measured instrumentation jitter
    (via sum of squares - reference Appendix 4)
```

Reference load B (50 ohms to ground) should be used for this measurement.

10.4.5 *High Speed Clock Self-trigger Cycle Jitter Test* — If the ATE is configured with dedicated high speed clock pins, an external instrument must be used to measure short term, cycle to cycle (or period) instability.

¹² Trigger off the scope probe for this and the subsequent jitter test. Use a high persistence display to show signal jitter. Use of a high bandwidth-sampling oscilloscope with statistical capability is recommended. Instrumentation jitter should be extracted from the measured signal jitter, as explained in Appendix 4.

¹³ When recording measurement data, log all measurements as they are taken from the measurement equipment and show the associated equipment tolerances as a separate entity.

10.4.5.1 This can be done by making period measurements of the high speed clock channel under test, with a high bandwidth, digital sampling oscilloscope. A 50-ohm probe should be used to minimize measurement jitter. The tolerance for this test is $\pm 20\text{ps}$ (min-max) due to the tester/instrument interaction using a generic measurement method. The measurement results are expressed as RMS. This measurement depends on the jitter distribution being Gaussian. Reference Appendix 4 for additional detail regarding this measurement. If in the application of this method it is determined that the jitter is non-Gaussian, skip this test and make the appropriate notation on the exceptions page (Appendix 3). The following nested loop outline describes the test flow:

```

for pin = (all high speed clock pins)
  for amplitude = 3V
    for test_cycle = 10*min to min by min
      for clock_delay = 50%
        for i = 1 to 1000
          meas(i) = measure the period of the clock pin under
            test
          end i
          measured signal jitter = RMS spread of meas(1)
            through meas(1000)
          end format_delay
          end test_cycle
          end amplitude
        end pin
        measured instrumentation jitter = RMS spread of
          oscilloscope trigger
          (method described further in Appendix 4)
        actual RMS signal jitter = measured signal jitter -
          measured instrumentation jitter
        (via sum of squares - reference Appendix 4)

Reference load B (50 ohms to ground) should be used
for this measurement.
  
```

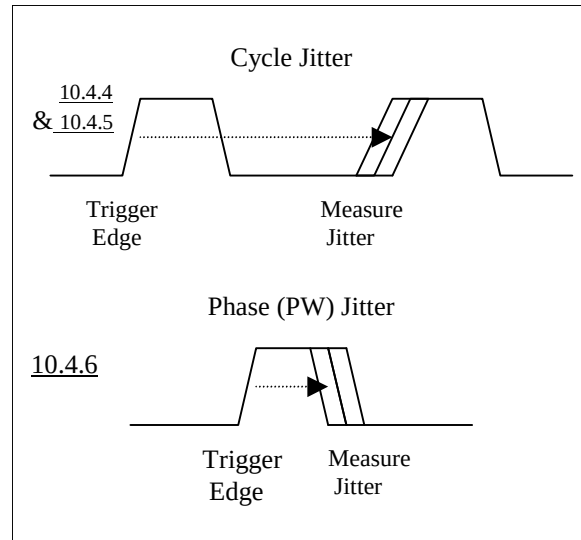


Figure 5
Jitter Tests – Sections 10.4.4, 10.4.5 and 10.4.6

10.4.6 High Speed Clock Self-trigger Phase Jitter Test
— If the ATE is configured with dedicated high speed clock pins, an external instrument must be used to measure short term, phase (or duty cycle) instability. This can be done by making pulse width measurements of the high speed clock channel under test, using a high bandwidth, digital-sampling oscilloscope. A 50-ohm probe should be used to minimize measurement jitter. The tolerance for this test is $\pm 20\text{ps}^{14}$ (min-max) due to the tester/instrument interaction using a generic measurement method. The results are expressed as RMS.

10.4.6.1 This measurement depends on the jitter distribution being Gaussian. Reference Appendix 4 for additional detail regarding this measurement. If in the application of this method it is determined that the jitter is non-Gaussian, skip this test and make the appropriate notation on the exceptions page (Appendix 3). The following nested loop outline describes the test flow:

```

for pin = (all high speed clock pins)
  for amplitude = 3V
    for test_cycle = 10*min to min by min
      for clock_delay = 50%
        for i = 1 to 1000
          meas(i) = measure the pulse width of the clock pin
            under test
          end i
          measured signal jitter = RMS spread of meas(1)
            through meas(1000)
          end format_delay
        end pin
      end test_cycle
    end amplitude
  end pin
  
```

¹⁴ When recording measurement data, log all measurements as they are taken from the measurement equipment and show the associated equipment tolerance as a separate entity.