SEMI HB1-0315
SPECIFICATIONS FOR SAPPHIRE WAFERS INTENDED FOR USE FOR MANUFACTURING HIGH BRIGHTNESS-LIGHT EMITTING DIODE DEVICES

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1 Purpose

1.1 Sapphire wafers are widely used in producing high brightness-light emitting diode (HB-LED) devices that are used in multiple applications such as LCD backlights, signage and solid-state lighting. Improving manufacturing efficiency and cost reductions are critical elements in enabling continued industry advance. Sapphire wafers represent a key inflection point to obtain these goals. A recent SEMI survey identified key parameters and dimensions critical to enabling manufacturing automation across multiple manufacturing steps. These specifications are intended to provide the necessary information for specifying such wafers.

2 Scope

2.1 These specifications cover dimensional, wafer preparation, and crystallographic orientation characteristics for five categories of single-crystal single-side polished sapphire wafers used in HB-LED manufacturing as follows:

- Category 4a – Flatted 100 mm diameter, 650 µm thick, polished c-axis sapphire wafers
- Category 6a – Flatted 150 mm diameter, 1,000 µm thick, polished c-axis sapphire wafers
- Category 6b – Flatted 150 mm diameter, 1,300 µm thick, polished c-axis sapphire wafers
- Category 6c – Notched 150 mm diameter, 1,000 µm thick, polished c-axis sapphire wafers
- Category 6d – Notched 150 mm diameter, 1,300 µm thick, polished c-axis sapphire wafers

2.1.1 In addition, methods of measurements suitable for determining the characteristics in the specifications are indicated.

2.1.2 Those characteristics for which standardized values have been agreed upon are indicated in the specification tables.

2.1.3 A complete purchase specification requires that additional characteristics be specified along with test methods suitable for determining their magnitude. Guidance for such characteristics is provided in Related Information 1.

2.2 These specifications are directed specifically to sapphire wafers with one polished surface. Wafers polished on both sides, or unpolished, or with epitaxial film, are not covered; however, customers of such wafers may find that these specifications are useful guides in defining their requirements.

2.3 For referee purposes, SI (System International commonly called metric) units are used for all sapphire wafers.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

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SEMI M40 — Guide for Measurement of Roughness of Planar Surfaces on Polished Wafers

SEMI M65 — Specifications for Sapphire Substrates to Use for Compound Semiconductor Epitaxial Wafers

SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF523 — Practice for Unaided Visual Inspections of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variations of Silicon Wafers

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.2 *ASQ Standard*[1]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standard*[2]

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specified Precision, the Average for a Characteristic of a Lot or Process

3.4 *JIS Standards*[3]

JIS H 0611 — Methods of Measurement of Thickness, Thickness Variation and Bow of Silicon Wafer

JIS H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Terms and acronyms associated with silicon wafers and silicon technology are listed and defined in SEMI M59. Many of these terms and acronyms can be applied to sapphire wafers and their associated technology.

4.2 *General Definitions*

NOTE 1: Many of these definitions are similar to but slightly different from those in SEMI M59. In many cases the definitions in SEMI M59 can be generalized to include sapphire terms, but this is not being done at the present time.

4.2.1 *back surface* — the exposed surface opposite to that upon which devices have been or will be fabricated.

4.2.2 *bow* — the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer.

[1] American Society for Quality, 600 North Plankinton Avenue, Milwaukee, WI 53203, USA; Telephone: 414.272.8575, Fax: 414.272.1734, http://www.asq.org

[2] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: 610.832.9585, Fax: 610.832.9555, http://www.astm.org

[3] Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: 81.3.3583.8005, Fax: 81.3.3586.2014, http://www.jsa.or.jp

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4.2.3 *bow, back surface, of a wafer* — the positive or negative deviation of the center point of the back surface of an unconstrained, horizontally positioned wafer from a back-surface reference plane established by three points within the boundary of the fixed quality area.

4.2.4 *bow, front surface, of a wafer* — the positive or negative deviation of the center point of the front surface of an unconstrained, horizontally positioned wafer from a front-surface reference plane established by three points within the boundary of the fixed quality area.

4.2.5 *constrained condition* — the state of a wafer under test, when one side of the wafer is clamped to an ideally flat surface; for example, when pulled down by a vacuum onto an ideally clean flat chuck.

4.2.6 *edge exclusion (EE), nominal* — the distance from the FQA boundary to the periphery of a wafer of nominal dimensions.

4.2.7 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal edge exclusion, EE, over which the specified values of a parameter apply. Because the nominal edge exclusion relates to the nominal diameter of a wafer, the size of the FQA is independent of wafer diameter and flat length tolerances.

4.2.8 *front surface* — the exposed surface upon which devices have been or will be fabricated.

NOTE 2: In cases where there is no difference between the front and back surfaces, then the surfaces may be determined arbitrarily, and are therefore interchangeable.

4.2.9 *lot* — for the purposes of commercial exchange of wafers, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above that have been identified by the supplier as constituting a lot.

4.2.10 *median surface, of a wafer* — the locus of points equidistant from the front and back surfaces of the wafer.

4.2.11 *reference plane* — a plane from which deviations of a specified surface of the wafer are measured.

4.2.12 *sapphire* — single crystal aluminum oxide (Al_2O_3) having a definite orientation.

4.2.13 *sori, of a wafer* — the algebraic difference between the most positive and most negative deviations of the front surface of a wafer that is not chucked from a reference plane that is a least squares fit to the front surface within the fixed quality area.

4.2.14 *substrate* — a wafer that is the basis for subsequent processing operations in the fabrication of devices.

4.2.15 *thickness, of a wafer* — the distance through the wafer between corresponding points on the front and back surfaces.

4.2.16 *total thickness variation (TTV)* — the difference between the maximum and minimum values of the thickness of a wafer within the fixed quality area.

4.2.17 *unconstrained condition* — the state of a wafer under test, when the wafer is in a stress-free condition with deformation due only to gravity.

4.2.18 *warp, back-surface, of a wafer* — the algebraic difference between the maximum most positive and minimum most negative deviations of all points of the back surface of an unconstrained, horizontally positioned wafer from a back-surface reference plane that is established by three points within the boundary of the fixed quality area.

4.2.19 *warp, of a wafer* — the difference between the maximum most positive and minimum most negative distances of the median surface of a free, unclamped wafer from a reference plane within the fixed quality area.

4.2.20 *warp, front-surface, of a wafer* — the algebraic difference between the maximum most positive and minimum most negative deviations of all points of the front surface of an unconstrained, horizontally positioned wafer from a front-surface reference plane that is established by three points within the boundary of the fixed quality area.

5 Ordering Information

5.1 Purchase orders for sapphire wafers furnished to these specifications shall include the following items:

5.1.1 Growth method,

5.1.2 Crystal orientation (see Appendix 1),

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5.1.3 Wafer surface orientation target and tolerance (see Appendix 1),

5.1.4 Nominal edge exclusion (see Appendix 2),

5.1.5 Wafer ID marking (see Appendix 3),

5.1.6 Front and back surface roughness,

5.1.7 Diameter and tolerance,

5.1.8 Type, dimensions, and orientation of orientation fiducial,

5.1.9 Edge chamfer (see Appendix 4),

5.1.10 Thickness and total thickness variation,

5.1.11 Wafer flatness, and

5.1.12 Wafer shape.

NOTE 3: The traditional wafer shape terms 'bow' and 'warp' are measures of median surface variations. Because the main concern with the shape of sapphire wafers is the manner that they are used in epitaxial deposition equipment, the back or front surface variation may be more significant than median surface variation. Therefore these terms have been modified to include the selection of the desired surface to be characterized.

5.2 In addition, the purchase order must indicate the test method to be used in evaluating each of these items.

5.3 Also, bulk and front and back surface defects, such as bubbles, scratches, edge chips and indents, and surface contamination requirements together with appropriate test methodology should be included in the purchase order.

NOTE 4: To be considered an edge chip the peripheral length and radial penetration must exceed a certain specified size.

5.4 The following items must also be included in the purchase order:

5.4.1 Sampling and lot acceptance procedures (see § 7),

5.4.2 Certification (if required) (see § 9), and

5.4.3 Packing and shipping container labeling requirements (see § 10).

5.5 Finally, several other characteristics may also be specified in purchase orders for sapphire wafers for any particular application. These can be selected from the items listed in the Sapphire Wafer Specification Format for Order Entry, Parts 1 and 2, which are given in Related Information 1 (see Table R1-1).

6 Requirements for Standardized Sapphire Wafers

6.1 *100 mm Sapphire Wafers for HB-LED Applications*

6.1.1 One type of 100 mm diameter single-side polished c-axis sapphire wafers is commonly used in the HB-LED industry. Double-side polished wafers are also used, but these are not directly covered by this Specification.

6.1.2 Specifications for this type of sapphire wafers are listed in Table 1. All of the parameters listed in the table should be included in the purchase order or contract. The item numbers in the left hand column are taken from Part 2 of Table R1-1, the Sapphire Wafer Specification Format for Order Entry.

6.1.2.1 Values for which standardized parameter values have been agreed upon are listed in Part a of the table.

6.1.2.2 Those necessary properties for which standardized values could not be agreed upon are listed "as specified in the purchase order or contract" in Part b of the table. Values may be inserted and the item moved to part a when agreement in the industry is achieved. Meanwhile, see Related Information 1 for guidance in selecting such values.

6.1.3 If other types of wafers are required for an application or for research purposes, these may be ordered through the use of the sapphire wafer specification format for order entry, found in Table R1-1 in Related Information 1.

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Table 1 Requirements for Flatted 100 mm Diameter, Polished Sapphire Wafers

Part a: Standardized Specifications

Item Number	*Property*	*Value*
	Wafer Category	*4a*
2-1.2	Crystal Orientation	c-axis ±0.1°
2-1.3.2	Wafer Surface Orientation Tolerance	±0.1°
2-1.6	Nominal Edge Exclusion	2 mm
2-3.1	Diameter	100.0 ± 0.1 mm
2-3.2	Orientation Fiducial	Flat
2-3.3	Flat Length	32.5 ± 1.0 mm
2-3.4	Flat Orientation	a-plane ± 0.3°
2-3.6	Thickness	650 ± 25 µm
2-3.7	Total Thickness Variation (TTV)	≤20 µm
2-3.9	Bow Tolerance[#1]	±10 µm
2-3.10	Warp[#2]	≤30 µm

Part b: Other Requirements to be Included in the Purchase Order or Contract

Item Number	*Property*	*Value*
2-1.3.1	Wafer Surface Orientation Target	as specified in the purchase order or contract
2-2.1	Wafer ID Marking	on front and/or back surface as specified in purchase order or contract
2-2.2	Front Surface Roughness[#4]	polished, $R_a \leq 0.3$ nm; over agreed spatial bandwidth
2-2.3	Back Surface Roughness[#4]	$0.6 \leq R_a \leq 1.2$ µm; over agreed spatial bandwidth
2-2.4	Back Surface Roughness Tolerance within a Wafer	±0.2 µm; over agreed spatial bandwidth
2-3.5	Edge Chamfer	as specified in the purchase order or contract
2-3.8	Bow Target[#1]	as specified in the purchase order or contract
2-3.11	Flatness, SBIR[#3]	as specified in the purchase order or contract
2-4.1	Scratches	as specified in the purchase order or contract
2-4.2	Edge Chips and Indents	as specified in the purchase order or contract
2-4.3	Surface Contamination	as specified in the purchase order or contract

#1 The surface associated with the wafer bow must be specified in the purchase order or contract. Because it is sometimes desired to specify a slightly positive or negative value for bow, the target value is listed as "as specified in the purchase order or contract" and the deviation from this value is limited to 10 µm larger or smaller, taking into account the sign of the bow. Note that in accordance with the wafer coordinate system defined in SEMI M20, positive values of bow denote a convex (mounded) front, median, or back surface when the wafer is positioned with its front surface up. Conversely, negative values of bow denote a concave (dished) median surface when the wafer is positioned with its front surface up.

#2 Again, the surface associated with the wafer warp must be specified in the purchase order or contract. Because warp can never be less than the magnitude of the bow of a wafer, no target value is specified. The maximum value of warp is given as 30 µm and the minimum value can never be less than 0 µm.

#3 See Appendix 1 of SEMI M1 for definitions of flatness algorithms.

#4 SEMI M40 provides guidance for measuring surface roughness.

6.2 *150 mm Sapphire Wafers for HB-LED Applications*

6.2.1 Four types of 150 mm diameter single-side polished c-axis sapphire wafers are commonly used in the HB-LED industry. There are two thicknesses (1,000 and 1,300 µm) and two types of fiducials (flat and notch). Double-side polished wafers are also used, but these are not directly covered by this Specification.

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6.2.2 Specifications for these four types of sapphire wafers are listed in Table 2. All of the parameters listed in the table should be included in the purchase order or contract. The item numbers in the left hand column are taken from Part 2 of Table R1-1, the Sapphire Wafer Specification Format for Order Entry.

6.2.2.1 Values for which standardized parameter values have been agreed upon are listed in Part a of the table.

6.2.2.2 Those necessary properties for which standardized values could not be agreed upon are listed "as specified in the purchase order or contract" in Part b of the table. Values may be inserted and the item moved to part a when agreement in the industry is achieved. Meanwhile, see Related Information 1 for guidance in selecting such values.

6.2.3 If other types of wafers are required for an application or for research purposes, these may be ordered through the use of the sapphire wafer specification format for order entry, found in Table R1-1 in Related Information 1.

Table 2 Requirements for 150 mm Diameter, Polished *c*-Axis Sapphire Wafers

Part a: Standardized Specifications

Item Number	*Property*	*Value*			
	Wafer Category	*6a*	*6b*	*6c*	*6d*
2-1.2	Crystal Orientation	c-axis ±0.1°			
2-1.3.2	Wafer Surface Orientation Tolerance	±0.1°			
2-1.6	Nominal Edge Exclusion	2 mm			
2-3.1	Diameter	150.0 ± 0.2 mm			
2-3.2	Orientation Fiducial	Flat	Flat	Notch	Notch
2-3.3	Flat Length	47.5 ± 2.5 mm		not applicable	
	Notch Depth	not applicable		1.00 mm +0.25 mm −0.00 mm	
	Notch Angle	not applicable		90° +5° −1°	
2-3.4	Flat Orientation	a-plane ± 0.3°		not applicable	
	Orientation of Notch Axis	not applicable		a-axis ± 0.3°	
2-3.5	Edge Chamfer	200 ± 50 µm			
2-3.6	Thickness	1,000 ± 25 µm	1,300 ± 25 µm	1,000 ± 25 µm	1,300 ± 25 µm
2-3.7	Total Thickness Variation (TTV)	≤20 µm			
2-3.9	Bow Tolerance[#1]	±10 µm			
2-3.10	Warp[#2]	≤30 µm			

Part b: Other Requirements to be Included in the Purchase Order or Contract

Item Number	*Property*	*Value*
2-1.1	Growth Process	as specified in the purchase order or contract
2-1.3.1	Wafer Surface Orientation Target	as specified in the purchase order or contract
2-2.1	Wafer ID Marking	on front and/or back surface as specified in purchase order or contract
2-2.2	Front Surface Roughness[#4]	polished, $R_a \leq 0.3$ nm; over agreed spatial bandwidth
2-2.3	Back Surface Roughness[4]	$0.6 \leq R_a \leq 1.2$ µm; over agreed spatial bandwidth
2-2.4	Back Surface Roughness Tolerance within a Wafer	±0.2 µm; over agreed spatial bandwidth
2-3.8	Bow Target[#1]	as specified in the purchase order or contract
2-3.11	Flatness, SBIR[#3]	as specified in the purchase order or contract
2-4.1	Scratches	as specified in the purchase order or contract
2-4.2	Edge Chips and Indents	as specified in the purchase order or contract
2-4.3	Surface Contamination	as specified in the purchase order or contract

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