

SEMI M1-90

SPECIFICATIONS FOR POLISHED MONOCRYSTALLINE SILICON WAFERS

1. Preface

1.1 These specifications cover requirements for monocrystalline high-purity silicon wafers used in semiconductor device manufacture. Dimensional and crystallographic orientation characteristics and limits on surface defects are the only standardized properties set forth below.

1.2 A complete purchase specification requires that additional physical properties be defined. These properties are listed, together with test methods suitable for determining their magnitude.

1.3 These specifications are directed specifically to silicon wafers with one polished surface. Wafers polished on both sides, or unpolished, or with epitaxial deposits are not covered. Values given for thickness, TTV, bow and warp apply only to wafers without back surface films or extrinsic gettering treatments. However, purchasers of such wafers may find these specifications to be a useful guide in defining their requirements.

1.4 For referee purposes, U.S. customary units shall be used for wafers of 2- and 3-inch nominal diameters, and SI (System International, commonly called metric) units for 80-mm and larger diameter wafers.

2. Applicable Documents

2.1 ASTM Standards¹

		F 28	Method for Measuring the Minority-Carrier Lifetime in Bulk Germanium and Silicon
		F 42	Test Methods for Conductivity Type of Extrinsic Semiconducting Materials
		F 43	Test Methods for Resistivity of Semiconductor Materials
		F 47	Test Method for Crystallographic Perfection of Silicon by Preferential Etch Techniques
		F 76	Test Methods for Measuring Hall Mobility and Hall Coefficient in Extrinsic Semiconductor Single Crystals
		F 81	Method for Measuring Radial Resistivity Variation on Silicon Slices
		F 84	Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array
		F 120	Practice for Determination of the Concentration of Impurities in Single Crystal Semiconductor Materials by Infrared Absorption Spectroscopy
		F 123	Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption
E 122	Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process	F 154	Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces
F 21	Test Method for Hydrophobic Surface Films by the Atomizer Test	F 391	Test Method for Minority Carrier Diffusion Length in Silicon by Measurement of Steady-State Surface Photovoltage
F 22	Test Method for Hydrophobic Surface Films by the Water-Break Test	F 398	Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wave Number or Wavelength of the Plasma Resonance Minimum
F 24	Method for Measuring and Counting Particulate Contamination on Surfaces		
F 26	Test Methods for Determining the Orientation of a Semiconductive Single Crystal		

¹ American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103 (All cited standards except for E 122 may be found in Volume 10.05 of the Annual Book of ASTM Standards; E 122 may be found in Volume 14.02.)



F 416	Test Method for Detection of Oxidation Induced Defects in Polished Silicon Wafers	F 1189	Test Method for Using Computer Assisted Infrared Spectrophotometry to Measure the Integrated Oxygen Content of Silicon Slices Polished on Both Sides
F 419	Test Method for Net Carrier Density in Silicon Epitaxial Layers by Voltage-Capacitance of Gated and Ungated Diodes	2.2	<i>DIN Standards</i> ²
F 523	Practice for Unaided Visual Inspection of Polished Silicon Slices	50430	Messung des spezifischen elektrischen Widerstandes von stabförmigen Einkristallen aus Silicium oder Germanium mit dem Zwei-Sonden-Gleichstrom-Verfahren (Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals in Bars by Means of the Two Point-Probe Direct Current Method)
F 533	Test Method for Thickness and Thickness Variation of Silicon Slices		
F 534	Test Method for Bow of Silicon Slices		
F 612	Practice for Cleaning Surfaces of Polished Silicon Slices		
F 613	Test Method for Measuring Diameter of Silicon Slices and Wafers	50431	Messung des spezifischen elektrischen Widerstandes von Einkristallen aus Silicium oder Germanium mit dem Vier-Sonden Gleichstrom-Verfahren bei linearer Anordnung der Sonden (Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Collinear Four Probe Array)
F 657	Test Method for Measuring Warp and Total Thickness Variation on Silicon Slices and Wafers by a Noncontact Scanning Method		
F 671	Test Method for Measuring Flat Length on Slices of Electronic Materials		
F 673	Test Method for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage	50432	Bestimmung des Leitungstyps von Silicium oder Germanium mittels Richttest oder Thermosonde (Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hotprobe)
F 775	Test Methods for Wafer and Slice Flatness by Interferometric Noncontact Technique	50433/1	Bestimmung der Orientierung von Einkristallen mit einem Roentgen-goniometer (Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction)
F 847	Test Methods for Crystallographic Orientation of Flats on Single Crystal Silicon Slices and Wafers by X-Ray Techniques		
F 928	Test Methods for Edge Contour of Silicon Wafers	50433/2	Bestimmung der Orientierung von Einkristallen nach der Lichtfigurenmethode (Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure)
F 951	Test Method for Radial Interstitial Oxygen Variation		
F 1188	Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption	50433/3	Bestimmung der Orientierung von Einkristallen mittels Laue Rück Strahlverfahren (Determination of the Orientation of Single Crystals by Means of Laue Back Scattering)

² DIN Standards - Deutsches Institut für Normung e.v., Beuth Verlag GmbH, Burggrafstrasse 4-10, D-1000 Berlin 30, Federal Republic of Germany

- 50434 Bestimmung der Kristallbaufehler einkristalliner Siliciumproben an geätzten (111)-Flächen (Determination of Crystal Perfection of Monocrystalline Silicon Samples on Etched (111)-Surfaces)
- 50435 Bestimmung der radialen Variation des spezifischen elektrischen Widerstandes an Silicium oder Germanium-Scheiben mit dem Vier-Sonden Gleichstromverfahren (Determination of the Radial Resistivity Variation of Silicon or Germanium Slices by Means of a Four-Point-DC-Probe)
- 50438/1 Bestimmung des Verunreinigungsgehaltes in Silicium mittels Infrarot-Absorption; Sauerstoff (Determination of Impurity Content in Silicon by Infrared Absorption; Oxygen)
- 50438/2 Bestimmung des Verunreinigungsgehaltes in Silicium mittels Infrarot Absorption; Kohlenstoff (Determination of Impurity Content in Silicon by Infrared Absorption; Carbon)
- 50440/1 Messung der Rekombinations-Tragerlebensdauer in Silicium-Einkristallen nach der Photoleitfähigkeitsmethode; Messung an quaderförmigen Testproben (Measurement of Recombination Carrier Lifetime in Silicon Single Crystals by Means of Photoconductive Decay Method; Measurement on Bar-Shaped Test Samples)
- 50441/1 Messung der geometrischen Dimensionen von Halbleiter-scheiben; Messung der Dicke (Measurement of the Geometric Dimensions of Semiconductor Slices; Measurement of Thickness)
- 50441/2 Messung der geometrischen Dimensionen von Halbleiter-scheiben; Prüfung der Kantenverrundung (Measurement of the Geometric Dimensions of Semiconductor Slices; Testing of Edge Rounding)
- 2.3 JIS Standard**
- H 0611 Methods of Measurement of Thickness Taper and Bow for Silicon Wafers³
- 2.4 SEMI Standard**
- SEMI M13 Specification for Alphanumeric Marking of Silicon Wafers
- 2.5 Other Standard**
- MIL-STD-105D Sampling Procedures and Tables for Inspection by Attributes⁴
- 3. Definitions**
- dopant* - a chemical element, usually from the third or fifth columns of the periodic table, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.
- fixed quality area (FQA)* - that portion of the area of a wafer surface, defined by a nominal edge exclusion, X, over which the specified values of a parameter apply. The FQA lies within and is at all points the distance X (the nominal edge exclusion) away from the periphery of a wafer of nominal dimensions. (See Figure 1.)
- NOTE 1 - The FQA is independent of wafer diameter and flat length tolerances. For the purpose of defining the FQA, the wafer periphery at locations with notch fiducials is assumed to follow the circumference of a circle with diameter equal to the nominal wafer diameter.
- flatness* - for wafer surfaces, the deviation of the front surface, expressed in TIR or maximum FPD relative to a specified reference plane when the back surface of the wafer is ideally flat, as when pulled down by a vacuum onto an ideally clean flat chuck.
- NOTE 2 - The flatness of a wafer may be described as either:
1. The global flatness, or
 2. The maximum value of site flatness as measured on all sites, or
 3. The percentage of sites which have a site flatness equal to or less than a specified value.
- focal plane* - the plane perpendicular to the optical axis of an imaging system which contains the focal point of the imaging system.
- NOTE 3 - The reference plane used by an imaging system is coincident with or parallel with the focal plane. Full field imaging systems employ coincident global focal and reference planes. Partial field imaging systems employ either coincident site focal and reference planes or displaced site focal and global reference planes. If the

³ Japanese Standards Association, 1-24, Akasaka 4 Chome, Minato-ku, Tokyo, 107 JAPAN
⁴ Naval Publication and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120



reference plane is not coincident with the focal plane, it is displaced from the focal plane so that the point on the front surface at a site center lies in the focal plane.

focal plane deviation (FPD) - the distance parallel to the optical axis from a point on the wafer surface to the focal plane.

global flatness - the TIR or the maximum FPD relative to a specified reference plane within the FQA.

lot - for the purposes of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

maximum FPD - the largest of the absolute values of the focal plane deviations.

orthogonal misorientation - in wafers cut intentionally "off orientation", the angle between the projection of the vector normal to the wafer surface onto a {111} plane and the projection on that plane of the nearest <110> direction. (See Figure 2.)

reference plane - a plane defined by one of the following:

1. Three points at specified locations on the front surface of the wafer, or
2. The least squares fit to the front surface of the wafer using all points within the FQA, or
3. The least squares fit to the front surface of the wafer using all points within a site, or
4. An ideal back surface (equivalent to the ideally flat chuck surface that contacts the wafer).

NOTE 4 - The specified reference plane should be chosen with due regard for the capabilities of the imaging system. Front surface or back surface reference planes should be selected depending on the wafer mounting system. If the wafer cannot be gimbaled in the imaging system, a back surface reference plan should be specified.

shape - for wafer surfaces, the deviation of a specified wafer surface relative to a specified reference plane when the wafer is in an unclamped condition, expressed as the range or total indicator reading (TIR) or as the maximum reference plane deviation (maximum RPD) within the specified fixed quality area.

NOTE 5 - This definition is analogous to the definition of flatness, which applies to the front surface geometry when the wafer is in the clamped condition.

site - a rectangular area, on the front surface of the wafer, whose sides are parallel and perpendicular to the primary

(orientation) flat or to the notch bisector, and whose center falls within the FQA.

site array - a set of contiguous sites.

site flatness - the TIR or the maximum FPD of the portion of a site which falls within the FQA.

sori - the difference between the maximum and minimum distances between a front surface reference plane and the surface of a wafer which is not chucked. The reference plane is chosen either so that the difference (sori) is minimized or as a least-squares fit to the front surface.

total indicator reading (TIR) - the smallest perpendicular distance between two planes, both parallel with the reference plane, which enclose all points on the front surface of a wafer within the FQA or the site, depending on which is specified.

4. Wafer Ordering Information

4.1 Purchase orders for silicon wafers furnished to this specification shall include the following items:

4.1.1 Nominal diameter (see applicable polished silicon wafer standard).

4.1.2 Crystal growth method (see NOTE 6).

4.1.3 Surface orientation (see applicable polished silicon wafer standard).

4.1.4 Conductivity type (see applicable polished silicon wafer standard) and dopant (see NOTE 6).

4.1.5 Resistivity or resistivity range.

4.1.6 Lot acceptance procedures (see Section 8).

4.1.7 Certification (if required) (see Section 11).

4.1.8 Packing and marking (see Section 12).

4.1.9 Selection of test method to be used in evaluating those items for which alternate tests exist (see Section 9).

4.2 *Optional Criteria* - The following items may be specified optionally in addition to those listed above.

4.2.1 Doping method and thermal treatment (see NOTE 6).

4.2.2 Radial resistivity variation.

4.2.3 Crystal perfection.

4.2.4 Impurities other than common doping elements such as oxygen and carbon.

4.2.5 Flatness - the following conditions must be specified in connection with flatness measurement:



- A. Type of Measurement:
 - 1. Global flatness
 - 2. Maximum site or flatness
 - 3. Percentage of sites within specification
- B. Parameter: TIR or maximum FPD
- C. Nominal Edge Exclusion: X
- D. For site flatness (where specified):
 - 1. Site Dimension x, y
 - 2. Array pattern and location relative to FQA center
- E. Reference Plane:
 - 1. Three point (also, specify point locations)
 - 2. Least squares fit to the front surface within the FQA
 - 3. Least squares fit to the front surface within a site
 - 4. Ideal back surface
- F. Focal Plane:
 - 1. Global
 - 2. Site

4.2.6 Edge contour

4.2.7 Hall or conductivity mobility (see NOTE 7)

4.2.8 Diffusion length (see NOTE 7)

4.2.9 Minority carrier lifetime (see NOTE 7)

NOTE 6 - The dopant, crystal growth method (for example, Czochralski or floating zone), and doping method (for example, ion implantation, neutron transmutation, etc.) with subsequent heat treatment are difficult to ascertain in the finished wafers. Verification test procedures or certification of these characteristics (see Section 11) shall be agreed upon between the supplier and the purchaser.

NOTE 7 - Items 4.2.7, 4.2.8, and 4.2.9 are less commonly specified than the others, but are included for completeness as parameters for which methods of evaluation have been developed.

5. Dimensions and Permissible Variations

5.1 The material shall conform to the dimensions and dimensional tolerances as specified in the polished silicon wafer standard applicable to the specified nominal diameter.

NOTE 8 - Wafers of the same nominal diameter may typically have different dimensional configurations in different regions of the world. Many of these configurations are represented in this specification. In

selecting the appropriate polished wafer standard, consideration should be given to compatibility with processes and equipment generally available in the region of use.

5.1.1 Sori is an attribute that may be specified between the supplier and the purchaser in lieu of bow or warp or both.

5.2 If edge contoured wafers are specified on the purchase order, the profile shall conform to the following requirements at all points on the wafer periphery (except interior portions of notches, if present).

5.2.1 When the wafer is aligned with the SEMI Wafer Edge Profile Template (see Figure 3) so that the x-axis of the template is coincident with the wafer surface and the y-axis of the template is tangent with the outermost radial portion of the contour, the wafer edge profile must be contained within the clear region of the template. (See Figure 4 for examples of acceptable and unacceptable contours.)

5.2.2 No sharp points or protrusions are permitted anywhere on the wafer edge contour.

5.2.3 Cosmetic attributes of the edge contour are not covered by this specification. They shall be agreed upon between supplier and purchaser.

5.3 Fiducial indications shall conform to the requirements of the appropriate polished silicon wafer standard.

5.3.1 Where secondary flats are specified, they shall be located as shown in Figure 5.

5.3.2 Where notches are specified, they shall conform to the dimensions in Figure 6.

5.4 Where alphanumeric marking is specified, the code character properties and code field location shall conform to SEMI M13.

6. Materials and Manufacture

6.1 The material shall consist of wafers from ingots grown by the process specified in the purchase order or contract.

7. Physical Requirements

7.1 The material shall conform to the crystallographic orientation details as specified in the appropriate polished silicon wafer standard.

7.2 The material shall conform to the details specified in the purchase order or contract, as follows:

7.2.1 Conductivity type and dopant (see NOTE 6),

7.2.2 Resistivity,

NOTE 13 - Resistivity of wafers is most appropriately determined for referee purposes by ASTM Method F 84 or DIN 50431. Under some circumstances these tests may be considered destructive, and an alternative means may be required. One nondestructive test is ASTM Test Method F 673, having a range from 0.0001 to 100 ohm cm. Another nondestructive test is ASTM Test Method F 398. This method is limited to carrier concentrations in the ranges from 1.5×10^{18} to 1.5×10^{21} cm^{-3} for *n*-type silicon and from 3×10^{18} to 5×10^{20} cm^{-3} for *p*-type, and has only moderate inter-laboratory precision. Other available methods include ASTM Test Method F 43 or DIN 50430 (referee methods requiring a bar-shaped sample) and ASTM Test Method F 419 (which is destructive, and of limited range).

9.12 *Radial Resistivity Variation* - Determine in accordance with ASTM Method F 81 or DIN 50435.

9.13 *Crystal Perfection* - Determine in accordance with ASTM Test Method F 47 or DIN 50434 (to determine grain boundaries, twinning, slip, dislocations and lineage) and ASTM Test Method F 416 (to determine oxidation induced defects).

9.14 *Other Impurities* - Determine by methods agreed upon between the supplier and the purchaser.

NOTE 14 - General infrared techniques are given in ASTM Practice F 120. ASTM Test Methods F 1188 and F 1189 and DIN 50438/1 are specific tests for oxygen, and ASTM Test Method F 123 and DIN 50438/2 are specific for carbon; special thick test specimens are necessary. Radial variation of oxygen may be determined in accordance with ASTM Test Method F 951.

9.15 *Flatness* - Determine by a method agreed upon between the supplier and the purchaser.

NOTE 15 - Flatness may be determined for referee purposes by ASTM Test Method F 775. Many commercially available flatness measurement instruments are based on principles other than the interferometric technique underlying ASTM Test Method F 775. Although these other methods have not been standardized, they are widely used.

9.16 *Edge Contour* - Determine in accordance with ASTM Test Methods F 928 or DIN 50441/2.

9.17 *Mobility* - If Hall mobility is specified, determine in accordance with ASTM Test Methods F 76; if conductivity mobility is specified, determine by a method agreed upon between the supplier and the purchaser.

9.18 *Diffusion Length* - Determine in accordance with ASTM Test Method F 391.

9.19 *Minority Carrier Lifetime* - Determine in accordance with ASTM Method F 28 or DIN 50440/1; special test specimens are required.

10. Standard Defect Limits

10.1 Definitions for the Polished Wafer Defect terms in Table 1 are given in ASTM Practices F 154 and F 523 and in ASTM Test Method F 416.

10.2 *Minimal Conditions or Dimensions* - Minimal conditions or dimensions for defects are stated below and shall be used for determining wafer acceptability. Anomalies smaller than these limits shall not be considered defects.

area contamination - any foreign matter on the surface in localized areas which is revealed under the inspection lighting conditions as discolored, mottled or cloudy appearance resulting from smudges, stains, water spots, etc.

crack - any anomaly conforming to the definition and greater than 0.010 inch (0.25 mm) in total length.

crater - any individually distinguishable surface anomaly conforming to the definition and visible when viewed under diffused illumination.

crow's foot - any anomaly conforming to the definition and greater than 0.010 inch (0.25 mm) in total length.

dimple - any smooth surface depression greater than 3 mm in diameter.

edge chip and indent - any edge anomaly including saw exit marks conforming to the definition and greater than 0.010 inch (0.25 mm) in radial depth and peripheral length.

groove - any anomaly conforming to the definition and greater than 0.0005 inch (0.13 mm) wide or 0.030 inch (0.76 mm) in length.

haze - haze is indicated when the image of a narrow beam tungsten lamp filament is detectable on the polished wafer surface. (Under some conditions contamination may appear as haze.)

mound - any anomaly conforming to the definition and greater than 0.010 inch (0.25 mm) in maximum dimension.

orange peel - any visually detectable roughened surface conforming to the definition and observable under diffused illumination.

particulate contamination - distinct particles resting on the surface which are revealed under collimated light as bright points.