



SEMI M1-94

SPECIFICATIONS FOR POLISHED MONOCRYSTALLINE SILICON WAFERS

1 Preface

1.1 These specifications cover requirements for monocrystalline high-purity silicon wafers used in semiconductor device manufacturing. Dimensional and crystallographic orientation characteristics and limits on surface defects are the only standardized properties set forth below.

1.2 A complete purchase specification requires that additional physical properties be specified along with test methods suitable for determining their magnitude. SEMI M18 provides a comprehensive listing of such properties and associated test methods and may be used for this purpose (see also Section 4).

1.3 These specifications apply specifically to silicon wafers with one chem-mechanically polished surface. Wafers polished on both sides, or unpolished, or with epitaxial deposits are not covered. Values given for thickness, TTV, bow, and warp apply only to wafers without back surface films or extrinsic gettering treatments. However, purchasers of such wafers may find these specifications to be a useful guide in defining their requirements.

1.4 For referee purposes, U.S. customary units shall be used for wafers of 2- and 3-inch nominal diameters, and SI (System International, commonly called metric) units for 80 mm and larger diameter wafers.

2 Applicable Documents

2.1 ASTM Standards¹

E 122 — Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process

F 21 — Test Method for Hydrophobic Surface Films by the Atomizer Test

F 22 — Test Method for Hydrophobic Surface Films by the Water-Break Test

F 24 — Method for Measuring and Counting Particulate Contamination on Surfaces

¹ American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103 (All cited standards except for *E 122* may be found in Volume 10.05 of the Annual Book of ASTM Standards; *E 122* may be found in Volume 14.02.)

F 26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

F 28 — Method for Measuring the Minority-Carrier Lifetime in Bulk Germanium and Silicon

F 42 — Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

F 43 — Test Methods for Resistivity of Semiconductor Materials

F 47 — Test Method for Crystallographic Perfection of Silicon by Preferential Etch Techniques

F 76 — Test Methods for Measuring Hall Mobility and Hall Coefficient in Extrinsic Semiconductor Single Crystals

F 81 — Method for Measuring Radial Resistivity Variation on Silicon Slices

F 84 — Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array

F 120 — Practice for Determination of the Concentration of Impurities in Single Crystal Semiconductor Materials by Infrared Absorption Spectroscopy

F 154 — Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

F 391 — Test Method for Minority Carrier Diffusion Length in Silicon by Measurement of Steady-State Surface Photovoltage

F 398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wave Number or Wavelength of the Plasma Resonance Minimum

F 416 — Test Method for Detection of Oxidation Induced Defects in Polished Silicon Wafers

F 419 — Test Method for Net Carrier Density in Silicon Epitaxial Layers by Voltage-Capacitance of Gated and Ungated Diodes

F 523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

F 533 — Test Method for Thickness and Thickness Variation of Silicon Slices



- F 534* — Test Method for Bow of Silicon Slices
- F 612* — Practice for Cleaning Surfaces of Polished Silicon Slices
- F 613* — Test Method for Measuring Diameter of Silicon Slices and Wafers
- F 657* — Test Method for Measuring Warp and Total Thickness Variation on Silicon Slices and Wafers by a Noncontact Scanning Method
- F 671* — Test Method for Measuring Flat Length on Slices of Electronic Materials
- F 673* — Test Method for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage
- F 775* — Test Methods for Wafer and Slice Flatness by Interferometric Noncontact Technique
- F 847* — Test Methods for Crystallographic Orientation of Flats on Single Crystal Silicon Slices and Wafers by X-Ray Techniques
- F 928* — Test Methods for Edge Contour of Silicon Wafers
- F 951* — Test Method for Radial Interstitial Oxygen Variation
- F 1188* — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption
- F 1189* — Test Method for Using Computer-Assisted Infrared Spectrophotometry to Measure the Integrated Oxygen Content of Silicon Slices Polished on Both Sides
- F 1241* — Terminology of Silicon Technology
- F 1366* — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectroscopy
- F 1388* — Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of MOS (Metal-Oxide-Silicon) Capacitors
- F 1390* — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning
- F 1391* — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption
- 50430* — Messung des spezifischen elektrischen Widerstandes von stabförmigen Einkristallen aus Silicium oder Germanium mit dem Zwei-Sonden-Gleichstrom-Verfahren (Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals in Bars by Means of the Two Point-Probe Direct Current Method)
- 50431* — Messung des spezifischen elektrischen Widerstandes von Einkristallen aus Silicium oder Germanium mit dem Vier-Sonden Gleichstrom-Verfahren bei linearer Anordnung der Sonden (Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Collinear Four Probe Array)
- 50432* — Bestimmung des Leitungstyps von Silicium oder Germanium mittels Richttest oder Thermosonde (Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hot-Probe)
- 50433/1* — Bestimmung der Orientierung von Einkristallen mit einem Roentgengoniometer (Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction)
- 50433/2* — Bestimmung der Orientierung von Einkristallen nach der Lichtfiguren-methode (Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure)
- 50433/3* — Bestimmung der Orientierung von Einkristallen mittels Laue-Rückstrahl-verfahren (Determination of the Orientation of Single Crystals by Means of Laue Back Scattering)
- 50434* — Nachweis von Kristalldefekten in Silizium-Einkristallen mittels Ätztechnik an {111}- und {100}-Flächen (Detection of Crystal Defects in Silicon Monocrystals by Etching on {111} and {100} Surfaces)
- 50435* — Bestimmung der radialen Variation des spezifischen elektrischen Widerstandes an Silicium oder Germanium-Scheiben mit dem Vier-Sonden-Gleichstromverfahren (Determination of the Radial Resistivity Variation of Silicon or Germanium Slices by Means of a Four- Point-DC-Probe)
- 50438/1* — Bestimmung des Verunreinigungs-gehaltes in Silicium mittels Infrarot Absorption; Sauerstoff

2.2 DIN Standards²

² DIN Standards, Deutsches Institut für Normung e.v., available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-1000 Berlin 30, Federal Republic of Germany



(Determination of Impurity Content in Silicon by Infrared Absorption; Oxygen)

50438/2 — Bestimmung des Verunreinigungs-gehaltes in Silicium mittels Infrarot Absorption; Kohlenstoff (Determination of Impurity Content in Silicon by Infrared Absorption; Carbon)

50440/1 — Messung der Rekombinations-Tragerlebensdauer in Silicium-Einkristallen nach der Photoleitfähigkeitsverfahren; Messung an quaderförmigen Proben (Measurement of Recombination Carrier Lifetime in Silicon Single Crystals by Means of Photoconductive Decay Method; Measurement on Bar-Shaped Test Samples)

50441/1 — Messung der geometrischen Dimensionen von Halbleiterscheiben; Messung der Dicke (Measurement of the Geometric Dimensions of Semiconductor Slices; Measurement of Thickness)

50441/2 — Messung der geometrischen Dimensionen von Halbleiterscheiben; Prüfung der Kantenverrundung (Measurement of the Geometric Dimensions of Semiconductor Slices; Testing of Edge Rounding)

50441/4 — Messung der geometrischen Dimensionen von Halbleiterscheiben: Scheibendurchmesser und Flattiefe (Measurement of the Geometrical Dimensions of Semiconductor Slices: Diameter and Flat Depth of Slices)

2.3 JIS Standard³

H 0611 — Methods of Measurement of Thickness Taper and Bow for Silicon Wafers

2.4 SEMI Standards

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

2.5 Other Standard⁴

MIL-STD-105E — Sampling Procedures and Tables for Inspection by Attributes

³ Japanese Standards Association, 1-24, Akasaka 4 Chome, Minato-ku, Tokyo, 107 JAPAN

⁴ Naval Publication and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120

3 Definitions

3.1 Many terms relating to silicon technology are defined in ASTM Terminology F 1241.

3.2 Definitions for many of the Polished Wafer Defect terms in Table 1 are given in ASTM Practices F 154 and F 523 and in ASTM Test Method F 416.

3.3 Other terms are defined as follows:

acceptor — an impurity in a semiconductor which accepts electrons excited from the valence band, leading to hole conduction.

anisotropic, in semiconductor technology — exhibiting different physical properties in differing crystallographic directions.

anisotropic etch — a selective etch which exhibits an accelerated etch rate along specific crystallographic directions.

NOTE 1 — Anisotropic etches are used to determine crystal orientation, to fabricate micromechanical structures, and to facilitate dielectric component isolation.

azimuth, in ellipsometry — the angle between the major axis of the ellipse and the plane of incidence.

backside — not preferred, use *back surface* as defined in ASTM Terminology F 1241.

bipolar — semiconductor device fabrication technology which produces transistors that use both holes and electrons as charge carriers.

carrier, in semiconductor materials — an entity capable of carrying electric charge through a solid, for example, valence holes and conduction electrons in semiconductors; charge carrier.

chem-mechanical polish, in semiconductor technology — a process for the removal of surface material from the wafer which utilizes chemical and mechanical actions to achieve a mirror-like surface for subsequent processing.

chuck mark — any physical mark on either surface of a wafer caused by a robotic end effector, chuck, or wand.

cleavage plane — a crystallographically preferred fracture plane.

conductivity (electrical) — a measure of the ease with which charge carriers flow in a material; the reciprocal of resistivity.



NOTE 2 — In a semiconductor, the conductivity is proportional to the product of free carrier density, electron electrical, and carrier mobility. Most variant of all crystal properties, conductivity can range over 13 orders of magnitude. Conductivity can be locally modified by temperature, carrier injection, irradiation, or magnetic field. Symbol is σ and units are $(\Omega \cdot \text{cm})^{-1}$.

conductivity type, of a semiconductor crystal or wafer — a property that identifies the majority charge carrier in the semiconductor; see also *n-type*, *p-type*.

contaminant, area — foreign matter visible to the unaided eye under high-intensity (narrow-beam) illumination on the wafer of extent greater than a single light point defect.

contaminant, particulate — see *light point defect*.

crystal defect — departure from the ideal arrangement of atoms in a crystal.

crystal indices — see *Miller indices*.

crystallographic notation — a symbolism based on Miller indices used to label planes and directions in a crystal as follows:

plane	(111)
family of planes	{111}
direction	[111]
family of directions	<111>

depletion layer — a region in which the mobile carrier charge density is not sufficient to neutralize the net fixed charge density of donors and acceptors; barrier layer; blocking layer; space-charge layer.

dimple — a shallow depression with gently sloping sides that exhibits a concave, spheroidal shape and is visible to the unaided eye under proper lighting conditions.

donor — an impurity or imperfection in a semiconductor which donates electrons to the conduction band, leading to electron conduction.

dopant — a chemical element, usually from the third or fifth columns of the periodic table, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

doping — addition of specific impurities to a semiconductor to control the electrical resistivity.

edge profile — on edge contoured wafers (whose edges have been shaped chemically or mechanically), a description of the contour of the boundary of the wafer that joins the front and back surfaces.

etch — a solution, a mixture of solutions, or a mixture of gases that attacks the surfaces of a film or substrate, removing material either selectively or nonselectively; see also *anisotropic etch*, *preferential etch*.

fixed quality area (FQA) — the central area of a wafer surface, defined by a nominal edge exclusion, X, over which the specified values of a parameter apply.

NOTE 3 — The boundary of the FQA is at all points the distance X away from the periphery of a wafer of nominal dimensions. (See Figure 1.) The size of the FQA is independent of wafer diameter and flat length tolerances. For the purpose of defining the FQA, the wafer periphery at locations with notch fiducials is assumed to follow the circumference of a circle with diameter equal to the nominal wafer diameter.

flat, on a semiconductor wafer — a portion of the periphery of a circular wafer that has been removed to a chord; see also *primary orientation flat*, *secondary flat*.

flat diameter — the linear dimension across the surface of a semiconductor wafer from the center of the flat through the wafer center to the circumference of the wafer on the opposite edge along the diameter perpendicular to the flat. (See Figure 3.)

NOTE 4 — The flat diameter may be associated with the primary orientation flat, with a secondary flat, if present, or with any other flat, if present. In such cases, the term may be modified as *primary orientation flat diameter*, *secondary flat diameter*, etc. In the case of opposing primary orientation and secondary flats, as occurs on [100] *n*-type wafers 125 mm and smaller in diameter, the concept of flat diameter does not apply because the diameter perpendicular to the flats does not intersect the wafer circumference.

flatness — for wafer surfaces, the deviation of the front surface, expressed in TIR or maximum FPD relative to a specified reference plane when the back surface of the wafer is ideally flat, as when pulled down by a vacuum onto an ideally clean flat chuck.

NOTE 5 — The flatness of a wafer may be described as either:



1. The global flatness, or
2. The maximum value of site flatness as measured on all sites, or
3. The percentage of sites which have a site flatness equal to or less than a specified value.

focal plane — the plane perpendicular to the optical axis of an imaging system which contains the focal point of the imaging system.

NOTE 6 — The reference plane used by an imaging system is coincident with or parallel with the focal plane. Full field imaging systems employ coincident global focal and reference planes. Partial field imaging systems employ either coincident site focal and reference planes or displaced site focal and global reference planes. If the reference plane is not coincident with the focal plane, it is displaced from the focal plane so that the point on the front surface at a site center lies in the focal plane.

focal plane deviation (FPD) — the distance parallel to the optical axis from a point on the wafer surface to the focal plane.

four-point probe — an electrical probe arrangement for determining the resistivity of a material in which separate pairs of contacts are used (1) for passing current through the specimen and (2) measuring the potential drop caused by the current.

front side — not preferred; use *front surface* as defined in ASTM Terminology F 1241.

global flatness — the TIR or the maximum FPD relative to a specified reference plane within the FQA.

goniometer — an instrument to measure angles.

NOTE 7 — Goniometers are frequently used with x-ray diffraction equipment to measure crystal axis angles or for optical angle measurement.

gradient, resistivity — not preferred; see *resistivity variation*.

groove, in a semiconductor wafer — a shallow scratch with rounded edges that is usually the remnant of a scratch not completely removed by polishing.

hole — a mobile vacancy in the electronic valence structure of a semiconductor which acts like a positive electron charge with positive mass; the majority carrier in *p*-type material.

ingot, in silicon technology — a cylinder or rectangular solid of polycrystalline or single crystal silicon, generally of slightly irregular dimensions.

NOTE 8 — Silicon wafers are usually sliced from cylindrical single-crystal ingots that have been ground to a uniform diameter prior to slicing.

light point defect — an isolated, localized anomaly, such as a particle or pit on or in a wafer, resulting in increased light scattering intensity relative to that of the surrounding wafer surface. Contrast with *point defect*.

lot — for the purposes of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

majority carrier — type of charge carrier constituting more than one half the total charge-carrier concentration (e.g., holes in *p*-type material).

maximum FPD — the largest of the absolute values of the focal plane deviations.

Miller indices, of a crystallographic plane — the smallest integers proportional to the reciprocals of the intercepts of the plane on the three crystal axes of unit length.

minority carrier — type of charge carrier constituting less than one half the total charge-carrier concentration (e.g., electrons in *p*-type material).

notch, on a semiconductor wafer — an intentionally fabricated indent of specified shape and dimensions oriented such that the diameter passing through the center of the notch is parallel with a specified low index crystal direction.

orthogonal misorientation — in wafers cut intentionally "off orientation," the angle between the projection of the vector normal to the wafer surface onto a {111} plane and the projection on that plane of the nearest <110> direction. (See Figure 2.)

point defect — a localized crystal defect such as a lattice vacancy, interstitial atom, or substitutional impurity. Contrast with *light point defect*.

preferential etch — a selective etch that etches regions of different crystal strain or conductivity at different



rates, used to delineate crystal defects or regions of differing conductivity on wafer surfaces.

primary orientation flat — the flat of longest length on the wafer, oriented such that the chord is parallel with a specified low index crystal plane; *major flat*.

radial gradient — not preferred; see *resistivity variation*.

reference plane — a plane defined by one of the following:

1. Three points at specified locations on the front surface of the wafer, or
2. The least squares fit to the front surface of the wafer using all points within the FQA, or
3. The least squares fit to the front surface of the wafer using all points within a site, or
4. An ideal back surface (equivalent to the ideally flat chuck surface that contacts the wafer).

NOTE 9 — The specified reference plane should be chosen with due regard for the capabilities of the imaging system. Front surface or back surface reference planes should be selected depending on the wafer mounting system. If the wafer cannot be gimbaled in the imaging system, a back surface reference plane should be specified.

profilometer — an instrument for measuring the topographical profile of a surface.

resistivity, (electrical) — The measure of difficulty with which charged carriers flow through a material; the reciprocal of *conductivity*.

NOTE 10 — The resistivity of a semiconductor or other material is the ratio of the potential gradient (electric field) parallel with the current to the current density. Symbol is σ and units are ($\Omega \cdot \text{cm}$).

secondary flat — a flat of length shorter than the primary orientation flat, whose position with respect to the primary orientation flat identifies the type and orientation of the wafer.

shape — for wafer surfaces, the deviation of a specified wafer surface relative to a specified reference plane when the wafer is in an unclamped condition, expressed as the range or total indicator reading (TIR) or as the maximum reference plane deviation (maximum RPD) within the specified fixed quality area.

NOTE 11 — This definition is analogous to the definition of flatness, which applies to the front surface geometry when the wafer is in the clamped condition.

site — a rectangular area, on the front surface of the wafer, whose sides are parallel and perpendicular to the primary orientation flat or to the notch bisector, and whose center falls within the FQA.

site array — a set of contiguous sites.

site flatness — the TIR or the maximum FPD of the portion of a site which falls within the FQA.

NOTE 12 — Precise site flatness measurement requires measurement points located closely enough to reveal the surface topology in detail. It is recommended that site flatness be measured using a data point array with adjacent points separated by 2 mm or less. It is also recommended that the data set used to calculate site flatness have data at each site corner and along each site boundary. This makes the effective site measurement area equal to the site size.

smudge — dense local area of contamination usually caused by handling or fingerprints.

sori — the sum of the magnitudes of the maximum positive and maximum negative distances from the front surface of a wafer that is not chucked to a reference plane that is a least-squares fit to the front surface.

total indicator reading (TIR) — the smallest perpendicular distance between two planes, both parallel with the reference plane, which enclose all points on the front surface of a wafer within the FQA or the site, depending on which is specified.

waves — uneven contours in the surface of a wafer visible to the unaided eye under large-area diffuse illumination.

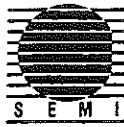
4 Wafer Ordering Information

4.1 Purchase orders for silicon wafers furnished to this specification shall include the following items:

4.1.1 Nominal diameter (see applicable polished silicon wafer standard).

4.1.2 Crystal growth method (see Note 13).

4.1.3 Surface orientation (see applicable polished silicon wafer standard).



4.1.4 Conductivity type (see applicable polished silicon wafer standard) and dopant (see Note 13).

4.1.5 Resistivity or resistivity range.

4.1.6 Lot acceptance procedures (see Section 8).

4.1.7 Certification (if required) (see Section 11).

4.1.8 Packing and marking (see Section 12).

4.1.9 Selection of test method to be used in evaluating those items for which alternate tests exist (see Section 9).

4.2 *Optional Criteria* — The following items may be specified optionally in addition to those listed above.

4.2.1 Doping method and thermal treatment (see Note 13).

4.2.2 Radial resistivity variation.

4.2.3 Crystal perfection.

4.2.4 Impurities other than common doping elements such as oxygen and carbon.

4.2.5 *Flatness* — The following conditions must be specified in connection with flatness measurement:

A. Type of Measurement

1. Global flatness
2. Maximum site flatness
3. Percentage of sites within specification

B. Parameter: TIR or maximum FPD

C. Nominal Edge Exclusion: X

D. For site flatness (where specified):

1. Site Dimension: x, y
2. Array pattern and location relative to FQA center

E. Reference Plane:

1. Three point (also, specify point locations)
2. Least squares fit to the front surface within the FQA
3. Least squares fit to the front surface within a site
4. Ideal back surface

F. Focal Plane:

1. Global

2. Site

4.2.6 Edge contour

4.2.7 Hall or conductivity mobility (see Note 14)

4.2.8 Diffusion length (see Note 14)

4.2.9 Minority carrier lifetime (see Note 14)

NOTE 13 — The dopant, crystal growth method (for example, Czochralski or floating zone), and doping method (for example, ion implantation, neutron transmutation, etc.) with subsequent heat treatment are difficult to ascertain in the finished wafers. Verification test procedures or certification of these characteristics (see Section 11) shall be agreed upon between the supplier and the purchaser.

NOTE 14 — Items 4.2.7, 4.2.8, and 4.2.9 are less commonly specified than the others, but are included for completeness as parameters for which methods of evaluation have been developed.

5 Dimensions and Permissible Variations

5.1 The material shall conform to the dimensions and dimensional tolerances as specified in the polished silicon wafer standard applicable to the specified nominal diameter.

NOTE 15 — Wafers of the same nominal diameter may typically have different dimensional configurations in different regions of the world. Many of these configurations are represented in this specification. In selecting the appropriate polished wafer standard, consideration should be given to compatibility with processes and equipment generally available in the region of use.

5.1.1 Sori is an attribute that may be specified between the supplier and the purchaser in lieu of bow or warp or both.

5.1.2 If bow is specified, a sign may be included in the specification to denote convex (positive) or concave (negative) curvature of the median surface of the wafer with the front surface up. If no sign is included in the specification, bow may vary between -a and +a, where "a" is the specified maximum magnitude of bow.

5.2 If edge contoured wafers are specified on the purchase order, the profile shall conform to the following requirements at all points on the wafer periphery (except interior portions of notches, if present).