SEMI M1-0302
SPECIFICATIONS FOR POLISHED MONOCRYSTALLINE SILICON WAFERS

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1 Purpose

1.1 These specifications cover requirements for monocrystalline high-purity silicon wafers used in semiconductor device manufacturing. Dimensional and crystallographic orientation characteristics and limits on surface defects are the only standardized properties set forth below.

1.2 A complete purchase specification requires that additional physical properties be specified along with test methods suitable for determining their magnitude. SEMI M18 provides a comprehensive listing of such properties and associated test methods and may be used for this purpose (see also Section 4).

1.3 These specifications apply specifically to silicon wafers with one chem-mechanically polished surface. Wafers polished on both sides, or unpolished, or with epitaxial deposits are not covered. Values given for thickness, TTV, bow, and warp apply only to wafers without back surface films or extrinsic gettering treatments. However, purchasers of such wafers may find these specifications to be a useful guide in defining their requirements.

1.4 For referee purposes, U.S. customary units shall be used for wafers of 2 and 3-inch nominal diameters, and SI (system international, commonly called metric) units for 80 mm and larger diameter wafers.

1.5 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory practices prior to use.

2 Referenced Standards

2.1 *SEMI Standards*

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M20 — Specification for Establishing a Wafer Coordinate System

SEMI T1 — Specification for Back Surface Bar Code Marking of Silicon Wafers

SEMI T2 — Specification for Marking of Wafers with a Two-Dimensional Matrix Code Symbol

NOTE 1: A revision to SEMI T2 to extend it to include rectangular code symbols is currently being balloted in a companion document.

2.2 *ASTM Standards*[1]

E 122 — Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process

F 21 — Test Method for Hydrophobic Surface Films by the Atomizer Test

F 22 — Test Method for Hydrophobic Surface Films by the Water-Break Test

F 26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

F 28 — Method for Measuring the Minority-Carrier Lifetime in Bulk Germanium and Silicon

F 42 — Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

F 43 — Test Methods for Resistivity of Semiconductor Materials

F 47 — Test Method for Crystallographic Perfection of Silicon by Preferential Etch Techniques

F 76 — Test Methods for Measuring Hall Mobility and Hall Coefficient in Extrinsic Semiconductor Single Crystals

F 81 — Method for Measuring Radial Resistivity Variation on Silicon Slices

F 84 — Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555. Website: www.astm.org

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F 154 — Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

F 391 — Test Method for Minority Carrier Diffusion Length in Silicon by Measurement of Steady-State Surface Photovoltage

F 398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wave Number or Wavelength of the Plasma Resonance Minimum

F 416 — Test Method for Detection of Oxidation Induced Defects in Polished Silicon Wafers

F 419 — Test Method for Net Carrier Density in Silicon Epitaxial Layers by Voltage-Capacitance of Gated and Ungated Diodes

F 523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

F 533 — Test Method for Thickness and Thickness Variation of Silicon Slices

F 534 — Test Method for Bow of Silicon Slices

F 613 — Test Method for Measuring Diameter of Silicon Slices and Wafers

F 657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Slices and Wafers by a Noncontact Scanning Method

F 671 — Test Method for Measuring Flat Length on Slices of Electronic Materials

F 673 — Test Method for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

F 847 — Test Methods for Crystallographic Orientation of Flats on Single Crystal Silicon Slices and Wafers by X-Ray Techniques

F 928 — Test Methods for Edge Contour of Silicon Wafers

F 951 — Test Method for Radial Interstitial Oxygen Variation

F 1188 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

F 1241 — Terminology of Silicon Technology

F 1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectroscopy

F 1388 — Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of MOS (Metal-Oxide-Silicon) Capacitors

F 1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

F 1391 — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

F 1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

F 1526 — Standard Test Method for Measuring Surface Metal Contamination on Silicon Wafers by Total Reflection X-Ray Fluorescence Spectroscopy

F 1528 — Standard Test Method for Measuring Boron Contamination in Heavily Doped N-Type Silicon Substrates by Secondary Ion Mass Spectrometry

F 1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

F 1535 — Test Method for Carrier Recombination Lifetime is Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

F 1617 — Standard Test Method for Measuring Surface Sodium, Aluminum, and Potassium on Silicon and Epi Substrates by Secondary Ion Mass Spectrometry

F 1619 — Standard Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with P-Polarized Radiation Incident at the Brewster Angle

2.3 *DIN Standards*[2]

50430 — Messung des spezifischen elektrischen Widerstandes von stabformigen Einkristallen aus Silicium oder Germanium mit dem Zwei-Sonden-Gleichstrom-Verfahren (Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals in Bars by Means of the Two Point-Probe Direct Current Method)

50431 — Messung des spezifischen elektrischen Widerstandes von Einkristallen aus Silicium oder Germanium mit dem Vier-Sonden Gleichstrom-Verfahren bei linearer Anordnung der Sonden (Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Collinear Four Probe Array)

50432 — Bestimmung des Leitungstyps von Silicium oder Germanium mittels Richttest oder Thermosonde (Determination of the Conductivity Type of Silicon or

2 DIN Standards, Deutsches Institut fur Normung e.v., available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-1000 Berlin 30, Germany

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Germanium by Means of Rectification Test or Hot-Probe)

50433/1 — Bestimmung der Orientierung von Einkristallen mit einem Roentgengoniometer (Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction)

50433/2 — Bestimmung der Orientierung von Einkristallen nach der Lichtfiguren-methode (Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure)

50433/3 — Bestimmung der Orientierung von Einkristallen mittels Laue-Ruckstrahl-verfahren (Determination of the Orientation of Single Crystals by Means of Laue Back Scattering)

50434 — Nachweis von Kristalldefekten in Silizium-Einkristallen mittels Atztechnik an {111}- und {100}-Flachen (Detection of Crystal Defects in Silicon Monocrystals by Etching on {111} and {100} Surfaces)

50435 — Bestimmung der radialen Variation des spezifischen elektrischen Widerstandes an Silicium oder Germanium-Scheibenmitdem Vier-Sonden-Gleichstromverfahren (Determination of the Radial Resistivity Variation of Silicon or Germanium Slices by Means of a Four-Point-DC-Probe)

50438/1 — Bestimmung des Verunreinigungs-gehaltes in Silicium mittels Infrarot Absorption; Sauerstoff (Determination of Impurity Content in Silicon by Infrared Absorption; Oxygen)

50438/2 — Bestimmung des Verunreinigungs-gehaltes in Silicium mittels Infrarot Absorption; Kohlenstoff (Determination of Impurity Content in Silicon by Infrared Absorption; Carbon)

50440/1 — Messung der Rekombinations-Tragerlebensdauer in Silicium-Einkristallen nach der Photoleitfahigkeitsverfahren; Messung an quaderformigen Proben (Measurement of Recombination Carrier Lifetime in Silicon Single Crystals by Means of Photoconductive Decay Method; Measurement on Bar-Shaped Test Samples)

50441/1 — Messung der geometrischen Dimensionen von Halbleiterscheiben; Messung der Dicke (Measurement of the Geometric Dimensions of Semiconductor Slices; Measurement of Thickness)

50441/2 — Messung der geometrischen Dimensionen von Helblaiterscheiben; Prufung der Kantenverrundung (Measurement of the Geometric Dimensions of Semiconductor Slices; Testing of Edge Rounding)

50441/4 — Messung der geometrischen Dimensionen von Halbleiterscheiben: Scheibendurchmesser und Flattiefe (Measurement of the Geometrical Dimensions of Semiconductor Slices: Diameter and Flat Depth of Slices)

2.4 *JIS Standards*[3]

H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

H 0611 — Methods of Measurement of Thickness Taper and Bow for Silicon Wafers

2.5 *Other Standards*

ANSI/ASME B46.1 — Surface Texture (Surface Roughness, Waviness, and Lay)[4]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes[5]

ISO 4287/1 — Surface Roughness – Terminology – Part 1: Surface and its Parameters[6]

NOTE 2: As listed or revised, all documents cited shall be the latest publications of adopted standards.

3 Terminology

3.1 Many terms relating to silicon technology are defined in ASTM Terminology F 1241.

3.2 Definitions for many of the polished wafer defect terms in Table 1 are given in ASTM Practices F 154 and F 523 and in ASTM Test Method F 416.

3.3 Other terms are defined as follows:

3.3.1 *acceptor* — an impurity in a semiconductor which accepts electrons excited from the valence band, leading to hole conduction.

3.3.2 *anisotropic, in semiconductor technology* — exhibiting different physical properties in differing crystallographic directions.

3.3.3 *anisotropic etch* — a selective etch which exhibits an accelerated etch rate along specific crystallographic directions.

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3 Japanese Standards Association, 1-24, Akasaka 4 Chome, Minato-ku, Tokyo 107, Japan

4 This standard is currently being revised by a committee of The American Society of Mechanical Engineers, United Engineering Center, 345 E. 47th St., New York, NY 10017. In this draft revision, terminology is collected in a document designated B46.1.1; this document should be referred to in connection with additional terms related to surface roughness. Note that the nomenclature and symbols in ASME B46.1.1 may differ from those employed herein. Also note that ASME B46.1.1 is still under development, and the terms and definitions therein may change prior to approval by ASME and ANSI.

5 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

6 ISO Central Secretariat, C.P. 56, CH-1211 Geneve 20 Switzerland; available in the U.S. from American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036

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3.3.3.1 Discussion: Anisotropic etches are used to determine crystal orientation, to fabricate micromechanical structures, and to facilitate dielectric component isolation.

3.3.4 *azimuth, in ellipsometry* — the angle between the major axis of the ellipse and the plane of incidence.

3.3.5 *backside* — not preferred, use *back surface* as defined in ASTM Terminology F 1241.

3.3.6 *bipolar* — semiconductor device fabrication technology which produces transistors that use both holes and electrons as charge carriers.

3.3.7 *carrier, in semiconductor materials* — an entity capable of carrying electric charge through a solid, for example, valence holes and conduction electrons in semiconductors; charge carrier.

3.3.8 *chem-mechanical polish, in semiconductor technology* — a process for the removal of surface material from the wafer which uses chemical and mechanical actions to achieve a mirror-like surface for subsequent processing.

3.3.9 *chuck mark* — any physical mark on either surface of a wafer caused by a robotic end effector, chuck, or wand.

3.3.10 *cleavage plane* — a crystallographically preferred fracture plane.

3.3.11 *conductivity (electrical)* — a measure of the ease with which charge carriers flow in a material; the reciprocal of resistivity.

3.3.11.1 Discussion: In a semiconductor, the conductivity is proportional to the product of free carrier density, electron electrical, and carrier mobility. Most variant of all crystal properties, conductivity can range over 13 orders of magnitude. Conductivity can be locally modified by temperature, carrier injection, irradiation, or magnetic field. Symbol is σ and units are $(\Omega \bullet cm)^{-1}$.

3.3.12 *conductivity type, of a semiconductor crystal or wafer* — a property that identifies the majority charge carrier in the semiconductor; see also *n-type*, *p-type*.

3.3.13 *contaminant, particulate* — see *light point defect*.

3.3.14 *contamination, area* — matter, unintentionally added to the surface of a wafer, of extent greater than a single localized light scatterer.

3.3.14.1 Discussion: Area contamination may be foreign matter on the wafer surface resulting from chuck marks, finger or glove prints, stains, wax or solvent residues, etc.

3.3.15 *contamination, particulate* — a particle or particles on the surface of a wafer.

3.3.16 *crystal defect* — departure from the ideal arrangement of atoms in a crystal.

3.3.17 *crystal indices* — see *Miller indices*.

3.3.18 *crystallographic notation* — a symbolism based on Miller indices used to label planes and directions in a crystal as follows:

plane	(111)
family of planes	{111}
direction	[111]
family of directions	<111>

3.3.19 *depletion layer* — a region in which the mobile carrier charge density is not sufficient to neutralize the net fixed charge density of donors and acceptors; barrier layer; blocking layer; space-charge layer.

3.3.20 *dimple* — a shallow depression with gently sloping sides that exhibits a concave, spheroidal shape and is visible to the unaided eye under proper lighting conditions.

3.3.21 *donor* — an impurity or imperfection in a semiconductor which donates electrons to the conduction band, leading to electron conduction.

3.3.22 *dopant* — a chemical element, usually from the third or fifth columns of the periodic table, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

3.3.23 *doping* — addition of specific impurities to a semiconductor to control the electrical resistivity.

3.3.24 *edge exclusion area* – the area between the FQA and the actual periphery of the wafer. The area varies with the actual dimensions of the wafer.

3.3.25 *edge exclusion, nominal* (EE) – the distance from the FQA boundary to periphery of a wafer of nominal dimensions.

3.3.26 *edge profile* — on edge contoured wafers (whose edges have been shaped chemically or mechanically), a description of the contour of the boundary of the wafer that joins the front and back surfaces.

3.3.27 *etch* — a solution, a mixture of solutions, or a mixture of gases that attacks the surfaces of a film or substrate, removing material either selectively or nonselectively; see also *anisotropic etch*, *preferential etch*.

3.3.28 *fixed quality area (FQA)* — the central area of a wafer surface, defined by a nominal edge exclusion,

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EE, over which the specified values of a parameter apply.

3.3.28.1 Discussion: The boundary of the FQA is at all points the distance *EE* away from the periphery of a wafer of nominal dimensions. (See Figure 1.) The size of the FQA is independent of wafer diameter and flat length tolerances. For the purposes of defining the FQA, the periphery of a wafer of nominal dimensions at locations with notch fiducials is assumed to follow the circumference of a circle with diameter equal to the nominal wafer diameter. It may be necessary to specify exclusion areas where the values of a specified parameter do not apply for regions like: the notch, laser marks, or where handling/gripping devices contact the wafer.

3.3.29 *flat, on a semiconductor wafer* — a portion of the periphery of a circular wafer that has been removed to a chord; see also *primary orientation flat*, *secondary flat*.

3.3.30 *flat diameter* — the linear dimension across the surface of a semiconductor wafer from the center of the flat through the wafer center to the circumference of the wafer on the opposite edge along the diameter perpendicular to the flat. (See Figure 3.)

3.3.30.1 Discussion: The flat diameter may be associated with the primary orientation flat, with a secondary flat, if present, or with any other flat, if present. In such cases, the term may be modified as primary orientation flat diameter, *secondary flat diameter*, etc. In the case of opposing primary orientation and secondary flats, as occurs on [100] *n*-type wafers 125 mm and smaller in diameter, the concept of flat diameter does not apply because the diameter perpendicular to the flats does not intersect the wafer circumference.

3.3.31 *flatness* — for wafer surfaces, the deviation of the front surface, expressed in TIR or maximum FPD relative to a specified reference plane when the back surface of the wafer is ideally flat, as when pulled down by a vacuum onto an ideally clean flat chuck.

3.3.31.1 Discussion: The flatness of a wafer may be described as either:

1. The global flatness, or
2. The maximum value of site flatness as measured on all sites, or
3. The percentage of sites which have a site flatness equal to or less than a specified value.

3.3.32 *focal plane* — the plane perpendicular to the optical axis of an imaging system which contains the focal point of the imaging system.

3.3.32.1 Discussion: The reference plane used by an imaging system is coincident with or parallel with the focal plane. Full field imaging systems employ coincident global focal and reference planes. Partial field imaging systems employ either coincident site focal and reference planes or displaced site focal and global reference planes. If the reference plane is not coincident with the focal plane, it is displaced from the focal plane so that the point on the front surface at a site center lies in the focal plane.

3.3.33 *focal plane deviation (FPD)* — the distance parallel to the optical axis from a point on the wafer surface to the focal plane.

3.3.34 *four-point probe* — an electrical probe arrangement for determining the resistivity of a material in which separate pairs of contacts are used (1) for passing current through the specimen and (2) measuring the potential drop caused by the current.

3.3.35 *front side* — not preferred; use *front surface* as defined in ASTM Terminology F 1241.

3.3.36 *global flatness* — the TIR or the maximum FPD relative to a specified reference plane within the FQA.

3.3.37 *goniometer* — an instrument to measure angles.

3.3.37.1 Discussion: Goniometers are frequently used with x-ray diffraction equipment to measure crystal axis angles or for optical angle measurement.

3.3.38 *gradient, resistivity* — not preferred; see *resistivity variation*.

3.3.39 *groove, in a semiconductor wafer* — a shallow scratch with rounded edges that is usually the remnant of a scratch not completely removed by polishing.

3.3.40 *haze* — non-localized light-scattering resulting from surface topography (microroughness) or from dense concentrations of surface or near-surface imperfections; see also *laser light-scattering event*.

3.3.40.1 Discussion: Haze due to the existence of a collection of imperfections is a mass effect; individual imperfections of the type which result in haze cannot be readily distinguished by the eye or other optical detection system without magnification. In a particle counter, haze results in a background signal; this signal and laser light-scattering events together comprise the signal due to light-scattering from a wafer surface.

3.3.41 *hole* — a mobile vacancy in the electronic valence structure of a semiconductor which acts like a positive electron charge with positive mass; the majority carrier in *p*-type material.

3.3.42 *ingot, in silicon technology* — a cylinder or rectangular solid of polycrystalline or single crystal silicon, generally of slightly irregular dimensions.

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3.3.42.1 Discussion: Silicon wafers are usually sliced from cylindrical single-crystal ingots that have been ground to a uniform diameter prior to slicing.

3.3.43 *laser light-scattering event* — a signal pulse that exceeds a preset threshold, generated by the interaction of a laser beam with a discrete scatterer at a wafer surface as sensed by a detector; see also *haze*.

3.3.43.1 Discussion: The amplitude of the signal, as measured by any combination of incidence orientation and collection orientation, does not convey topographic information (i.e., pit or particle). It does not allow the observer to deduce the size or origin of the scatterer without other detailed knowledge, such as its index of refraction and shape. In a particle counter, the background signal due to haze and laser light-scattering events together comprise the signal due to light-scattering from a wafer surface.

3.3.44 *lay* — the predominant direction of the surface texture.

3.3.44.1 Discussion: Although the texture of polished silicon wafers is generally isotropic, some epitaxial wafers exhibit a pattern of steps and ledges when examined by atomic force microscopy at near atomic resolution. Contoured wafer edges may also exhibit lay even after polishing.

3.3.45 *light point defect (LPD)* — not preferred, see *localized light-scatterer (LLS)*.

3.3.45.1 Discussion: To some, the term light point defect implies a defective part; hence, a search was undertaken for a more neutral term. Several were tried, and finally, despite some objection to the difficulty of saying the code, the term localized light scatterer was approved as a replacement. This term is general in nature and can refer to features detected both visual inspection and by automated inspection using a scanning laser system.

3.3.46 *localized light-scatterer (LLS)* — an isolated feature, such as a particle or a pit, on or in a wafer surface, resulting in increased light-scattering intensity relative to that of the surrounding wafer surface; sometimes called light point defect.

3.3.46.1 Discussion: Localized light scatterers of sufficient size appear as points of light under high intensity optical illumination; these points of light can be observed visually, but the observation is a qualitative one. Localized light scatterers are observed by automated inspection techniques as laser-light scattering events. Automated inspection techniques are quantitative in the sense that scatterers with different scattering intensities can be segregated. However, the amplitude of the scattered light intensity (laser light-scattering event), as measured by any combination of incident beam direction and collection optics, does not by itself convey topographical information; particles and pits cannot be distinguished solely on the basis of amplitude data. Also, the observer cannot deduce the size or shape of the LLS from the signal amplitude alone. The presence of LLS's does not necessarily decrease the utility of the wafer.

3.3.47 *lot* — for the purposes of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

3.3.48 *majority carrier* — type of charge carrier constituting more than one half the total charge-carrier concentration (e.g., holes in *p*-type material).

3.3.49 *maximum FPD* — the largest of the absolute values of the focal plane deviations.

3.3.50 *microroughness* — surface roughness components with spacing between irregularities (spatial wavelength) less than about 100 µm.

3.3.51 *Miller indices, of a crystallographic plane* — the smallest integers proportional to the reciprocals of the intercepts of the plane on the three crystal axes of unit length.

3.3.52 *minority carrier* — type of charge carrier constituting less than one half the total charge-carrier concentration (e.g., electrons in *p*-type material).

3.3.53 *notch, on a semiconductor wafer* — an intentionally fabricated indent of specified shape and dimensions oriented such that the diameter passing through the center of the notch is parallel with a specified low index crystal direction.

3.3.54 *orthogonal misorientation* — in wafers cut intentionally "off orientation," the angle between the projection of the vector normal to the wafer surface onto a {111} plane and the projection on that plane of the nearest <100> direction. (See Figure 2.)

3.3.55 *particle* — a small, discrete piece of foreign material or silicon not connected crystallographically to the wafer.

3.3.55.1 Discussion: Particles may be pieces of solid material or condensate from liquids or gases. Particles are observed by automated inspection as laser light-scattering events, but they may also be observed visually under high intensity illumination as points of light or studied by other methods, including scanning electron microscopy. Particles on wafer surfaces can usually be removed by non-etching cleaning.

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3.3.56 *point defect* — a localized crystal defect such as a lattice vacancy, interstitial atom, or substitutional impurity. Contrast with *light point defect*.

3.3.57 *preferential etch* — a selective etch that etches regions of different crystal strain or conductivity at different rates, used to delineate crystal defects or regions of differing conductivity on wafer surfaces.

3.3.58 *primary orientation flat* — the flat of longest length on the wafer, oriented such that the chord is parallel with a specified low index crystal plane; *major flat*.

3.3.59 *profilometer* — an instrument for measuring the topographical profile of a surface.

3.3.60 *rms microroughness* (R_q) — the root mean square of the surface profile height deviations Z(x) from the mean line taken within the evaluation Length L.

3.3.60.1 Discussion: *rms microroughness*, R_q is one of several statistical metrics which can be used to describe a surface profile; definitions for other metrics and for such concepts as mean line, evaluation length, and power spectral density function, may be found in ANSI/ASME B46.1 and ISO 4287/1.

3.3.60.2 The function R_q is related to a one-dimensional measurement of the surface profile as follows:

$$R_q = \left[\frac{1}{L} \int_0^L Z(x)^2 dx \right]^{1/2}$$

3.3.60.3 The digital approximation of R_q for a profile consisting of N equally spaced points is:

$$R_q = \left[\frac{1}{N} \sum_{i=1}^{N} Z_i^2 \right]^{1/2}$$

3.3.60.4 Experimentally, the profile is always limited by the spatial bandwidth of the measurement. For a profile of length L, consisting of N equally spaced points, the lower spatial frequency limit f_1 can never be less than $1/L$ and the upper spatial frequency limit f_2 can never be greater than the Nyquist limit, $N/2L$. In practical cases, $f_1 \approx 2/L$; the achievable value of f_2 depends on instrumental parameters.

3.3.60.5 R_q can also be estimated by integrating the one-dimensional power spectral density (PSD) function, *PSD(f)*, over the spatial frequency range between two spatial frequencies, f_1 and f_2, which lie within the bandwidth of the measurement:

$$R_q = \left[\int_{f_1}^{f_2} PSD(f) \mathrm{d}f \right]^{1/2}$$

3.3.60.6 In all cases, R_q must be reported together with the lower and upper limits, f_1 and f_2, respectively, of the spatial frequency bandwidth over which it has been determined. Alternatively, the spatial bandwidth may be expressed in terms of the upper and lower spatial wavelengths, $\lambda 2$ (=$1/f_2$) and $\lambda 1$ (=$1/f_1$), respectively.

3.3.61 *rms area microroughness*, (R_{qA}) — the root mean square of the topographic deviations of a surface Z(x,y) from the mean surface taken within the evaluation area A_e (=L_xL_y).

3.3.61.1 Discussion: The rms area microroughness is one of several statistical metrics which can be used to describe surface topography; definitions for other metrics and for such concepts as mean surface and evaluation area may be found in ANSI/ASME B46.1 and ISO 4287/1.

3.3.61.2 The function R_{qA} is related to a two-dimensional measurement of the surface profile as follows:

$$R_{qA} = \left[\frac{1}{A_e} \int_0^{L_x} \int_0^{L_y} Z(x,y)^2 \ \mathrm{d}x\mathrm{d}y \right]^{1/2}$$

3.3.61.3 The digital approximation of R_{qA} for a surface profile consisting of N by M data points equally spaced along the x and y directions, respectively, is:

$$R_{qA} = \left[\frac{1}{NM} \sum_{i=l}^{M} \sum_{j=l}^{N} Z_{ij}^2 \right]^{1/2}$$

3.3.61.4 Experimentally, the profile is always limited by the spatial bandwidth of the measurement. In the x direction, the profile length is Lx divided into N equally spaced points; the lower spatial frequency limit for fx can never be less than $1/L_x$ and the upper spatial frequency limit can never be greater than the Nyquist limit, $N/2L_x$. Similarly, in the y direction, the profile length is L_y divided into M equally spaced points; the lower frequency limit for f_y can never be less than $1/L_y$ and the upper spatial frequency limit can never be greater than the Nyquist limit, $M/2L_y$. Practical limits to the spatial bandwidth are governed by considerations similar to those for the one-dimensional case (see Discussion under *rms microroughness*).

3.3.61.5 R_{qA} can also be estimated by integrating the two-dimensional power spectral density (PSD) function, $PSD(f_x, f_y)$, over the spatial frequency range between spatial frequencies which lie within the bandwidth of the measurement:

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$$R_{qA} = \left[\int_{f_{x1}}^{f_{x2}} \int_{f_{y1}}^{f_{y2}} PSD_A(f_x, f_y)\, \mathrm{d}f_x \mathrm{d}f_y \right]^{1/2}$$

3.3.61.6 If the surface is assumed to be isotropic and the instrument response function is neglected, the rms microroughness over the spatial frequency range between f_1 and f_2 can also be obtained by integrating the isotropic PSD function:

$$R_{qA} = \left[\int_{f_1}^{f_2} PSD_{iso}(f)\, \mathrm{d}f \right]^{1/2}$$

where $PSD_{iso}(f) = \int_0^{2\pi} PSD_A(f_x, f_y) f\, \mathrm{d}\beta = 2\pi f\, PSD_A(f_x, f_y)$ and $f = (f_x^2 + f_y^2)^{1/2}$.

3.3.62 *radial gradient* — not preferred; see *resistivity variation*.

3.3.63 *reference plane* — a plane defined by one of the following:

1. Three points at specified locations on the front surface of the wafer, or
2. The least squares fit to the front surface of the wafer using all points within the FQA, or
3. The least squares fit to the front surface of the wafer using all points within a site, or
4. An ideal back surface (equivalent to the ideally flat chuck surface that contacts the wafer).

3.3.63.1 Discussion: The specified reference plane should be chosen with due regard for the capabilities of the imaging system. Front surface or back surface reference planes should be selected depending on the wafer mounting system. If the wafer cannot be gimbaled in the imaging system, a back surface reference plane should be specified.

3.3.64 *resistivity, (electrical)* — the measure of difficulty with which charged carriers flow through a material; the reciprocal of *conductivity*.

3.3.64.1 Discussion: the resistivity of a semiconductor or other material is the ratio of the potential gradient (electric field) parallel with the current to the current density. Symbol is σ and units are $(\Omega \bullet \mathrm{cm})^{-1}$.

3.3.65 *roughness* — the more narrowly spaced components of surface texture.

3.3.65.1 Discussion: These components are considered within defined limits of spatial wavelength (or frequency).

3.3.66 *scan direction* — the direction of successive subsites in a scanner site flatness calculation.

3.3.66.1 Discussion: The scanner site flatness value obtained for a site may depend on scan direction.

3.3.67 *scanner site flatness* — the maximum subsite TIR or the maximum subsite FPD, of a site. The subsite TIR is the TIR of the portion of the subsite that falls within the FQA and within the site; the subsite FPD is the maximum FPD of the portion of the subsite that falls within the FQA and within the site. The reference plane is calculated using all points within the subsite that fall within the FQA.

3.3.67.1 Discussion: Precise scanner site flatness measurement requires measurement points located closely enough to reveal the surface topography in detail. It is recommended that the scanner site flatness be measured using a data point array with adjacent points separated by 1 mm or less.

3.3.68 *secondary flat* — a flat of length shorter than the primary orientation flat, whose position with respect to the primary orientation flat identifies the type and orientation of the wafer.

3.3.69 *shape* — for wafer surfaces, the deviation of a specified wafer surface relative to a specified reference plane when the wafer is in an unclamped condition, expressed as the range or total indicator reading (TIR) or as the maximum reference plane deviation (maximum RPD) within the specified fixed quality area.

3.3.69.1 Discussion: This definition is analogous to the definition of flatness, which applies to the front surface geometry when the wafer is in the clamped condition.

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3.3.70 *site* — a rectangular area, on the front surface of the wafer, whose sides are parallel and perpendicular to the primary orientation flat or to the notch bisector, and whose center falls within the FQA.

3.3.71 *site array* — a set of contiguous sites.

3.3.72 *site flatness* — the TIR or the maximum FPD of the portion of a site which falls within the FQA.

3.3.72.1 Discussion: Precise site flatness measurement requires measurement points located closely enough to reveal the surface topology in detail. It is recommended that site flatness be measured using a data point array with adjacent points separated by 2 mm or less. It is also recommended that the data set used to calculate site flatness have data at each site corner and along each site boundary. This makes the effective site measurement area equal to the site size.

3.3.73 *smudge* — dense local area of contamination usually caused by handling or fingerprints.

3.3.74 *sori* — the difference between the maximum positive and maximum negative deviations of the front surface of a wafer that is not chucked from a reference plane that is a least-squares fit to the front surface.

3.3.75 *subsite, of a site* — a rectangular area, Lss × Wss, on the front surface of a wafer, associated with a particular site. The center of the subsite must be within the site. Some part of the subsite must be within or on the FQA boundary. A subsite corresponds to the instantaneous area exposed by a scanning stepper (see Figures 8 and 9).

3.3.76 *surface texture* — the topographic deviations of a real surface from a reference surface.

3.3.76.1 Discussion: Surface texture includes roughness, waviness, and lay.

3.3.77 *total indicator reading (TIR)* — the smallest perpendicular distance between two planes, both parallel with the reference plane, which encloses all points on the front surface of a wafer within the FQA, the site, or the subsite, depending on which is specified.

3.3.78 *waves* — uneven contours in the surface of a wafer visible to the unaided eye under large-area diffuse illumination.

3.3.79 *waviness* — the more widely spaced component of surface texture.

3.3.79.1 Discussion: Waviness may be caused by such factors as machine or work piece deflections, vibration, and chatter. Roughness may be considered as superimposed on a wavy surface.

4 Wafer Ordering Information

4.1 Purchase orders for silicon wafers furnished to this specification shall include the following items:

4.1.1 Nominal diameter (see applicable polished silicon wafer standard).

4.1.2 Crystal growth method (see NOTE 4).

4.1.3 Surface orientation (see applicable polished silicon wafer standard).

4.1.4 Conductivity type (see applicable polished silicon wafer standard) and dopant (see NOTE 4).

4.1.5 Resistivity or resistivity range.

4.1.6 Lot acceptance procedures (see Section 8).

4.1.7 Certification (if required) (see Section 11).

4.1.8 Packing and marking (see Section 12).

4.1.9 Selection of test method to be used in evaluating those items for which alternate tests exist (see Section 9).

4.2 *Optional Criteria* — The following items may be specified optionally in addition to those listed above.

4.2.1 Doping method and thermal treatment (see NOTE 4).

4.2.2 Radial resistivity variation.

4.2.3 Crystal perfection.

4.2.4 Impurities other than common intentionally added dopant elements, such as interstitial atomic oxygen and substitutional carbon or in heavily doped n-type silicon, boron contamination.

4.2.5 Surface metal contaminants.

4.2.6 *Flatness* — The following conditions must be specified in connection with flatness measurement:

A. Type of Measurement
   1. Global flatness
   2. Maximum site flatness
   3. Percentage of sites within specification

B. Parameter: TIR or maximum FPD

C. Nominal Edge Exclusion: X

D. For site flatness (where specified):
   1. Site dimensions: x_{site} and y_{site} are relative to the SEMI M20 wafer coordinate system. The first site dimension listed in a site flatness specification shall be the x_{site} and the second dimension shall be the y_{site}.

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