SEMI M1-1106
SPECIFICATIONS FOR POLISHED MONOCRYSTALLINE SILICON WAFERS

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1 Purpose

1.1 Monocrystalline (single crystal) silicon wafers are utilized for essentially all integrated circuits and many other semiconductor devices. To permit common processing equipment to be used in multiple device fabrication lines, it is essential for the wafer dimensions to be standardized.

1.2 In addition, as technology advances to smaller and smaller dimensions for the elements of high density integrated circuits, it has become of interest to standardize additional properties of the wafers.

1.3 This specification provides the essential dimensional and certain other common characteristics of silicon wafers, including polished wafers as well as substrates for epitaxial and certain other kinds of silicon wafers.

2 Scope

2.1 These specifications cover ordering information and certain requirements for high-purity, monocrystalline polished silicon wafers used in semiconductor device and integrated circuit manufacturing or as substrates (or starting wafers) for other kinds of wafers, including epitaxial, annealed, and SOI wafers.

2.2 Dimensional requirements are provided for the following categories of polished wafers:

- Category 1.1 — 2 in. polished monocrystalline silicon wafers with secondary flat
- Category 1.2 — 3 in. polished monocrystalline silicon wafers with secondary flat
- Category 1.5 — 100 mm polished monocrystalline silicon wafers, 525 µm thick, with secondary flat
- Category 1.6 — 100 mm polished monocrystalline silicon wafers, 625 µm thick, with secondary flat
- Category 1.7 — 125 mm polished monocrystalline silicon wafers with secondary flat
- Category 1.8.1 — 150 mm polished monocrystalline silicon wafers with secondary flat and T/3 edge profile template
- Category 1.8.2 — 150 mm polished monocrystalline silicon wafers with secondary flat and T/4 edge profile template
- Category 1.9.1 — 200 mm notched polished monocrystalline silicon wafers with T/3 edge profile template
- Category 1.9.2 — 200 mm notched polished monocrystalline silicon wafers with T/4 edge profile template
- Category 1.10.1 — 200 mm flatted polished monocrystalline silicon wafers with T/3 edge profile template without secondary flat
- Category 1.10.2 — 200 mm flatted polished monocrystalline silicon wafers with T/4 edge profile template without secondary flat
- Category 1.11 — 100 mm flatted polished monocrystalline silicon wafers without secondary flat
- Category 1.12 — 125 mm flatted polished monocrystalline silicon wafers without secondary flat
- Category 1.13.1 — 150 mm flatted polished monocrystalline silicon wafers with T/3 edge profile template without secondary flat
- Category 1.13.2 — 150 mm flatted polished monocrystalline silicon wafers with T/4 edge profile template without secondary flat
- Category 1.15 — 300 mm notched polished monocrystalline silicon wafers

2.2.1 Values given for thickness, TTV, bow, and warp apply only to wafers prior to application of back surface films, extrinsic gettering treatments, or other thermal treatments.

2.2.2 The dimensional characteristics of Category 1.10.1, 1.10.2, 1.11, 1.12, 1.13.1, and 1.13.2 wafers specified in this document are identical with those specified in JEITA EM-3602, and the dimensional characteristics of Category 1.15 wafers are essentially equivalent with those specified in JEITA EM-3602.

2.3 A complete purchase specification requires that additional physical properties be specified along with test methods suitable for determining their magnitude. This standard provides a comprehensive listing of such properties and associated test methods. This listing provides a systematic basis for constructing the purchase specification for any kind of polished silicon wafer or substrate and is expected to be used for such purposes.

2.4 These specifications apply specifically to prime silicon wafers with at least one chem-mechanically polished surface. Ground, lapped, and unpolished wafers are not covered in this specification but this specification may provide guidance in connection with their procurement.

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2.5 In addition, these specifications cover specification requirements for basic 300 mm diameter, double-side polished silicon wafers that are suitable for many advanced integrated circuit applications. If this kind of wafer is desired, physical properties other than those listed in the table of requirements shall not be included in the purchase specification.

2.6 These specifications do not cover the requirements for the following related silicon materials and wafers:

- Polycrystalline silicon (see SEMI M16 or JEITA EM-3601),
- Epitaxial wafers (see SEMI M62),
- Epitaxial wafers with buried layer (see SEMI M61),
- Test wafers (see SEMI M8),
- Premium wafers (see SEMI M24),
- Reclaimed wafers (see SEMI M38),
- Annealed wafers (see SEMI M57),
- SOI wafers (see SEMI M34, SEMI M41, SEMI M47, or JEITA EM-3603),
- Dielectrically isolated wafers (see SEMI M22), and
- Solar-grade silicon wafers (see SEMI M6).

They do, however, provide the ordering information for test, premium, and reclaimed wafers, as well as the ordering information for the polished substrates and starting wafers used to prepare epitaxial, annealed, and SOI wafers.

2.7 The complete EDI Code List for items in the Order Form appropriate to silicon wafers, including polished wafers and substrates, can be found in SEMI M18.

2.8 For referee purposes, U.S. customary units shall be used for wafers of 2 in. and 3 in. nominal diameters, and SI (system international, commonly called metric) units for 100 mm and larger diameter wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards*

SEMI M6 — Specification for Silicon Wafers for Use as Photovoltaic Solar Cells

SEMI M8 — Specification for Polished Monocrystalline Silicon Test Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M16 — Specification for Polycrystalline Silicon

SEMI M18 — Guide for Developing Specification Forms for Order Entry of Silicon Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M26 — Guide for the Re-use of 100, 125, 150, and 200 mm Wafer Shipping Boxes Used to Transport Wafers

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M34 — Guide for Specifying SIMOX Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M38 — Specification for Polished Reclaimed Silicon Wafers

SEMI M40 — Guide for Measurement of Surface Roughness of Planar Surfaces on Silicon Wafer

SEMI M41 — Specification of Silicon-on-Insulator (SOI) for Power Device/ICs

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI M44 — Guide to Conversion Factors for Interstitial Oxygen in Silicon

SEMI M45 — Provisional Specification for 300 mm Wafer Shipping System

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SEMI M47 — Specification for Silicon-on-Insulator (SOI) Wafers for CMOS LSI Applications

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

SEMI M57 — Guide for Specifying Silicon Annealed Wafers

SEMI M58 — Test Method for Evaluating DMA-Based Particle Deposition Systems and Processes

SEMI M59 — Terminology for Silicon Technology

SEMI M61 — Specification for Silicon Epitaxial Wafers with Buried Layers

SEMI M62 — Specifications for Silicon Epitaxial Wafers

SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF28 — Test Methods for Minority-Carrier Lifetime in Bulk Germanium and Silicon by Measurement of Photoconductive Decay

SEMI MF42 — Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF84 — Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF391 — Test Methods for Minority Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF525 — Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF533 — Test Method for Thickness and Thickness of Variation of Silicon Wafers

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF657 —Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

SEMI MF847 — Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF951 — Test Method for Determination of Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF978 — Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

SEMI MF1048 — Test Method for Measuring Reflective Total Integrated Scatter

SEMI MF1049 — Practice for Shallow Etch Pit Detection on Silicon Wafers

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1188 — Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

SEMI MF1239 — Test Method for Oxygen Precipitation Characteristics of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1388 — Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of Metal-Oxide-Silicon (MOS) Capacitors

SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1391 — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1528 — Test Method for Measuring Boron Contamination in Heavily Doped *n*-Type Silicon Substrates by Secondary Ion Mass Spectrometry

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SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1535 — Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and Epi Substrates by Secondary Ion Mass Spectrometry

SEMI MF1619 — Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with *p*-Polarized Radiation Incident at the Brewster Angle

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon

SEMI MF1982 — Test Methods for Analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desporption Gas Chromatography

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T1 — Specification for Back Surface Bar Code Marking of Silicon Wafers

SEMI T2 — Specification for Marking of Wafers with a Two-Dimensional Matrix Code Symbol

SEMI T3 — Specification for Wafer Box Labels

SEMI T6 — Procedure and Format for Reporting of Test Results by Electronic Data Interchange (EDI)

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ASTM Standards*[1]

D 523 — Standard Test Method for Specular Gloss

E 122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

3.3 *JEITA (formerly JEIDA) Standards*[2]

EM-3401 (43) — Terminology Of Silicon Wafer Flatness

EM-3501 (18) — Standard Methods for Determining the Orientation of a Semiconductive Silicon Single Crystal

EM-3502 (53) — Test method for recombination lifetime in silicon wafers by measurement of photoconductivity decay by microwave reflectance

EM-3503 (56) — Standard test method for substitutional atomic carbon content of silicon by infrared absorption

EM-3504 (61) — Standard test method for interstitial atomic oxygen content of silicon by infrared absorption

EM-3601 — Standard Specification for High Purity Polycrystalline Silicon

EM-3602 (27) — Standard specification for dimensional properties of silicon wafers with specular surfaces

EM-3603 — Standard of SOI wafers and metrology

3.4 *JIS Standards*[3]

H 0604 — Measuring of minority-carrier life time in silicon single crystal by photoconductive decay method

H 0607 — Determination of Conductivity Type in Germanium by Thermoelectromotive Method

H 0609 — Test methods of crystalline defects in silicon by preferential etch techniques

H 0611 — Methods of measurement of thickness, thickness variation and bow of silicon wafer

H 0614 — Visual inspection for silicon wafers with specular surfaces

1 ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555, Website: http://www.astm.org

2 Japan Electronics and Information Technology Industries Association, 3rd floor, Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan. Telephone: 81.3.3518.6434, Fax: 81.3.3295.8727, Website: http://www.jeita.or.jp

3 Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005, Fax: 81.3.3586.2014, Website: http://www.jsa.or.jp

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H 0615 — Test method for determination of impurity concentrations in silicon crystal by photoluminescence spectroscopy

Z 8741 — Specular glossiness — Methods of measurement

3.5 *DIN Standards*[4]

50431 — Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Collinear Four-Probe Array

50432 — Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hot-Probe

50433/1 — Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction

50433/2 — Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure

50433/3 — Determination of the Orientation of Single Crystals by Means of Laue Back Scattering

50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

50435 — Determination of the Radial Resistivity Variation of Silicon or Germanium Slices by Means of a Four-Point-DC-Probe

50438/1 — Determination of Impurity Content in Silicon by Infrared Absorption: Oxygen

50438/2 — Determination of Impurity Content in Silicon by Infrared Absorption: Carbon

50440/1 — Measurement of Recombination Carrier Lifetime in Silicon Single Crystals by Means of Photoconductive Decay Method; Measurement on Bar-Shaped Test Samples

50441/1 — Determination of the Geometric Dimensions of Semiconductor Slices: Measurement of Thickness

50441/2 — Determination of the Geometric Dimensions of Semiconductor Slices: Testing of Edge Rounding

50441/3 — Measurement of the Geometric Dimensions of Semiconductor Slices; Determination of Flatness Deviation of Polished Slices by Means of Multiple Beam Interference

50441/4 — Determination of the Geometrical Dimensions of Semiconductor Slices: Diameter and Flat Depth of Slices

50443/1 — Recognition of Defects and Inhomogenities in Semiconductor Single Crystals by X-Ray Topography: Silicon

50445 — Contactless Determination of the Electrical Resistivity of Semiconductor Wafers with the Eddy Current Method

3.6 *ANSI Standards*[5]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

ANSI/EIA 556-B — Outer Shipping Container Standard

3.7 *ISO Standard*[6]

ISO 14706 — Surface chemical analysis — Determination of surface elemental contamination on silicon wafers by total reflection X-ray fluorescence spectroscopy (TXRF)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Terms and acronyms associated with silicon wafers and silicon technology are listed and defined in SEMI M59.

4 Deutches Institut für Normung e.V., standards are available in both English and German editions from Beuth Verlag GmbH, Burggrafenstrasse 6, 10787 Berlin, Germany, Telephone: 49.30.2601-0, Fax: 49.30.2601.1263, Website: http://www.beuth.de

5 American National Standards Institute, New York Office: 25 West 43rd Street, New York, NY 10036, USA. Telephone: 212.642.4900, Fax: 212.398.0023, Website: http://www.ansi.org

6 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11, Fax: 41.22.733.34.30, Website: http://www.iso.ch.

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5 Ordering Information

5.1 Purchase orders for silicon wafers furnished to this specification shall include the following items. These items are indicated on the Silicon Wafer Specification Format for Order Entry, Parts 1 and 2, shown in Table 1 with a ♦ symbol in the left-most column.

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.8 Wafer Surface Orientation
- 2-2.1 Resistivity
- 2-6.1 Diameter
- 2-6.2 Fiducial Dimensions
- 2-6.3 Primary Flat/Notch Orientation
- 2-6.4 Secondary Flat Length
- 2-6.5 Secondary Flat Location
- 2-6.6 Edge profile
- 2-6.7 Thickness

5.2 In addition, the purchase order must indicate the test method to be used in evaluating each of those items for which alternate test procedures exist.

5.3 *The following items must also be included in the purchase order:*

5.3.1 Lot acceptance procedures,

5.3.2 Certification (if required),

5.3.3 Packing and shipping container labeling requirements, and

5.4 Finally, many other characteristics may be specified in purchase orders for silicon wafers.

5.4.1 These shall be selected from the other items listed in the Silicon Wafer Specification Format for Order Entry, Parts 1 and 2 (see Table 1).

5.4.1.1 The parameter values provided in the requirements tables in § 6 may be used to identify appropriate values in the specification without selecting a value for each line. However, even if these requirements table values are used, the desired test methodology must be selected in accordance with ¶ 5.2.

5.4.2 It is essential that all choices for the items selected to be specified be made in order not to have unspecified parameters that would lead to surprises between supplier and customer. This is particularly important in the specification of wafer site flatness, for which a variety of parameters must be selected as outlined in Appendix 1.

5.4.3 Of the various items listed, the following (listed in the order in which they appear in Table 1) are most often selected, especially for wafers to be used for advanced integrated circuit manufacture:

- 2-1.6 Nominal edge exclusion (to define the fixed quality area)
- 2-4 Structural characteristics
- 2-5.1 Wafer ID Marking
- 2-6.8 Total Thickness Variation (TTV or GBIR, see § R2-7.7)
- 2-6.10 Warp (and sometimes 2.6.9 Bow or 2-6.11 Sori)
- 2-6.13 Site Flatness (SFQR)
- 2-8.5 Localized Light Scatterers (LLS)

6 Requirements

6.1 *General Characteristics*

6.1.1 The crystal growth method shall be modified Czochralski (Cz), float zone (FZ), or magnetic Czochralski (MCz) as specified on the purchase order. In some cases, the supplier is given the option of selecting Cz or MCz.

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6.1.1.1 If the Cz or MCz method is used for crystal growth, it may be permissible to utilize refined (previously melted) polysilicon in the growth charge; when this is the case, the appropriate box should be checked.

6.1.2 The crystal orientation shall be as specified on the purchase order. Usually either (100) or (111) is specified, but (110) is sometimes specified for polished wafers to be used for making SOI wafers. Occasionally, another orientation, such as (311) or (511), is specified.

6.1.3 The conductivity type shall be either *n* or *p*.

6.1.4 The dopant shall be specified to match the conductivity type. In general, boron (B) is used for *p*-type material, while phosphorus (P) is most commonly used for *n*-type material. For some applications, antimony (Sb) or arsenic (As) are used to obtain *n*-type wafers. For high power applications, neutron transmutation doping is often used to obtain high resistivity *n*-type wafers.

6.1.5 The nominal edge exclusion, *EE*, specifies the diameter of the fixed quality area (FQA), which is given by the nominal diameter minus 2·*EE* (see Figure 1). This quantity provides a center-referenced property.

6.1.5.1 This quantity is usually specified as 2 mm or 3 mm, but some advanced wafer processing technologies are moving in the direction of 1 mm. However, it should be noted that not all processes and metrology can work as close to the wafer edge as implied by the nominal edge exclusion.

6.1.5.2 In addition, it is sometimes necessary to specify additional exclusion zones, such as those for wafer identification marks or wafer holding areas.

6.1.5.3 Although use of edge referenced properties is discouraged, some equipments and procedures are based on edge referenced dimensions. When this occurs, the quality area is not fixed and some part of the fixed quality area may fall outside the evaluated area, which is generally not a desirable situation.

6.1.6 A co-dopant may be required for polished wafers intended to be processed into annealed wafers. Some co-dopants may also be used in connection with control of oxygen precipitation characteristics even when the wafer is not annealed.

6.1.7 *Wafer Surface Orientation* — The wafer shall conform to the surface orientation as specified in the purchase order.

6.1.7.1 For on-orientation wafers, the angular tolerance from the plane perpendicular to the growth axis shall be specified.

6.1.7.2 For off-orientation wafers, both the misorientation angle from the growth axis and its angular tolerance shall be specified.

6.1.7.2.1 A misorientation angle between 0.2° and 1° (0.6° ± 0.4°) from a (100) plane is frequently used for some epitaxial substrates.

6.1.7.2.2 A misorientation angle of 2.50° or 4° ± 0.5° from a (111) plane is often used for other epitaxial substrates.

6.1.7.3 Orthogonal misorientation is the tilt angle of the normal to a (111) wafer surface toward nearest <110> direction in a plane parallel with the primary flat as indicated in Figure 2.

6.1.7.3.1 The contribution of 5° of orthogonal misorientation to the total off-orientation angle is less than 0.5°.

6.1.7.4 For ion implant applications, the following tolerance issues should be considered:

6.1.7.4.1 For general use where channeling is to be avoided, the current wafer orientation specification of ±1.0° deviation from the [100] axis (perpendicular to the (100) plane of the wafer) is adequate. This specification is suitable for minimum channeling applications, provided that the appropriate ion implant equipment angle settings are employed.

6.1.7.4.2 Uniform, maximum channeling along the [100] axis perpendicular to the (100) wafer surface is strongly dependent on strict adherence to a 0° tilt angle. To achieve maximum channeling, crystallography requires the orientation to be within ±0.1° of a <100> direction. Also, the customer must remove all overlying oxide, nitride, poly, etc., layers from the wafer prior to a channeling implant. The customer must maintain very rigid control of the ion implant equipment angle setting in order to achieve maximum channeling across the wafer.

6.1.7.5 The tolerance of ±0.1° is derived from experimental ion implant profile data and ion implant modeling activity for implants into (100) silicon wafers. The ranges for which data was obtained are given in Table 2.

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Table 1 Silicon Wafer Specification Format for Order Entry, Parts 1 and 2

Part 1 General Information

ITEM	*INFORMATION*	*Date:*
Customer Name		
Purchase Order Number		
Line Number		
Item Number		
General Specification Number		
Revision Level		
Part Number/Revision		

Part 2 Polished Wafer or Substrate

ITEM			*SPECIFICATION*	*MEASUREMENT METHOD*
2-1 GENERAL CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice **must** be indicated in order to minimally specify a silicon wafer.)*				
♦	2-1.1	Growth Method	[ ]Cz; [ ]FZ; [ ]MCz; [ ]Supplier option of Cz or MCz	
	2-1.2	Use of Refined Polysilicon	[ ]Permitted; [ ]Not permitted	
♦	2-1.3	Crystal Orientation	[ ](100); [ ](111); [ ](110); [ ]Other: (specify) ( )	[ ]SEMI MF26 (X-Ray); [ ] SEMI MF26 (Optical); [ ]JEITA EM-3501; [ ]DIN 50433/1; [ ]DIN 50433/2; [ ]DIN 50433/3; [ ]Other: (specify)_____
♦	2-1.4	Conductivity Type	[ ]*p;* [ ]*n*	[ ]SEMI MF42; [ ]JIS H 0607; [ ]DIN 50432; [ ]Other: (specify)_____
♦	2-1.5	Dopant	[ ]B; [ ]P; [ ]Sb; [ ]As; [ ]Neutron Transmutation Doped; [ ]Other: (specify) _____	
	2-1.6	Nominal Edge Exclusion[#1] (see Figure 1)	[ ]2 mm; [ ]3 mm; [ ]5 mm; [ ]Other: (specify)_____mm	
	2-1.7	Co-dopant in Crystal	[ ]None; [ ]Nitrogen; [ ]Carbon; [ ]Nitrogen and Carbon; [ ]Argon; [ ]Other: (specify)_____	
♦	2-1.8	Wafer Surface Orientation (with respect to crystal orientation, see item 2-1.3)	[ ]On-orientation: [ ]0.00° ± 1.00°; [ ]0.00° ± _____° [ ]Off-orientation: [ ]0.6° ± 0.4° [ ]2.50° ± 0.50°; [ ]4.00° ± 0.50°; [ ]_____° ± _____°	[ ]SEMI MF26 (X-Ray); [ ] SEMI MF26 (Optical); [ ]JEITA EM-3501; [ ]DIN 50433/1; [ ]DIN 50433/2; [ ]DIN 50433/3; [ ]Other: (specify)_____
	2-1.9	Orthogonal Misorientation (see Figure 2)	[ ] ±5° max; [ ]Other: ±[ ]°, max	
2-2 ELECTRICAL CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice **must** be indicated in order to minimally specify a silicon wafer.)*				
♦	2-2.1	Resistivity Measured at	Nominal [ ] ± Tolerance [ ] Ω·cm [ ]Center Point; [ ]Other: (specify)_____	[ ]SEMI MF84; [ ] SEMI MF673; [ ]DIN 50431; [ ]DIN50445; [ ]Other: (specify)_____
	2-2.2	Radial Resistivity Variation (RRG)	Not greater than [ ]%	SEMI MF81 Figure 1 – [ ]A, [ ]B, [ ]C, [ ]D; [ ]DIN 50435; [ ]Other: (specify) _____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
	2-2.3	Resistivity Striations	Not greater than [ ]%	[ ]SEMI MF525; [ ]Other: (specify)_____
	2-2.4	Minority Carrier Lifetime	Greater than [ ] μs	SEMI MF28 [ ]A, [ ]B; SEMI MF391 [ ]A, [ ]B; [ ]SEMI MF1388; [ ]SEMI MF1535; [ ]JEITA EM-3502; [ ]JIS H 0604; [ ]DIN 50440/1; [ ]Other: (specify)_____
2-3 CHEMICAL CHARACTERISTICS				
	2-3.1	Oxygen Concentration (Values using the following Calibration Factor, see SEMI M44)	Nominal [ ] ± Tolerance [ ]; [ ]× 10^{17} cm^{-3}; [ ]ppma [ ]IOC-88; [ ] Old ASTM; [ ]New ASTM or Old DIN; [ ] Original JEITA; [ ]Other: (specify)_____	IR (Interstitial): [ ] SEMI MF1188; [ ] SEMI MF1619; [ ] JEIDA EM-3504; [ ] DIN 50438-1; [ ]Other: (specify)_____ SIMS (Total): [ ] SEMI MF1366; [ ]GFA (Total)
	2-3.2	Radial Oxygen Variation	Not greater than [ ]%	SEMI MF951 Plan [ ]A1; [ ]A2; [ ]A3; [ ]B; [ ]B1; [ ]C; [ ]D; [ ]Other: (specify)_____
	2-3.3	Carbon Concentration (Background, cf 2-1.7)	Not greater than [ ] [ ]ppma; [ ] × $10^{16}cm^{-3}$	[ ] SEMI MF1391; JEITA EM-3503; [ ]DIN 50438/2; [ ]Other: (specify)_____
	2-3.4	Boron Concentration in Heavily Doped *n*-type Silicon	Not greater than [ ] ppba	[ ]SEMI MF1528; [ ]Other: (specify)_____
	2-3.5	Bulk Iron Content	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^3	[ ]SEMI MF978 (DLTS); [ ]SEMI MF391(SPV); [ ] SEMI MF1535; [ ]JEITA EM3502 (μτ); [ ]Other (specify): _____
2-4 STRUCTURAL CHARACTERISTICS				
	2-4.1	Dislocation Etch Pit Density	[ ]Not greater than [ ]/cm^2	[ ]SEMI MF1809; [ ]JIS H 0609; [ ]DIN 50434; [ ]DIN 50443/1; [ ]Other: (specify)_____
	2-4.2	Slip	[ ]None [ ]Other: (specify)_____	[ ]SEMI MF1809; [ ]JIS H 0609; [ ]DIN 50434; [ ]DIN 50443/1; [ ]Other: (specify)_____
	2-4.3	Lineage	[ ]None [ ]Other: (specify)_____	[ ]SEMI MF1809; [ ]JIS H 0609; [ ]DIN 50434; [ ]DIN 50443/1; [ ]Other: (specify)_____
	2-4.4	Twin Boundary	[ ]None [ ]Other: (specify)_____	[ ]SEMI MF1809; [ ]JIS H 0609; [ ]DIN 50434; [ ]DIN 50443/1; [ ]Other: (specify)_____
	2-4.5	Swirl	[ ]Not greater than [ ]% of wafer area	[ ]SEMI MF1809; [ ]JIS H 0609; [ ]DIN 50434; [ ]DIN 50443/1; [ ]Other: (specify)_____
	2-4.6	Shallow Pits	Not greater than [ ]/cm^2	[ ]SEMI MF1727; [ ]SEMI MF1049; [ ]Other: (specify)_____

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		ITEM	SPECIFICATION	MEASUREMENT METHOD
	2-4.7	Oxidation Induced Stacking Faults (OSF)	Not greater than [ ]/cm^2	Test Cycle: [ ]SEMI MF1727; [ ]JIS H 0609; [ ]Other: (specify)_____ Observation Method: [ ]SEMI MF1726; [ ]JIS H 0609; [ ]DIN 50443/1; [ ]Other: (specify)_____
	2-4.8	Oxide Precipitates, BMD	Range: [ ] to [ ] Unit: [ ] cm^{-2}; [ ] cm^{-3}	Test Cycle: SEMI MF1239 [ ]A, [ ]B; p [ ]Other: (specify)_____
	2-4.9	Interstitial Oxygen Reduction ($\Delta[O_i]$)	Range: [ ] to [ ] [ ]ppma; [ ]× 10^{17} cm^{-3}	Test Cycle: SEMI MF1239 [ ]A, [ ]B; [ ]Other: (specify)_____
	2-4.10	Bulk defects by X-ray topography	[ ]Density:_____ cm^{-3}	[ ]DIN 50443/1; [ ]Other: (specify)_____
2-5 WAFER PREPARATION CHARACTERISTICS				
	2-5.1	Wafer ID Marking	[ ]None; [ ]SEMI M12; [ ]SEMI M13; [ ]SEMI T1; [ ]SEMI T2; [ ]SEMI T7; [ ]SEMI T7 + optional alphanumeric mark (see Figure 3); [ ]Other: (specify) _____	
	2-5.2	Front Surface Thin Film(s)	[ ]None [ ]Description:	
	2-5.3	Denuded Zone	[ ]None [ ]Description:	
	2-5.4	Extrinsic Gettering	[ ]None [ ]Description:	
	2-5.5	Backseal	[ ]None [ ]Description:	
	2-5.6	Annealing	[ ]None [ ]Description:	
	2-5.7	Edge Surface Condition	[ ]Ground; [ ]Etched; [ ]Polished[#2]	
	2-5.8	Back Surface Condition	[ ]Supplier Option; [ ]Caustic Etched; [ ]Acid Etched; [ ]Polished[#2] (see Item 2-9.8 for required gloss level)	
2-6 DIMENSIONAL CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice **must** be indicated in order to minimally specify a silicon wafer.* THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY OR THEY MAY BE [ ]Specified According to Category 1.__ Polished Wafers (see Tables 4–9). If the items are specified according to a standard wafer Category, the items marked with the symbol ➲ need not be entered individually.				
♦➲	2-6.1	Diameter	[ ]Nominal [ ] ± Tolerance [ ] mm	[ ]SEMI MF2074; [ ]DIN 50441/4; [ ]Other: (specify)_____
♦➲	2-6.2	Fiducial Dimensions	Flat [ ]Length or [ ]Diameter: [ ]Nominal [ ] ± Tolerance [ ] mm [ ]Notch Dimensions (see Figure 5)	[ ]SEMI MF671 (Flat Length); [ ]DIN 50441/4 (Flat Diameter); [ ]SEMI MF1152 (Notch Dimensions); [ ]Other: (specify)_____
♦➲	2-6.3	Primary Flat/Notch Orientation	[ ] (crystal axis) [_____] ± ____°	[ ]SEMI MF847 (Flat); [ ] Other: (specify)_____
♦➲	2-6.4	Secondary Flat Length	[ ]None; [ ]Other: _____±____mm	[ ]SEMI MF671; [ ]Other: (specify)_____
♦➲	2-6.5	Secondary Flat Location (see Figure 4)	[ ]None; [ ]Other: (θ) _____°	
♦➲	2-6.6	Edge Profile	[ ] (specify)_____	SEMI MF928: Method A [ ], Method B [ ]; DIN 50441/2: Procedure 1 [ ], Procedure 2 [ ]; [ ]Other: (specify)_____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
♦ ➲	2-6.7	Thickness	[ ]Nominal [ ] ± Tolerance [ ] µm	[ ]SEMI MF533; [ ]SEMI MF1530; [ ]JIS H 0611; [ ]DIN 50441/1; [ ]Other: (specify)_____
➲	2-6.8	Total Thickness Variation (TTV)	[ ] [ ] µm, max.	[ ]SEMI MF533; [ ]JIS H 0611; [ ]DIN 50441/1 (five or nine point); [ ]SEMI MF657 (partial scan); [ ]SEMI MF1530 (full scan); [ ]Other: (specify)_____
➲	2-6.9	Bow	[ ] [ ] µm, max	[ ]SEMI MF534; [ ]JIS H 0611; [ ]Other: (specify)_____
➲	2-6.10	Warp	[ ] [ ] µm, max	[ ]SEMI MF657; [ ]SEMI MF1390; [ ]Other: (specify)_____
	2-6.11	Sori	[ ] [ ] µm, max	[ ] SEMI MF1451; [ ] JEITA EM-3401; [ ]Other: (specify)_____
	2-6.12	Flatness, Global	Acronym:[#3] [ ] [ ] [ ] [ ] [ ] Value: [ ]µm	[ ]SEMI MF1530; [ ]DIN 50441/3; [ ]JEITA EM-3401; [ ]Other: (specify)_____
	2-6.13	Flatness, Site	Acronym:[#3] [ ] [ ] [ ] [ ] [ ] Value: Not greater than [ ]µm Site Size ___ mm × ___ mm [ ]% Usable Area_____ [ ]Include partial sites; [ ]Do not include partial sites Offset: x = [ ] mm, y = [ ] mm	[ ]SEMI MF1530; [ ]Other: (specify)_____
	2-6.14	Nanotopography	[ ]SEMI M43 (specify conditions):_____	
2-7 FRONT SURFACE CHEMISTRY				
	2-7.1	Surface Metal Contamination		
	2-7.1.1	Sodium	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	2-7.1.2	Aluminum	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	2-7.1.3	Potassium	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.1.4	Chromium	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.1.5	Iron	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
	2-7.1.6	Nickel	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.1.7	Copper	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.1.8	Zinc	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.1.9	Calcium	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.2	Other Surface Metals (List Separately)		
	2-7.2.1	_____	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.2.2	_____	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.2.3	_____	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.2.4	_____	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.2.5	_____	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.2.6	_____	[ ]Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	2-7.3	Surface Organics	[ ]Not greater than [ ]ng/cm^2	[ ]SEMI MF1982; [ ]Other: (specify)_____

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