SEMI M1-1117
SPECIFICATION FOR POLISHED SINGLE CRYSTAL SILICON WAFERS

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1 Purpose

1.1 Single crystal silicon wafers are utilized for essentially all integrated circuits and many other semiconductor devices. To permit common processing equipment to be used in multiple device fabrication lines, it is essential for the wafer dimensions to be standardized.

1.2 In addition, as technology advances to smaller and smaller dimensions for the elements of high-density integrated circuits, it has become of interest to standardize additional properties of the wafers.

1.3 This Specification provides the essential dimensional and certain other common characteristics of silicon wafers, including polished wafers as well as substrates for epitaxial and certain other kinds of silicon wafers.

2 Scope

2.1 This Specification covers ordering information and certain requirements for high-purity (electronic grade), single crystal polished silicon wafers used in semiconductor device and integrated circuit manufacturing. Such wafers are usually sliced from cylindrical single-crystal ingots that have been ground to a uniform diameter prior to slicing. This Specification also covers ordering information and certain requirements for electronic grade silicon wafers intended for use as substrates (or starting wafers) for other kinds of wafers, including epitaxial, annealed, and SOI wafers.

2.2 Standardized dimensional requirements are provided for a large number of categories of standardized polished wafers as listed in the tables in § 6.

2.3 Values given for thickness, total thickness variation (TTV), bow, and warp apply only to wafers prior to application of back surface films, extrinsic gettering treatments, or other thermal treatments.

2.4 This Specification applies specifically to prime silicon wafers with at least one chem-mechanically polished surface. Ground, lapped, and unpolished wafers are not covered but this Specification may provide guidance in connection with their procurement.

2.5 This Specification also provides guides for the specification of 300 and 450 mm diameter prime silicon wafers for the 32, 22, and 16 nm technology generations. These are included in Related Information 1.

2.6 This Specification does not cover requirements for the following related types of silicon materials and wafers:

- Polycrystalline silicon (see SEMI M16 or JEITA EM-3601A),
- Epitaxial wafers (see SEMI M62),
- Epitaxial wafers with buried layer (see SEMI M61),
- Test wafers (see SEMI M8),
- Premium wafers (see SEMI M24),
- Reclaimed wafers (see SEMI M38),
- Annealed wafers (see SEMI M57),
- SOI wafers (see SEMI M41, SEMI M71, or JEITA EM-3603B), and
- Solar-grade silicon wafers (see SEMI PV22).

They do, however, provide the ordering information for test, premium, and reclaimed wafers, as well as the ordering information for the polished substrates and starting wafers used to prepare epitaxial, annealed, and SOI wafers.

2.7 For reference purposes, U.S. customary units shall be used for wafers of 2 inch and 3 inch nominal diameters, and SI (system international, commonly called metric) units for 100 mm and larger diameter wafers.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

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3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M8 — Specification for Polished Monocrystalline Silicon Test Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M16 — Specification for Polycrystalline Silicon

SEMI M18 — Guide for Developing Specification Forms for Order Entry of Silicon Wafers

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M26 — Guide for the Re-Use of 100, 125, 150, and 200 mm Wafer Shipping Boxes Used to Transport Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M38 — Specification for Polished Reclaimed Silicon Wafers

SEMI M40 — Guide for Measurement of Roughness of Planar Surfaces on Silicon Wafers

SEMI M41 — Specification of Silicon-On-Insulator (SOI) for Power Device/ICs

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI M44 — Guide to Conversion Factors for Interstitial Oxygen in Silicon

SEMI M45 — Specification for 300 mm Wafer Shipping System

SEMI M49 — Guide for Specifying Geometry Measurement Systems for Silicon Wafers for the 130 nm to 16 nm Technology Generations

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Reference Spheres on Unpatterned Semiconductor Wafer Surfaces

SEMI M57 — Guide for Specifying Silicon Annealed Wafers

SEMI M58 — Test Method for Evaluating DMA-Based Particle Deposition Systems and Processes

SEMI M59 — Terminology for Silicon Technology

SEMI M61 — Specification for Silicon Epitaxial Wafers with Buried Layers

SEMI M62 — Specifications for Silicon Epitaxial Wafers

SEMI M67 — Practice for Determining Wafer Near-Edge Geometry from a Measured Thickness Data Array Using the ESFQR, ESFQD and ESBIR Metrics

SEMI M68 — Test Method for Determining Wafer Near-Edge Geometry from a Measured Height Data Array Using a Curvature Metric, ZDD

SEMI M70 — Test Method for Determining Wafer-Near-Edge Geometry Using Partial Wafer Site Flatness

SEMI M71 — Specification for Silicon-On-Insulator (SOI) Wafers for CMOS LSI

SEMI M73 — Test Methods for Extracting Relevant Characteristics from Measured Wafer Edge Profiles

SEMI M77 — Test Method for Determining Wafer Near-Edge Geometry Using Roll-Off Amount, ROA

SEMI M78 — Guide for Determining Nanotopography of Unpatterned Silicon Wafers for the 130 nm to 22 nm Generations in High Volume Manufacturing

SEMI M85 — Guide for the Measurement of Trace Metal Contamination on Silicon Wafers Surface by Inductively Coupled Plasma Mass Spectrometry

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SEMI MF26 — Test Method for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF28 — Test Methods for Minority-Carrier Lifetime in Bulk Germanium and Silicon by Measurement of Photoconductive Decay

SEMI MF42 — Test Method for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF84 — Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF391 — Test Methods for Minority Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF525 — Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF533 — Test Method for Thickness and Thickness of Variation of Silicon Wafers

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Test Method for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

SEMI MF847 — Test Method for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Test Method for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF951 — Test Method for Determination of Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF978 — Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

SEMI MF1048 — Test Method for Measuring Reflective Total Integrated Scatter

SEMI MF1049 — Practice for Shallow Etch Pit Detection on Silicon Wafers

SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1188 — Test Method for Interstitial Oxygen Content of Silicon by Infrared Absorption with Short Baseline

SEMI MF1239 — Test Method for Oxygen Precipitation Characteristics of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1388 — Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of Metal-Oxide-Silicon (MOS) Capacitors

SEMI MF1390 — Test Method for Measuring Bow and Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1391 — Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1528 — Test Method for Measuring Boron Contamination in Heavily Doped *n*-Type Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1535 — Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and Epi Substrates by Secondary Ion Mass Spectrometry

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SEMI MF1619 — Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with *p*-Polarized Radiation Incident at the Brewster Angle

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon

SEMI MF1982 — Test Method for Analyzing Organic Contaminants on Silicon Wafer Surfaces by Thermal Desorption Gas Chromatography

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI PV13 — Test Method for Contactless Excess-Charge-Carrier Recombination Lifetime Measurement in Silicon Wafers, Ingots, and Bricks Using an Eddy-Current Sensor

SEMI PV22 — Specification for Silicon Wafers for Use in Photovoltaic Solar Cells

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-sided Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ANSI Standard*[1]

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standards*[2]

ASTM D523 — Standard Test Method for Specular Gloss

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With Specific Precision, the Average for a Characteristic of a Lot or Process

3.4 *DIN Standards*[3]

3.5 *European Community Directive*[4]

2002/95/EC — On the restriction of the use of certain hazardous substances in electrical and electronic equipment

3.6 *ISO Standards*[5]

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence (TXRF) Spectroscopy

ISO 17331 — Surface Chemical Analysis – Chemical Methods for the Collection of Elements from the Surface of Silicon-Wafer Working Reference Materials and Their Determination by Total-Reflection X-ray Fluorescence (TXRF) Spectroscopy

3.7 *JEITA Standards*[6]

JEITA EM-3401 — Terminology of Silicon Wafer Flatness

[1] American National Standards Institute, 25 West 43rd Street, New York, NY 10036, USA; Telephone: +1.212.642.4900, Fax: +1.212.398.0023, http://www.ansi.org

[2] ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, http://www.astm.org

[3] Deutsches Institut für Normung (DIN) silicon standards are no longer available in either English or German editions from the publisher of DIN standards, Beuth Verlag GmbH, http://www.beuth.de. Consequently these standards have been removed from this section and moved to § 13 Related Documents.

[4] *Official Journal of the European Union*, February 13, 2003 Available for downloading from the following URL: http://164.36.164.20/sustainability/pdfs/finalrohs.pdf

[5] International Organization for Standardization, ISO Central Secretariat, 1, ch. de la Voie-Creuse, CP 56, CH-1211 Geneva 20, Switzerland; Telephone: +41.22.749.01.11, Fax: +41.22.733.34.30, http://www.iso.org

[6] Japan Electronics and Information Technology Industries Association, Ote Center Building, 1-1-3, Otemachi, Chiyoda-ku, Tokyo 100-0004, Japan; http://www.jeita.or.jp

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JEITA EM-3501 — Standard Methods for Determining the Orientation of a Semiconductor Silicon Single Crystal

JEITA EM-3502 — Test Method for Recombination Lifetime in Silicon Wafers by Measurement of Photoconductivity Decay by Microwave Reflectance

JEITA EM-3503 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

JEITA EM-3504 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

JEITA EM-3508 — Test Method for Bulk Micro Defect Density and Denuded Zone Width in Annealed Silicon Wafers

JEITA EM-3601A — Standard Specification for High Purity Polycrystalline Silicon

JEITA EM-3602 — Standard Specification for Dimensional Properties of Silicon Wafers with Specular Surfaces

JEITA EM-3603B — Standard of SOI Wafers and Metrology

3.8 *JIS Standards*[7]

JIS H 0604 — Measuring of Minority-Carrier Lifetime in Silicon Single Crystal by Photoconductive Decay Method

JIS H 0607 — Determination of Conductivity Type in Germanium by Thermoelectromotive Method

JIS H 0609 — Test methods of Crystalline Defects in Silicon by Preferential Etch Techniques

JIS H 0611 — Methods of Measurement of Thickness, Thickness Variation and Bow of Silicon Wafer

JIS H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

JIS H 0615 — Test Method for Determination of Impurity Concentrations in Silicon Crystal by Photoluminescence Spectroscopy

JIS Z 8741 — Specular Glossiness – Methods of Measurement

3.9 *MHI Standard*[8]

CEA 556-C — Outer Shipping Container Bar Code Label Standard

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Terms, acronyms, and symbols associated with silicon wafers and silicon technology are listed and defined in SEMI M59.

5 Ordering Information

5.1 A complete purchase specification requires that many physical properties be specified along with test methods suitable for determining their magnitude. Thus, purchase orders for silicon wafers furnished to this specification shall include the following items. These items are indicated on the Silicon Wafer Specification Format for Order Entry, Parts 1 and 2, shown in Table 1, with a ♦ symbol in the left-most column.

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.8 Wafer Surface Orientation

[7] Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: +81.3.3583.8005; Fax: +81.3.3586.2014; http://www.jsa.or.jp

[8] Material Handling Institute, 8720 Red Oak Blvd., Suite 201, Charlotte, NC 28217, USA; Telephone: +1.704.676.1190; Fax: +1.704.676.1199; http://www.mhi.org

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- 2-2.1 Resistivity
- 2-6.1 Diameter
- 2-6.2 Fiducial Dimensions
- 2-6.3 Primary Flat/Notch Orientation
- 2-6.4 Secondary Flat Length
- 2-6.5 Secondary Flat Location
- 2-6.6 Edge profile
- 2-6.7 Thickness

5.2 In addition, the purchase order must indicate the test procedure to be used in evaluating each of those items for which alternate test procedures exist either as different test methods or as different procedures within a standardized test method.

5.3 The following items must also be included in the purchase order:

5.3.1 Lot acceptance procedures,

5.3.2 Certification (if required) and

5.3.3 Packing and shipping container labeling requirements.

5.4 Finally, many other characteristics may also be specified in purchase orders for silicon wafers. These shall be selected from the other items listed in the Silicon Wafer Specification Format for Order Entry, Parts 1 and 2 (see Table 1).

5.5 The parameter values provided in the requirements tables in § 6 may be used to identify appropriate values in the specification without selecting a value for each line. However, even if these requirements table values are used, the desired test methodology must be selected in accordance with ¶ 5.2.

5.6 It is essential that all choices for the items selected to be specified be made in order not to have unspecified parameters that would lead to surprises between supplier and customer. This is particularly important in the specification of wafer site flatness, for which a variety of parameters must be selected as outlined in Appendix 1.

5.7 Of the various items listed, the following (listed in the order in which they appear in Table 1) are most often selected, especially for wafers to be used for advanced integrated circuit manufacture:

- 2-1.6 Nominal Edge Exclusion (to define the fixed quality area [FQA], see Figure 1.)
- 2-4 Structural Characteristics
- 2-5.1 Wafer ID Marking
- 2-6.6 Edge Profile
- 2-6.8 Total Thickness Variation (TTV or GBIR, see ¶ R4-7.7)
- 2-6.10 Warp (and sometimes 2-6.9 Bow or 2-6.11 Sori)
- 2-6.13 Site Flatness (SFQR)
- 2-8.5 Localized Light Scatterers (LLS)

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Table 1 Silicon Wafer Specification Format for Order Entry, Parts 1 and 2

Part 1 General Information		
ITEM	*INFORMATION*	*DATE:*
Customer Name		
Purchase Order Number		
Line Number		
Item Number		
General Specification Number		
Revision Level		
Part Number/Revision		

			Part 2 Polished Wafer or Substrate	
	ITEM		*SPECIFICATION*	*MEASUREMENT METHOD*
2-1 GENERAL CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice* ***must*** *be indicated in order to minimally specify a silicon wafer.)*				
♦	2-1.1	Growth Method	[ ] Cz; [ ] FZ; [ ] MCz; [ ] Supplier option of Cz or MCz	
	2-1.2	Use of Refined Polysilicon	[ ] Permitted; [ ] Not permitted	
♦	2-1.3	Crystal Orientation	[ ] (100); [ ] (111); [ ] (110); [ ] Other: (specify) ( )	[ ] SEMI MF26 (X-ray); [ ] SEMI MF26 (Optical); [ ] JEITA EM-3501; [ ] Other: (specify)_____
♦	2-1.4	Conductivity Type	[ ] *p;* [ ] *n*	[ ] SEMI MF42; [ ] JIS H 0607; [ ] Other: (specify)_____
♦	2-1.5	Dopant	[ ] B; [ ] P; [ ] Sb; [ ] As; [ ] Neutron Transmutation Doped; [ ] Other: (specify) _____	
	2-1.6	Nominal Edge Exclusion[#1] (see Figure 1)	[ ] 1.5 mm; [ ] 2 mm; [ ] 3 mm; [ ] 5 mm; [ ] Other: (specify)_____mm	
	2-1.7	Co-dopant in Crystal	[ ] None; [ ] Nitrogen; [ ] Carbon; [ ] Nitrogen and Carbon; [ ] Argon; [ ] Other: (specify)_____	
♦	2-1.8	Wafer Surface Orientation (with respect to crystal orientation, see Item 2-1.3)	[ ] On-orientation: [ ] 0.00° ± 1.00°; [ ] 0.00° ± ____° [ ] Off-orientation: [ ] 0.6° ± 0.4° [ ] 2.50° ± 0.50°; [ ] 4.00° ± 0.50°; [ ] _____° ± _____°	[ ] SEMI MF26 (X-ray); [ ] SEMI MF26 (Optical); [ ] JEITA EM-3501; [ ] Other: (specify)_____
	2-1.9	Orthogonal Misorientation (see Figure 2)	[ ] ±5° max; [ ] Other: ± [ ]°, max	
2-2 ELECTRICAL CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice* ***must*** *be indicated in order to minimally specify a silicon wafer.)*				
♦	2-2.1	Resistivity Measured at	Nominal [ ] ± Tolerance [ ] Ω·cm [ ] Center Point; [ ] Other: (specify)_____	[ ] SEMI MF84; [ ] SEMI MF673; [ ] Other: (specify)_____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
	2-2.2	Radial Resistivity Variation (RRG)	Not greater than [ ]%	SEMI MF81 Figure 1 – [ ] A, [ ] B, [ ] C, [ ] D; [ ] Other: (specify) _____
	2-2.3	Resistivity Striations	Not greater than [ ]%	[ ] SEMI MF525; [ ] Other: (specify)_____
	2-2.4	Minority Carrier Lifetime	Greater than [ ] µs	SEMI MF28 [ ] A, [ ] B; SEMI MF391 [ ] A, [ ] B; [ ] SEMI MF1388; [ ] SEMI MF1535; [ ] JEITA EM-3502; [ ] JIS H 0604; [ ] SEMI PV13 [ ] Other: (specify)_____
2-3 CHEMICAL CHARACTERISTICS				
	2-3.1	Oxygen Concentration (Values using the following Calibration Factor, see SEMI M44)	Nominal [ ] ± Tolerance [ ]; [ ] 10^{17} cm^{-3}; [ ] ppma [ ] IOC-88; [ ] Old ASTM; [ ] New ASTM or DIN; [ ] Original JEITA; [ ] Other: (specify)_____	IR (Interstitial): [ ] SEMI MF1188; [ ] SEMI MF1619; [ ] JEIDA EM-3504; [ ] Other: (specify)_____ [ ] SIMS (Total): SEMI MF1366; [ ] GFA (Total)
	2-3.2	Radial Oxygen Variation	Not greater than [ ]%	SEMI MF951 Plan [ ] A1; [ ] A2; [ ] A3; [ ] B; [ ] B1; [ ] C; [ ] D; [ ] Other: (specify)_____
	2-3.3	Carbon Concentration (Background, cf. 2-1.7)	Not greater than [ ] [ ] ppma; [ ] × $10^{16}cm^{-3}$	[ ] SEMI MF1391; [ ] JEITA EM-3503; [ ] Other: (specify)_____
	2-3.4	Boron Concentration in Heavily Doped *n*-type Silicon	Not greater than [ ] ppba	[ ] SEMI MF1528; [ ] Other: (specify)_____
	2-3.5	Bulk Iron Content	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^3	[ ] SEMI MF978 (DLTS); [ ] SEMI MF391(SPV); [ ] SEMI MF1535; [ ] JEITA EM-3502 (µτ); [ ] SEMI PV13 [ ] Other (specify): _____
	2-3.6	Hazardous Substances Restrictions	[ ] EC Directive 2002/95/EC [ ] Other: (specify) _____	See Appendix 2 Specify: _____
2-4 STRUCTURAL CHARACTERISTICS				
	2-4.1	Dislocation Etch Pit Density	[ ] Not greater than [ ]/cm^2	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.2	Slip	[ ] None [ ] Other: (specify)_____	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.3	Lineage	[ ] None [ ] Other: (specify)_____	[ ] SEMI MF1809; [ ] JIS H 0609; [[ ] Other: (specify)_____
	2-4.4	Twin Boundary	[ ] None [ ] Other: (specify)_____	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.5	Swirl	[ ] Not greater than [ ]% of wafer area	[ ] SEMI MF1809; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.6	Shallow Pits	Not greater than [ ]/cm^2	[ ] SEMI MF1727; [ ] SEMI MF1049; [ ] Other: (specify)_____

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	ITEM		SPECIFICATION	MEASUREMENT METHOD
	2-4.7	Oxidation Induced Stacking Faults (OSF)	Not greater than [ ]/cm^2	Test Cycle: [ ] SEMI MF1727; [ ] JIS H 0609; [ ] Other: (specify)_____ Observation Method: [ ] SEMI MF1726; [ ] JIS H 0609; [ ] Other: (specify)_____
	2-4.8	Oxide Precipitates	Range: [ ] to [ ] Unit: [ ] cm^{-2}; [ ] cm^{-3}	Test Cycle: SEMI MF1239 [ ] A, [ ] B; [ ] Other: (specify)_____
	2-4.9	Interstitial Oxygen Reduction ($\Delta[O_i]$)	Range: [ ] to [ ] [ ] ppma; [ ] × 10^{17} cm^{-3}	Test Cycle: SEMI MF1239 [ ] A, [ ] B; [ ] Other: (specify)_____
	2-4.10	Bulk defects by X-ray topography	[ ] Density:_____ cm^{-3}	[ ] Specify_____
	2-4.11	Bulk Micro Defects	[ ] Density:_____ cm^{-3}	[ ] JEITA EM-3508; [ ] Other: (specify)_____
2-5 WAFER PREPARATION CHARACTERISTICS				
	2-5.1	Wafer ID Marking	[ ] None; [ ] SEMI M12; [ ] SEMI M13; [ ] SEMI T7; [ ] SEMI T7 + optional alphanumeric mark (see Figure 3); [ ] Other: (specify) _____	
	2-5.2	Front Surface Thin Film(s)	[ ] None [ ] Description:	
	2-5.3	Denuded Zone	[ ] None [ ] Width: _____µm	[ ] JEITA EM-3508; [ ] Other: (specify)_____
	2-5.4	Extrinsic Gettering	[ ] None [ ] Description:	
	2-5.5	Backseal	[ ] None [ ] Description:	
	2-5.6	Annealing	[ ] None [ ] Description:	
	2-5.7	Edge Surface Condition	[ ] Ground; [ ] Etched; [ ] Polished[#2]	
	2-5.8	Back Surface Condition	[ ] Supplier Option; [ ] Caustic Etched; [ ] Acid Etched; [ ] Polished[#2] (see Item 2-9.8 for required gloss level)	
2-6 DIMENSIONAL CHARACTERISTICS *(Note that ♦ indicates a required item for which a value or choice* ***must*** *be indicated in order to minimally specify a silicon wafer.)*				
	THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY OR THEY MAY BE [ ] Specified According to Category 1.__ Polished Wafers (see Tables 3 through 9). If the items are specified according to a standard wafer Category, all the items in these tables need not be entered individually.			
♦➲	2-6.1	Diameter	[ ] Nominal [ ] ± Tolerance [ ] mm	[ ] SEMI MF2074; [ ] Other: (specify)_____
♦➲	2-6.2	Dimensions of Flat and Notch Fiducials	Flat [ ] Length or [ ] Diameter:[#3] [ ] Nominal [ ] ± Tolerance [ ] mm [ ] Notch Dimensions (see Figure 5) [ ] No Notch or Flat	[ ] SEMI MF671 (Flat Length); [ ] SEMI MF1152 (Notch Dimensions); [ ] Other: (specify)_____
♦➲	2-6.3	Orientation of Primary Flat, Notch, or Primary Orientation Fiducial Mark	[ ] (crystal axis) [_____]±____°	[ ] SEMI MF847 (Flat); [ ] Other: (specify)_____
♦➲	2-6.4	Secondary Flat Length	[ ] None; [ ] Other: _____±____mm	[ ] SEMI MF671; [ ] Other: (specify)_____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
♦➲	2-6.5	Angular Location of Secondary Flat (see Figure 4) or of Secondary and Tertiary Orientation Fiducial Marks (see Figure 6)	[ ] None; [ ] Other: (θ) _____±_____° [ ] None; [ ] see Table 9 [ ] None; [ ] see Table 9	
♦➲	2-6.6	Template-Coordinate Based Edge Profile Specification	[ ] T/3 template [ ] T/4 template [ ] Other template (specify)_____	SEMI MF928: Method A [ ], Method B [ ] Other: (specify)_____
		Profile-Parameter-Based Edge Profile Specification	[ ] Front edge width ____µm ± ____µm [ ] Front bevel angle ____° ± ____° [ ] Front shoulder radius ____µm ± ___µm [ ] Back shoulder radius ____µm ± ___µm [ ] Back bevel angle ____° ± ____° [ ] Back edge width ____µm ± ___µm [ ] Front apex angle ____° ± ____° (optional) [ ] Back apex angle ____° ± ____° (optional)	SEMI M73:[#4] Method 1 [ ], Method 2 [ ]; [ ] Other: (specify)_____
♦➲	2-6.7	Thickness	[ ] Nominal [ ] ± Tolerance [ ] µm	[ ] SEMI MF533; [ ] SEMI MF1530; [ ] JIS H 0611; [ ] Other: (specify)_____
➲	2-6.8	Total Thickness Variation (TTV)	[ ] [ ] µm, max	[ ] SEMI MF533; [ ] JIS H 0611; [ ] SEMI MF1530 (full scan); [ ] Other: (specify)_____
➲	2-6.9	Bow	[ ] [ ] µm, max	[ ] SEMI MF1390; [ ] JIS H 0611; [ ] Other: (specify)_____
➲	2-6.10	Warp	[ ] [ ] µm, max	[ ] SEMI MF1390; [ ] Other: (specify)_____
	2-6.11	Sori	[ ] [ ] µm, max	[ ] SEMI MF1451; [ ] JEITA EM-3401; [ ] Other: (specify)_____
	2-6.12	Flatness, Global	Acronym:[#5] [ ] [ ] [ ] [ ] Value: [ ] µm	[ ] SEMI MF1530; [ ] JEITA EM-3401; [ ] Other: (specify)_____
	2-6.13	Flatness, Site	Acronym:[#5] [ ] [ ] [ ] [ ] Value: Not greater than [ ] µm Site Size ___ mm × ___ mm [ ]% Usable Area_____ [ ] Include partial sites; [ ] Do not include partial sites Offset: x = [ ] mm, y = [ ] mm	[ ] SEMI MF1530; [ ] Other: (specify)_____
	2-6.14	Nanotopography	[ ] as described in SEMI M43 (specify conditions):_____ [ ] ≤_____ nm for 2 mm analysis area [ ] ≤_____ nm for 10 mm analysis area	 SEMI M78 SEMI M78
	2-6.15	Near Edge Geometry	[ ] ESFQR, [ ] ESFQD. or [ ] ESBIR [ ] ZDD [ ] L-ROA, [ ] P-ROA [ ] PSFQR, [ ] PSFQD	SEMI M67 SEMI M68 SEMI M77 SEMI M70

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ITEM			SPECIFICATION	MEASUREMENT METHOD
2-7 FRONT SURFACE CHEMISTRY				
	2-7.1	Surface Metal Contamination		
	2-7.1.1	Sodium	[ ] Not greater than [ ] × $10^{[\,]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] Other: (specify)_____
	2-7.1.2	Aluminum	[ ] Not greater than [ ] × $10^{[\,]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] Other: (specify)_____
	2-7.1.3	Potassium	[ ] Not greater than [ ] × $10^{[\,]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.1.4	Chromium	[ ] Not greater than [ ] × $10^{[\,]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.1.5	Iron	[ ] Not greater than [ ] × $10^{[\,]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.1.6	Nickel	[ ] Not greater than [ ] × $10^{[\,]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.1.7	Copper	[ ] Not greater than [ ] × $10^{[\,]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.1.8	Zinc	[ ] Not greater than [ ] × $10^{[\,]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
	2-7.1.9	Calcium	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.2	Other Surface Metals (List Separately)		
	2-7.2.1	_____	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.2.2	_____	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.2.3	_____	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.2.4	_____	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.2.5	_____	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.2.6	_____	[ ] Not greater than [ ] × $10^{[\ ]}$ atoms/cm^2	SEMI M85 [ ] (VPD-ICP-MS; [ ] (DADD-ICP-MS); [ ] AAS; [ ] SEMI MF1617 (SIMS); [ ] ISO 14706 (TXRF); [ ] ISO 17331 (VPD-TXRF); [ ] Other: (specify)_____
	2-7.3	Surface Organics	[ ] Not greater than [ ]ng/cm^2	[ ] SEMI MF1982; [ ] Other: (specify)_____

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ITEM			SPECIFICATION	MEASUREMENT METHOD
2-8 FRONT SURFACE INSPECTION CHARACTERISTICS				
	FOR ALL WAFER DIAMETERS, THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY. ALTERNATIVELY, FOR WAFERS 150 mm OR LESS IN DIAMETER, WHICH CAN BE INSPECTED VISUALLY, THE ITEMS LISTED MAY BE [ ] Specified according to Table 12. If the items are specified according to Table 12, the items marked with the symbol ⮟ need not be entered individually.			
⮟	2-8.1	Scratches – Macro	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.2	Scratches – Micro	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.3	Pits	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.4	Haze	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.5	Localized Light Scatterers (LLS)	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.6	Contamination/Area	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.7	Edge Chips and Indents	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.8	Edge Cracks	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.9	Cracks, Crow's Feet	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.10	Craters	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.11	Dimples	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.12	Grooves	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.13	Mounds	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
⮟	2-8.14	Orange Peel	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____

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	ITEM		SPECIFICATION	MEASUREMENT METHOD
✓	2-8.15	Saw Marks	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS;[#6] [ ] Other: (specify)_____
	2-8.16	Dopant Striation Rings	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-8.17	Stains	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-8.18	rms Microroughness	[ ] Not greater than [ ] nm, over spectral range from [ ] μm^{-1} to [ ] μm^{-1}	[ ] SEMI MF1048; [ ] AFM; [ ] Other: (specify)_____
2-9 BACK SURFACE INSPECTION CHARACTERISTICS				
	FOR ALL WAFER DIAMETERS, THE ITEMS LISTED IN THIS SECTION MAY BE SPECIFIED INDIVIDUALLY. ALTERNATIVELY, FOR WAFERS 150 mm OR LESS IN DIAMETER, WHICH CAN BE INSPECTED VISUALLY, THE ITEMS LISTED MAY BE [ ] Specified according to Table 12. If the items are specified according to Table 12, the items marked with the symbol ✓ need not be entered individually.			
✓	2-9.1	Edge Chips	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.2	Edge Cracks	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
✓	2-9.3	Cracks, Crow's Feet	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
✓	2-9.4	Contamination/Area	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
✓	2-9.5	Saw Marks	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.6	Stains	[ ] None; [ ] Other: (specify)_____	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.7	Roughness	[ ] _____ nm rms	[ ] SEMI M40; [ ] Other: (specify)_____
	2-9.8	Brightness (Gloss)	[ ] _____	[ ] ASTM D523; [ ] JIS Z 8741; [ ] Other: (specify)_____
	2-9.9	Scratches – Macro	[ ] None; [ ] Cum Length =[ ] mm	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.10	Scratches – Micro	[ ] None; [ ] Cum Length =[ ] mm	[ ] SEMI MF523; [ ] JIS H 0614; [ ] Other: (specify)_____
	2-9.11	Localized Light Scatterers	Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] µm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ] SEMI MF523; [ ] JIS H 0614; [ ] SSIS[#6]; [ ] Other: (specify)_____
2-10 OTHER (as required)				

#1 The nominal edge exclusion, *EE*, specifies the diameter of the FQA, which is given by the nominal diameter (see Item 2-6.1) minus 2*EE* (see Figure 1). This quantity provides a center referenced property. Although use of edge referenced properties is discouraged, some equipments and procedures are based on edge referenced dimensions. When this occurs, the quality area is not fixed and some part of the FQA may fall outside the evaluated area, which is generally not a desirable situation.

#2 If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

#3 Note that in the case of {100} *n*-type wafers, 125 mm or smaller in diameter, with a secondary flat (Categories 1.1, 1.2, 1.5, 1.6, and 1.7), the primary and secondary flats are opposing and the concept of flat diameter does not apply because the diameter perpendicular to the flats does not intersect the wafer circumference.

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#4 Thickness reported by parameter based edge profile measurement is typically different from the actual wafer thickness reported by standard dimensional metrology equipment used for flatness and shape. Users are cautioned not to assume the edge profile reported thickness is a valid wafer dimension.

#5 Flatness Acronyms are defined in the Flatness Decision Tree in Appendix 1.

#6 In today's technology, it may be possible to inspect for some of these items using automated surface scanning inspection systems (SSIS). Such systems should be calibrated according to SEMI M53 using polystyrene latex spheres deposited in accordance with SEMI M58. Some indication of the defects separable by such instruments is provided in SEMI M35; however, a standard test procedure has yet to be developed. Application of automated inspection with the use of an SSIS must be agreed upon between supplier and customer.

6 Requirements

6.1 *Standard Wafer Categories*

6.1.1 The standardized dimensions, dimensional tolerance, and characteristics of flat or notch fiducials for various standardized wafer categories are given in Table 3 through 9. These categories of wafer shall meet all requirements listed in the appropriate table, unless an exception is negotiated between supplier and customer and is shown on the purchase order.

NOTE 1: Based upon industry experience with 300 mm wafers, Table 9 for 450 mm wafers contains many more standardized parameters than the table for 300 mm and smaller wafers.

6.1.2 The various categories are summarized here:

Category 1.1	2 inch polished single crystal silicon wafers with secondary flat
Category 1.2	3 inch polished single crystal silicon wafers with secondary flat
Category 1.5	100 mm polished single crystal silicon wafers, 525 µm thick, with secondary flat
Category 1.6	100 mm polished single crystal silicon wafers, 625 µm thick, with secondary flat
Category 1.7	125 mm polished single crystal silicon wafers with secondary flat
Category 1.8.1	150 mm polished single crystal silicon wafers with secondary flat and T/3 edge profile template
Category 1.8.2	150 mm polished single crystal silicon wafers with secondary flat and T/4 edge profile template
Category 1.9.1	200 mm notched polished single crystal silicon wafers with T/3 edge profile template
Category 1.9.2	200 mm notched polished single crystal silicon wafers with T/4 edge profile template
Category 1.9.3	200 mm notched polished single crystal silicon wafers with parameter-specified edge profile
Category 1.10.1	200 mm flatted polished single crystal silicon wafers with T/3 edge profile template without secondary flat
Category 1.10.2	200 mm flatted polished single crystal silicon wafers with T/4 edge profile template without secondary flat
Category 1.11	100 mm flatted polished single crystal silicon wafers without secondary flat
Category 1.12	125 mm flatted polished single crystal silicon wafers without secondary flat
Category 1.13.1	150 mm flatted polished single crystal silicon wafers with T/3 edge profile template without secondary flat
Category 1.13.2	150 mm flatted polished single crystal silicon wafers with T/4 edge profile template without secondary flat
Category 1.15.1	300 mm notched polished single crystal silicon wafers with parameter-specified edge profile
Category 1.16.1	450 mm polished single crystal silicon wafers with notch centered on <110> axis

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Category 1.16.2	450 mm polished single crystal silicon wafers with notch centered on <100> axis
Category 1.16.3	450 mm polished single crystal notchless wafers primary back surface fiducial mark centered on <110> axis

6.1.3 The dimensional characteristics of Category 1.10.1, 1.10.2, 1.11, 1.12, 1.13.1, and 1.13.2 wafers are identical with those specified in JEITA EM-3602, and the dimensional characteristics of Category 1.15.1 wafers are equivalent with those specified in JEITA EM-3602, except for the edge profile characteristics.

6.1.4 Wafers of the same nominal diameter may typically have different dimensional configurations in different regions of the world. Many of these configurations are represented in these tables. In selecting the appropriate standard polished wafer category, consideration should be given to compatibility with processes and equipment generally available in the region of use.

6.2 *General Characteristics*

6.2.1 The crystal growth method shall be modified Czochralski (Cz), float zone (FZ), or magnetic Czochralski (MCz) as specified on the purchase order. In some cases, the supplier is given the option of selecting Cz or MCz.

6.2.1.1 If the Cz or MCz method is used for crystal growth, it may be permissible to utilize refined (previously melted) polysilicon in the growth charge; when this is the case, it should be indicated on the purchase order.

6.2.2 The crystal orientation shall be as specified on the purchase order. Usually either (100) or (111) is specified, but (110) is sometimes specified for polished wafers to be used for making SOI wafers. Occasionally, another orientation, such as (311) or (511), is specified.

6.2.3 The conductivity type shall be either *n* or *p*, as specified on the purchase order.

6.2.4 The dopant shall be specified to match the conductivity type. In general, boron (B) is used for *p*-type material, while phosphorus (P) is most commonly used for *n*-type material. For some applications, antimony (Sb) or arsenic (As) are used to obtain *n*-type wafers. For high power applications, neutron transmutation doping is often used to obtain high resistivity *n*-type wafers.

6.2.5 The nominal edge exclusion, *EE*, specifies the diameter of the FQA, which is given by the nominal diameter minus $2 \cdot EE$ (see Figure 1). The FQA is a center-referenced region that is independent in size from the wafer diameter tolerance, and, if the wafer is flatted, the flat length tolerance. For the purposes of defining the FQA, the periphery of a wafer of nominal dimensions at any location with a fiducial other than a flat is assumed to follow the circumference of a circle with diameter equal to the nominal wafer diameter.

6.2.5.1 The nominal edge exclusion is usually specified as 2 mm or 3 mm, but for notchless wafers *EE* is 1.5 mm. However, it should be noted that not all processes and metrology can work as close to the wafer edge as implied by the nominal edge exclusion (see the discussion in SEMI M49).

6.2.5.2 In addition, it is sometimes necessary to specify additional exclusion areas, such as those for wafer identification marks or wafer holding areas as discussed in SEMI M49.

6.2.5.3 Although use of edge-referenced properties is discouraged, some equipments and procedures are based on edge referenced dimensions. When this occurs, the quality area is not fixed and some part of the FQA may fall outside the evaluated area, which is generally not a desirable situation.

6.2.6 A co-dopant may be required for polished wafers intended to be processed into annealed wafers. Some co-dopants may also be used in connection with control of oxygen precipitation characteristics even when the wafer is not annealed.

6.2.7 *Wafer Surface Orientation* — The wafer shall conform to the surface orientation as specified in the purchase order.

6.2.7.1 For on-orientation wafers, the angular tolerance from the plane perpendicular to the growth axis shall be specified.

6.2.7.2 For off-orientation wafers, both the misorientation angle from the growth axis and its angular tolerance shall be specified.

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6.2.7.2.1 A misorientation angle between 0.2° and 1° (0.6° ± 0.4°) from a (100) plane is frequently used for some epitaxial substrates.

6.2.7.2.2 A misorientation angle of 2.50° or 4° ± 0.5° from a (111) plane is often used for other epitaxial substrates.

6.2.7.3 Orthogonal misorientation is the tilt angle of the normal to a (111) wafer surface toward nearest <110> direction in a plane parallel with the primary flat as indicated in Figure 2.

6.2.7.3.1 The contribution of 5° of orthogonal misorientation to the total off-orientation angle is less than 0.5°.

6.2.7.4 For ion implant applications, the following tolerance issues should be considered:

6.2.7.4.1 For general use where channeling is to be avoided, the current wafer orientation specification of ±1.0° deviation from the [100] axis (perpendicular to the (100) plane of the wafer) is adequate. This Specification is suitable for minimum channeling applications, provided that the appropriate ion implant equipment angle settings are employed.

6.2.7.4.2 Uniform, maximum channeling along the [100] axis perpendicular to the (100) wafer surface is strongly dependent on strict adherence to a 0° tilt angle. To achieve maximum channeling, crystallography requires the orientation to be within ±0.1° of a <100> direction. Also, the customer must remove all overlying oxide, nitride, poly, etc., layers from the wafer prior to a channeling implant. The customer must maintain very rigid control of the ion implant equipment angle setting in order to achieve maximum channeling across the wafer.

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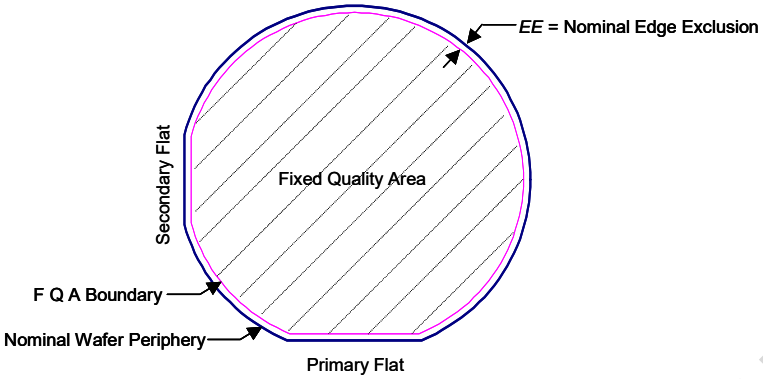
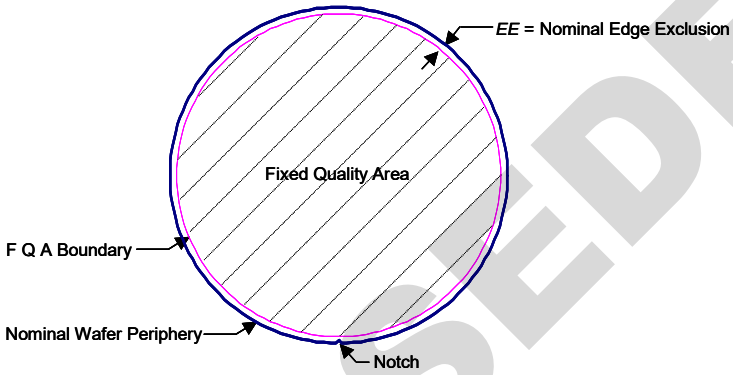
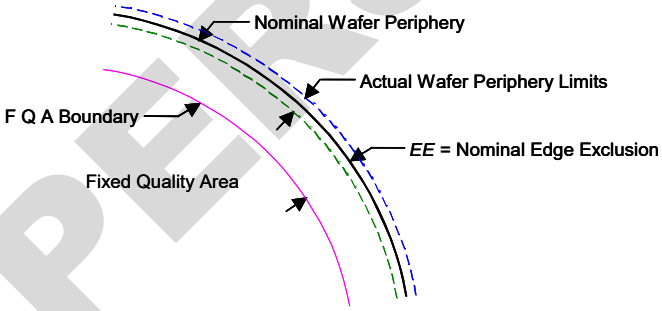


a. Flatted Wafer



b. Notched Wafer



c. Nominal and Actual Wafer Peripheries

Figure 1
Fixed Quality Area

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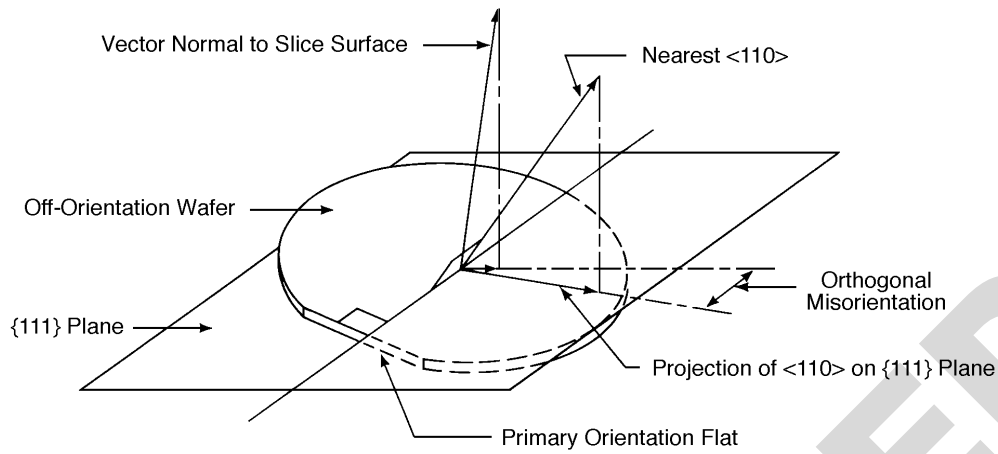

#1 If the off-orientation angle is determined with the seed end up, the polished surface of the finished wafer must be the surface toward the seed end, and vice versa. Polishing of the incorrect wafer surface results in an incorrect wafer tilt, which can cause unwanted pattern shifts and distortions if the wafer is used subsequently for epitaxial layer growth. Because the convention for determining the off-orientation angle is not the same worldwide, it is essential to establish accurately the desired convention.

Figure 2
Orthogonal Misorientation of {111} Wafer

6.2.7.5 The tolerance of ±0.1° is derived from experimental ion implant profile data and ion implant modeling activity for implants into (100) silicon wafers. The ranges for which data was obtained are given in Table 2.

Table 2 Energy Ranges for Ion Implant Modeling

Species	*Energy Range (keV)*
B	15 to 80
BF_2	15 to 65
As	15 to 180

6.3 *Electrical Characteristics*

6.3.1 The center-point room temperature resistivity of the wafers shall conform to the nominal and tolerance values specified on the purchase order.

6.3.2 The wafers shall conform to any requirements specified on the purchase order for radial resistivity variation, resistivity striations and minority carrier lifetime.

6.4 *Chemical Characteristics*

6.4.1 The wafers shall conform to any requirements specified on the purchase order for oxygen concentration, radial oxygen variation, carbon concentration, and, for heavily doped (low resistivity) *n*-type silicon wafers only, compensating boron concentration.

6.4.2 If specified on the purchase order, the wafers shall conform to the hazardous substances regulatory requirements of a jurisdiction. At present, the only publicly available requirements are in EC Directive 2002/95/EC. For information, the maximum concentrations of Cr, Cd, Hg, and Pb in the bulk or on the surface of the wafer required by this directive are given in Appendix 2.

NOTE 2: As requirements from other jurisdictions become publicly available, they will be added to Appendix 2.

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