

SEMI M10-0218 (Reapproved 0423) TERMINOLOGY FOR IDENTIFICATION OF STRUCTURES AND FEATURES SEEN ON GALLIUM ARSENIDE WAFERS

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NOTICE: Paragraphs entitled ‘NOTE:’ are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

1 Scope

1.1 The purpose of this Standard is to list, illustrate, and define various characters, features, and contaminants that are seen on highly polished GaAs wafers and present recommended practices for observation of these defects. These occurrences are frequently referred to as surface defects. The defects and common synonyms are arranged alphabetically in § 4, and each structure is referred to by its most common name and, in some cases, probably origins.

1.2 Two cases of surface preparations are considered in this Standard: (1) surfaces after chemical polishing, and (2) mechanically and chemically polished surfaces.

1.3 This Standard may involve hazardous materials, operations, and equipment.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

2 Referenced Standards and Documents

2.1 None.

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

3 Significance and Use

3.1 This Standard contains a compilation of the most commonly observed singularly discernable structures on polished GaAs surfaces. Ambiguities and uncertainties regarding surface defects may be resolved by reference to this Standard.

4 Definitions

4.1 *apex chip* — any material missing from the edge of a wafer having at least two distinct interior boundaries which form one or more distinct intersections.

4.2 *cavity* — (void): a vacancy or hole in the wafer.

NOTE 1: Usually left by dissolved precipitates and Ga inclusions, As disassociation or created by excess vapor pressure.

4.3 *cell structure* — (block structure): malformations attributable to crystal inhomogeneities and that have their origins in the crystal growth process.

4.4 *chips* — (edge chips, peripheral chips, peripheral indents, surface chips): areas of material mechanically removed from the surface or edge of a wafer.

NOTE 2: Chips indicate crystallographic damage in the adjacent material. The origins of some chips are in the handling of wafers arising from the physical transfer or placement of the specimen for process, measurement, or inspection purposes. The size of a

chip is defined by its maximum radial depth and peripheral chord length as measurable on an orthographic shadow projection of the specimen outline.

4.5 *chuck marks* — any physical mark on either surface of a wafer caused by a chuck or wand.

4.6 *contaminant* — (solvent residue, wax residue, film, mottled surface, smudge): surface feature that cannot be removed by the pre-inspection (non-etching) cleaning.

NOTE 3: Contaminant may be foreign matter on the surface such as localized areas which are smudged, stained, discolored, mottled, etc., or larger areas exhibiting a hazy or cloudy appearance resulting from a film of foreign material.

4.6.1 Solvent residue: type of film found on wafer surfaces after solvent evaporation from the surface. Note: The residue comes from either the solvent itself or material that the solvent has removed from the surface and redeposited. Wax residue: film of wax that migrated onto the wafer surface from several possible sources.

NOTE 4: The wax originally may have been used to hold the crystal in place during slicing or polishing. Excessive heat used in mounting or demounting, during lapping or polishing processes, may cause the wax to polymerize.

4.7 *crack* — cleavage or fracture that extends to the surface of a slice. It may or may not pass through the entire thickness of the slice. Often cracks are caused by the improper handling of wafers.

NOTE 5: Some crack-defect structures can be traced to process related events.

4.8 *dimple* — deformation appearing in mechanically polished GaAs wafers.

NOTE 6: This surface texture can be induced by floating the wafers during the initial stages of polishing.

4.9 *dislocation* — see slip, lineage, pit.

4.10 *edge chip* — see chip.

4.11 *embedded* — (abrasive grains): abrasive particles mechanically forced into the surface of the wafer.

4.12 *etch pit* — see pit.

4.12.1 *film* — see contaminant.

4.12.2 *flake* — material missing from one, but not the other, side of a wafer, whose sole interior boundary is one distinct line or arc not exceeding 2 mm in length, nor projecting into the wafer beyond the specified edge exclusion.

4.12.3 *gallium inclusion* — a segregated Ga-rich droplet incorporated into the surface structure.

NOTE 7: Normally caused by insufficient As vapor pressure at the termination of the crystal growth process or by Ga complexing with some dopants near saturation.

4.12.4 *grain boundary* — see lineage.

4.12.5 *haze* — (cloud, nebula): attributable to light scattering by concentrations of microscopic surface irregularities such as pits, oxides, small ridges or scratches, particles, etc. The light reflection from an individual irregularity probably could not be readily detected by the unaided eye, so haze is a mass effect. It is seen as a high density of tiny reflections.

NOTE 8: This type of contamination may occur during slicing, lapping, or polishing.

4.12.6 *lamella* — a special case of the twin. A multiple twin, extremely thin and relatively long, which may intersect more than one plane.

4.12.7 *lineage* — (dislocation pits, grain boundary): low-angle grain boundary resulting from an array of dislocations. This angle may vary from a fraction of a second to a minute of arc difference in orientation from one part of the crystal to another. The array of dislocations will appear as rows of pits on a preferentially etched surface.

NOTE 9: Lineage can be induced into the material in crystal growth or in subsequent thermal or epitaxial processes. Lineage will be visible to the unaided eye only after preferential etching.

4.12.8 *macroscratch* — see scratch.

4.12.9 *microscratch* — see scratch.

4.12.10 *microtwin* — see twin.