

SEMI M11-0704

SPECIFICATIONS FOR SILICON EPITAXIAL WAFERS FOR INTEGRATED CIRCUIT (IC) APPLICATIONS

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NOTICE: This Document is no longer supported by the global technical committee. It has been replaced by SEMI M62.

1 Purpose

1.1 This specification defines and provides examples of silicon epitaxial wafer requirements for integrated circuit device manufacture. It is restricted to wafers of diameter 100 mm or greater with epitaxial layer thickness less than or equal to 25 μm . By defining inspection procedures and acceptance criteria, both suppliers and consumers may uniformly define product characteristics and quality requirements.

2 Scope

2.1 This specification covers characteristics of both the substrate (as specified in SEMI M1) and the epitaxial layer, including handling and packaging. The primary standardized properties set forth in this specification relate to physical, electrical, and surface defect parameters.

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2.3 A complete purchase specification requires that additional physical properties be specified along with suitable test methods for their measurements. SEMI M18 may be used for this purpose.

2.4 These specifications are specifically directed to silicon homoepitaxial deposits on homogeneous silicon substrates only, for which more stringent uniformity and surface defect criteria are required than specified in SEMI M2.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M2 — Specification for Silicon Epitaxial Wafers for Discrete Device Applications

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI M44 — Guide for Conversion Factors for Interstitial Oxygen in Silicon

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems using Certified Depositions of Monodisperse Polystyrene Latex Spheres on Unpatterned Semiconductor Wafer Surfaces

SEMI MF95 — Test Method for Thickness of Epitaxial Layers of Silicon on Substrates of the Same Type by Infrared Reflectance

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial Layers Using an Inline Four-Point Probe with the Single Configuration

SEMI MF398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wavelength of the Plasma Resonance Minimum

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

SEMI MF525 — Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF672 — Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe

SEMI MF723 — Practice for Conversion between Resistivity and Dopant Density for Boron-Doped and Phosphorus-Doped Silicon

SEMI MF951 — Test Method for Determination of Radial Interstitial Oxygen Concentration Variation in Silicon

SEMI MF1188 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption with Short Baseline

SEMI MF1239 — Test Methods for Oxygen Precipitation Characterization of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1241 — Terminology of Silicon Technology

SEMI MF1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1393 — Test Method for Determining Net Carrier Density in Silicon Wafers by Miller Feedback Profiler Measurements with a Mercury Probe

SEMI MF1726 — Guide for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

3.2 Other Standards

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes¹

ISO 14644-1 — Cleanrooms and Associated Controlled Environments – Part 1: Classification of Airborne Particulates²

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Many terms relating to silicon technology are defined in SEMI MF1241.

4.2 Descriptions of other epitaxial wafer defects covered in Table 1 are given in SEMI MF154.

4.3 Definitions of selected epi wafer defects, extended to consider automatic surface inspection are given below.

4.3.1 *mound (epi)* — a rounded protrusion on a semiconductor wafer surface, which may have one or more partially developed facets (see Figure 1).

NOTE 1: Scattering event size reported by SSIS will differ from the physical size of the object. The figure captions in the examples highlight this fact. No useful method exists at the present time to quantify this relationship (see Section 7.3.3.3)

4.3.1.1 *Discussion* — Related characteristics include the following:

- *Device Characteristics That May be Affected* — Critical feature dimensions, lithographic equipment focus, gate oxide integrity.

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² International Organization for Standardization, ISO Central Secretariat, 1, ch. de la Voie-Creuse, CP 56, CH-1211 Geneva 20, Switzerland; Telephone: +41.22.749.01.11, Fax: +41.22.733.34.30, <http://www.iso.org>

- *Detection Characteristics Used for Characterization* — Mound height, diameter at 50% height.
- *Discrimination Characteristics Used for Characterization* — Positive height: 10 nm to 100 nm, or approximately 20% of the epi layer thickness; diameter: 0.1 μm to 6 μm ; circular symmetry.
- *Specification Characteristics Used for Wafer Qualification* — Number per wafer, mound height, height to diameter.

4.3.2 *epi stacking fault* — a two dimensional effect that results from a deviation from the normal stacking sequence of atoms in a crystal. [SEMI MF154, SEMI MF1727]

NOTE 2: Discrimination and specification characteristics are given in this section to facilitate equipment development (see Section 7.3.3.3) and are not intended for use in commercial wafer specifications.

4.3.2.1 *Discussion* — Epi stacking faults are typically linked together into squares in the case of $\{100\}$ oriented wafers, and triangles in the case of $\{111\}$ oriented wafers. Most stacking faults are nucleated at the epi layer substrate boundary, though some have been observed being nucleated further into the epi growth process. Faults are aligned along specific crystallographic directions. For $\{100\}$ wafer the sides of the faults are aligned along $\langle 110 \rangle$ directions. The length of a side is typically proportional to the epi layer thickness and related to the crystallographic orientation. In order to minimize the strain around a stacking fault contaminants may diffuse to these defects. Some stacking faults may have an effect on the local growth rate giving the stacking fault a three dimension aspect. This three dimensional aspect changes their light scattering cross section when observed by an SSIS (see Figures 3 through 7). Still more complicated are overlapping stacking faults which scatter even more than a single stacking fault of the same size (see Figure 4). Other types of defects may be composites of stacking faults and polysilicon growth which can also appear larger than a single stacking fault of the same lateral dimensions (see Figures 5 and 6). Related characteristics include the following:

- *Device Characteristics That May be Affected* — Leakage and gate oxide integrity, from crystallographic changes.
- *Detection Characteristics Used for Characterization* — Side length and depth, orientation parallel to a $\langle 110 \rangle$ direction.
- *Discrimination Characteristics Used for Characterization* — Shape, length.
- epi layer thickness: 1 μm to 10 μm . Stacking faults may cluster (see Figure 7) and scatter more than a single stacking fault.
- *Specification Characteristics Used for Wafer Qualification* — Number per wafer. Since certain types of epi stacking faults have no observed impact on device performance while others are killer defects no number can be assigned without a clear identification of the type of epi stacking fault that is involved.



Figure 1
A Mound. Magnification 1000 times using Nomarski Interference Microscopy.
Approximate SSIS scattering event size 0.22 µm.



Figure 2

This is a mound that does not have the sharp edges of an Epitaxial Stacking Fault, but is not as high as a Bump. They are typically sized much smaller in a SSIS than their actual size, but some have facets that scatter enough light to be more easily detected. Some people refer to this feature as a hillock which is a type of mound. The shape can be either circular or square. Magnification 500 times using Nomarski Interference Microscopy. Approximate SSIS event size: 0.15 μm .

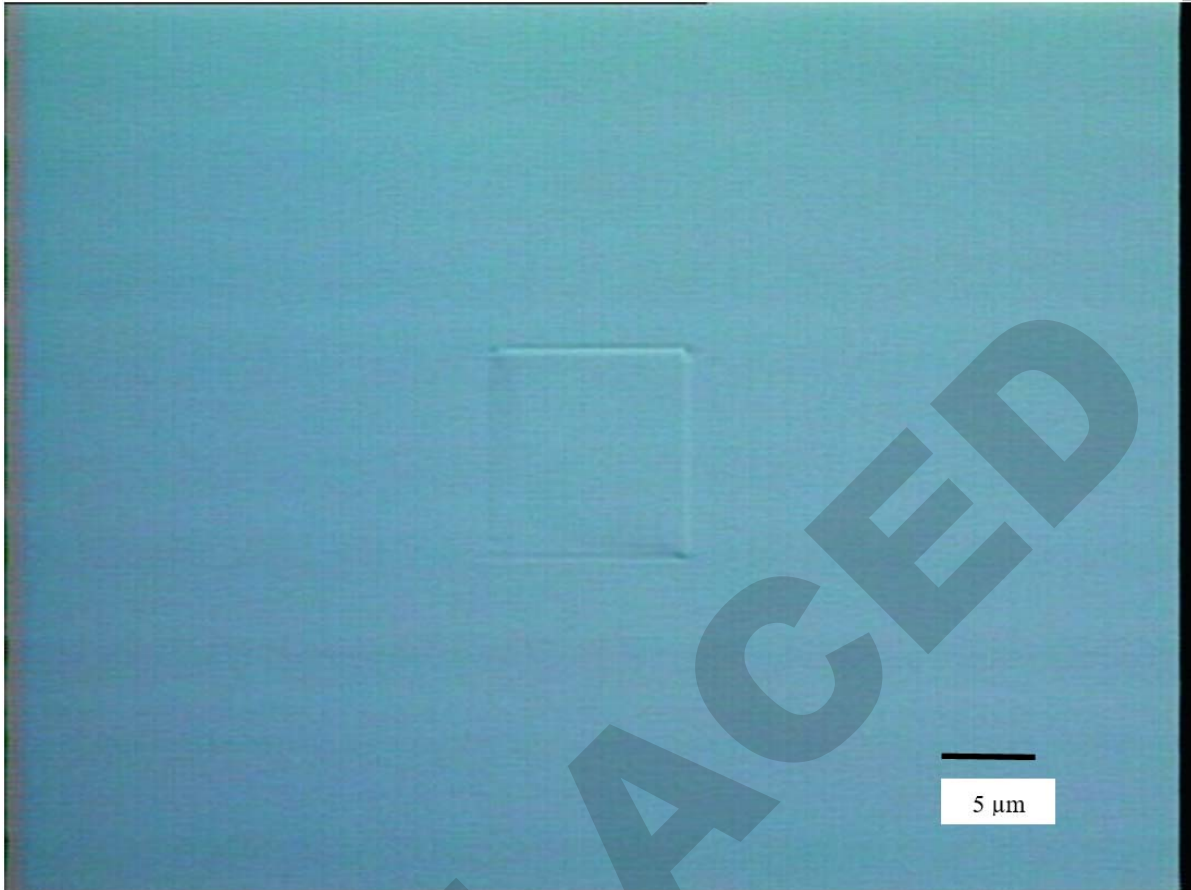


Figure 3

The Epi Stacking Fault (ESF) defect is a grown-in defect with 1 to 4 sides of a square visible. Magnification 1500 times using Nomarski Interference Microscopy. Approximate SSIS event size: 0.165 μm.

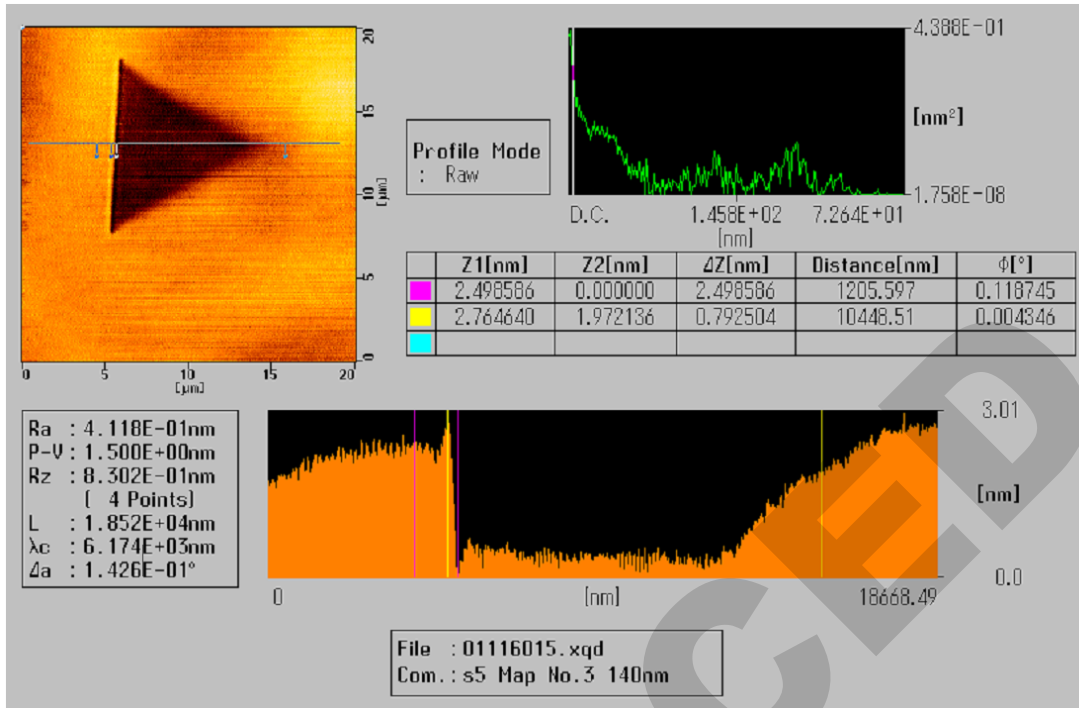


Figure 4
Epitaxial Stacking Fault. Atomic Force Microscope (AFM) Image.
Approximate SSIS scattering event size 0.12 μm.

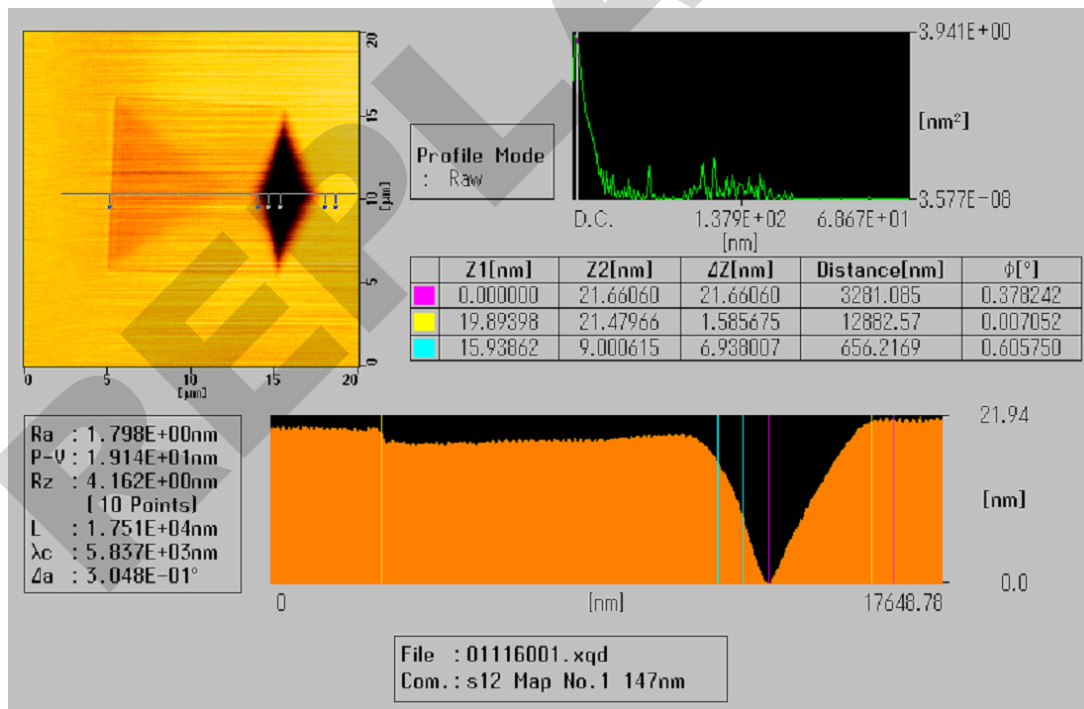


Figure 5
Epitaxial Stacking Fault showing four sides and a deep depression on a side of about 20 nm.
Atomic Force Microscope Image. Approximate SSIS scattering event size, 0.30 μm.

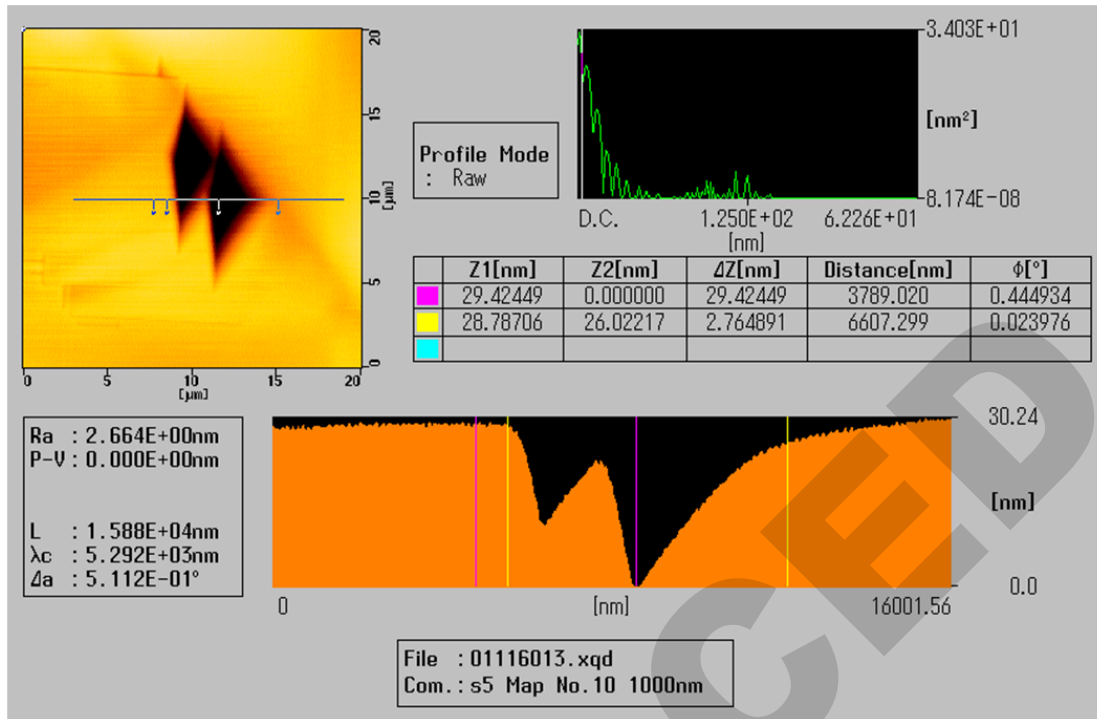


Figure 6
Double Epitaxial Stacking Fault. Atomic Force Microscope image.
Approximate SSIS event scattering size 1.05 μm

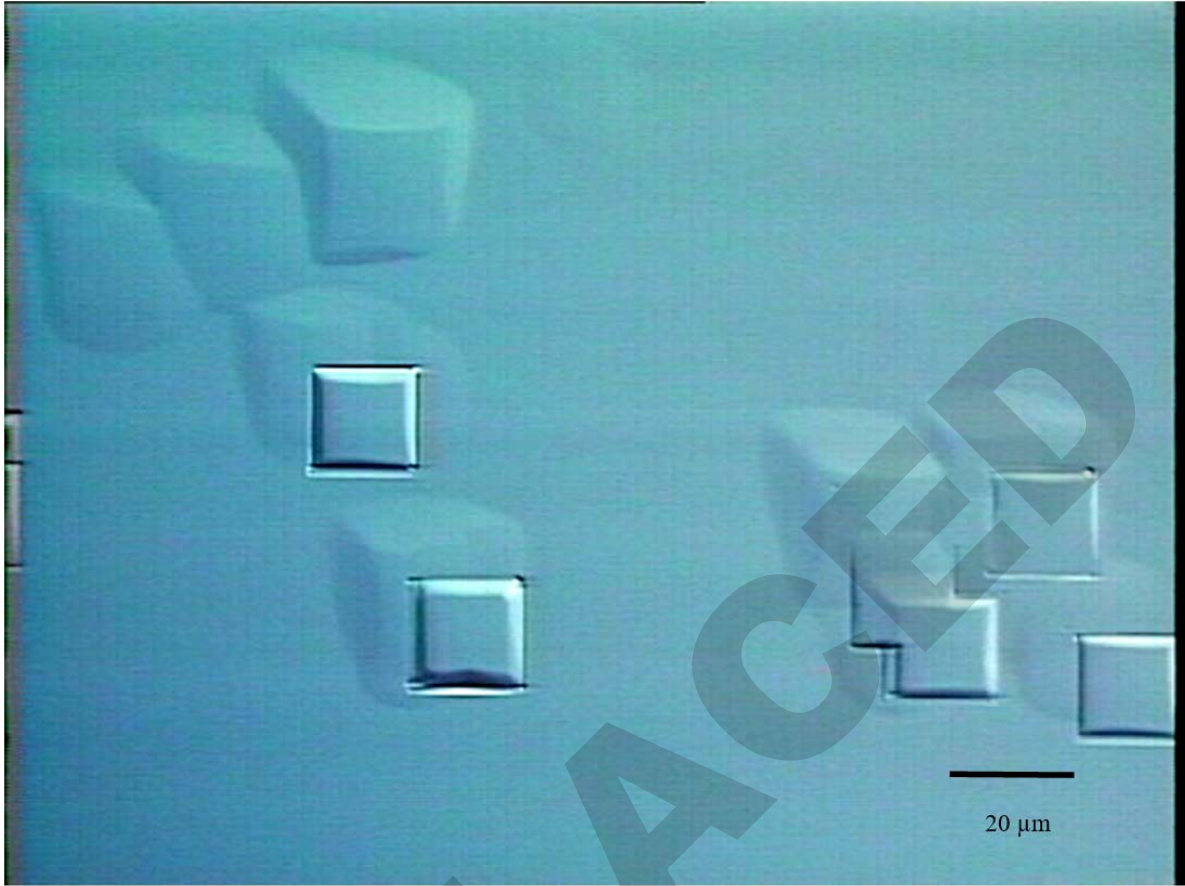


Figure 7

The Epitaxial Stacking Fault Cluster classification is used to define a group of ESFs in close proximity on the wafer surface. The group can either be overlapping or in a line (except when the line appears to be part of a Pre-Epi Scratch). Magnification 500 times using Nomarski Interference Microscopy.
Approximate SSIS event size, 0.20 μm

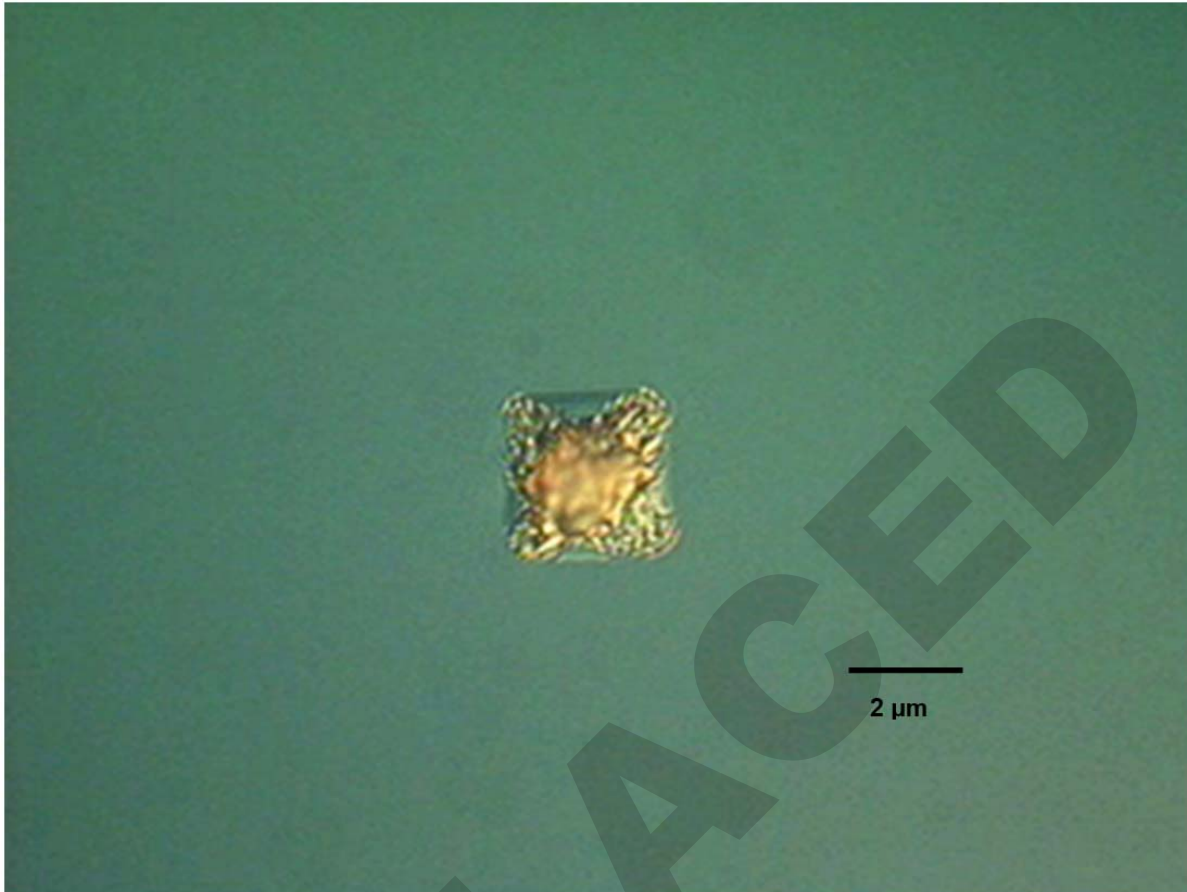


Figure 8
Composite Defect of polysilicon growth and stacking faults. Magnification 1000 times by Nomarski
Interference Microscopy. Approximate SSIS image event size >>1.0 μm



Figure 9

The Compound ESF defect is an epi stacking fault that has a broken surface, but maintains the square shape of an ESF. It typically scatters more light than a normal ESF because of the extra facets, so it is sized larger in a SSIS. Magnification 500 times using Nomarski Interference Microscopy.

Approximate SSIS event size: 280 μm