

SEMI M15-0298

POLISHED WAFER DEFECT LIMITS TABLE FOR SEMI-INSULATING GALLIUM ARSENIDE WAFERS

This Standard was technically approved by the Silicon Materials Global Technical Committee.

NOTICE: This Document was completely rewritten in 1998.

1 Purpose

1.1 This Standard defines the maximum number of defects, by type, that an acceptable polished Semi-Insulating Gallium Arsenide (GaAs) wafer may exhibit.

2 Scope

2.1 This Standard, established separately from SEMI M15, in accordance with the latest requirements for the material in advanced applications, covers polished semi-insulating GaAs wafers. The defect limits table can also be applied to conducting GaAs wafers, except for the specification of light point defects (LPD) mentioned hereinafter. 'Polished' shall refer to those wafers which have a specular chemical or chemical/mechanical finish applied to one side of the wafer, with the backside being as cut and etched, lapped and etched, ground and etched, or polished. The definition of defects is covered in ASTM F523 and ASTM F154.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 ASTM® Standards¹

ASTM F154 — Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

ASTM F523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

Table 1 Polished Wafer Defect Limits

Item #	Characteristics — Front Surface	Maximum Defects Limits Prime Wafer	Maximum Defects Limits Test Wafer	Notes
1	Scratches			
	Macroscratches	None		#1
	Maximum Number	----	3	
	Maximum Length	----	Radius/2	
	Microscratches	None	Not Specified	#1, #2
2	Pits			#1, #2
	2 in. Diameter Slices	None	5	
	3 in. Diameter Slices	None	15	
	4 in. Diameter Slices	None	30	
3	Haze	None	None	#1, #2
4	Cavity/Voids	None	None	#1
5	Contamination	None	None	#1, #2

¹ ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA; Telephone: +1.610.832.9585, Fax: +1.610.832.9555, <http://www.astm.org>. ASTM trademark is owned by ASTM International.

Item #	Characteristics — Front Surface	Maximum Defects Limits Prime Wafer	Maximum Defects Limits Test Wafer	Notes
6	Light Point Defects $\geq \phi$ 2.0 μm			
	2 in. Diameter Slices	10	20	#2, #3
	3 in. Diameter Slices	15	30	#2, #3
	4 in. Diameter Slices	20	40	#2, #3
	Light Point Defects $\geq \phi$ 3.0 μm			
	2 in. Diameter Slices	50	100	#2, #3
	3 in. Diameter Slices	100	200	#2, #3
18				
	4 in. Diameter Slices	200	400	#2, #3
7	Chips ($\geq 0.5 \text{ mm} \times 0.3 \text{ mm}$)	None	None	#1
8	Cracks	None	None	#1
9	Dimples	None	None	#1, #2
10	Gallium Inclusions/Precipitates	None	None	#1, #2
11	Orange Peel	None	None	#1, #2
12	Saw Marks	None	None	#1
13	Striations	None	None	#1, #2
14	Twins	None	None	#1, #2
15	Stain	None	None	#2, #4
16	Saw Marks	None	None	#1, #5
17	Chips ($\geq 0.5 \text{ mm} \times 0.3 \text{ mm}$)	None	None	#1
18	Cracks	None	None	#1
19	Listed Defects #10, 14	None	None	#1, #2
20	Listed Defects #1, 2, 6			#6

#1 These defect limits are meant to apply only to those characteristics which can be seen with the unaided eye under high-intensity illumination according to ASTM F523. Limits for other defects listed and defined in this section which require the aid of a microscope, preferential etching, or other apparatus must be agreed upon between supplier and user.

#2 *Peripheral Edge Allowance* — The outer edge exclusion for observation shall be determined from the following table:

Diameter	Outer Edge Exclusion for Observation
2 in.	2 mm
3 in.	3 mm
4 in.	3 mm

#3 LPD shall be counted by measuring equipment designed for detecting laser light scatter. Selection of the measuring equipment and the requirement for the precision are to be agreed upon between supplier and user.

#4 *Back Surface Stain* — An area of undercutting, texturing, or oxidation, common in waxless polished wafers.

#5 The depth of allowed saw marks is to be no greater than 5 μm . The measuring method is to be agreed upon between supplier and user.

#6 *Item #20* — To be agreed upon between supplier and user.