

SEMI M17-0998

SPECIFICATION FOR A UNIVERSAL WAFER GRID

1 Scope

1.1 This document defines a grid pattern which is useful for quantifying surface defects on a nominally circular semiconductor wafer. The grid is defined such that it contains 1000 elements of approximately equal area. Each grid element thus contains 0.1 percent of the total quality area of the surface being inspected. Defects which are non-uniformly distributed (for example, slip) can be quantified in terms of the percent defective (or percent useful) area on the wafer surface.

1.2 The quantification of defective area is done by overlaying a transparency of the grid onto a map of wafer defects or by mapping observed defects onto the grid. The number of grid elements which contain defects is counted. The element count divided by 10 corresponds to the percent of defective area. This grid could also be superimposed onto a CRT display, photograph, or computer generated map, where applicable. In use, grid pattern diameters must be scaled to the size of the map or image of the wafer to be overlaid.

1.3 The grid described is referenced to the center of the wafer. A concept of a "Fixed Quality Area" is used, based on nominal wafer diameter, such as is specified in SEMI M1.

1.4 Maximum allowable slip and other non-uniformly distributed defects on epitaxial layers are specified in SEMI M2 and SEMI M11, and are observed in accordance with ASTM Test Methods F 80 or F 523.

2 Applicable Documents

2.1 SEMI Standards

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M2 — Specifications for Silicon Epitaxial Wafers

SEMI M11 — Specifications for Silicon Epitaxial Wafers for Advanced Applications

2.2 ASTM Standards¹

F 47 — Test Method for Crystallographic Perfection of Silicon by Preferential Etch Techniques

F 80 — Test Method for Crystallographic Perfection of Epitaxial Deposits of Silicon by Etching Techniques

F 154 — Standard Practice and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

F 523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

F 1241 — Terminology for Silicon Technology

3 Terminology

3.1 Selected definitions (for information only) are listed in the glossary, Definitions for Semiconductor Materials, at the end of this volume.

3.2 Definitions for many surface defects are given in ASTM Terminology F 1241. Additional information is provided in ASTM Test Method F 47 and ASTM Practices F 154.

4 Grid Element Layout

4.1 Grid Element Scheme

4.1.1 Two types of grids are defined: one for wafers without a primary flat (for example, wafers where the primary fiducial is a notch), and one for wafers with a primary flat. The grid is divided by 18 concentric circles containing radial divisions which are assigned according to the diameter of each circle (see Table 1). The relative diameters of the concentric circles are established by the areas of each annulus. To find the actual diameter of any circle, multiply the relative diameter by the outer diameter of the grid.

4.1.2 The outer diameter of the grid is chosen to be the size appropriate for a particular application. This diameter would normally be chosen to be the nominal diameter of the fixed quality area to allow for such things as an edge exclusion, tolerance variations in the wafer diameter, and edge rounding. Table 2 shows (as an example) the circle diameters for a series of grids which have a fixed quality area radius 3 mm smaller than the nominal radius of selected wafers specified in SEMI M1.

4.1.3 Identification of each grid element is done by referring to a circle number and a division number on that circle. Circles are numbered from the center out, with the center circle being number 01 and the outermost circle being number 18. The divisions are numbered starting with the first division counterclockwise from the horizontal line which starts

¹ American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959 (All cited standards except for E 122 may be found in Volume 10.05 of the Annual Book of ASTM Standards; E 122 may be found in Volume 14.02.)

at the center of the grid and extends to the right, when the primary fiducial (flat or notch) is placed at the bottom of the grid. Divisions are progressively numbered counterclockwise from 01 to n, where n equals the total number of divisions on the circle. An element's address is given by two sets of numbers separated by a comma: circle (0 –18), division (01–n). Elements 18, 01 and 18, 100 are identified in Figure 1.

NOTE In this sense, the fixed quality area used by the Universal Wafer Grid deviates somewhat from the formal definition in SEMI M1 which embodies an edge exclusion of constant width around the entire periphery of the wafer including the region of the secondary flat.

4.2 *Wafers without a Primary Flat*

4.2.1 The grid elements for wafers without a primary flat are illustrated in Figure 1. This pattern is generated by making concentric circles with relative diameters and radial divisions as specified in Table 1. In this table the circle number is given in the leftmost column. The number of divisions and the included angle of each division in the circle are given in the second and third columns. The total number of divisions (from the center outward) is given in the fourth column. The included area ratio, given in the fifth column, is the total number of divisions included within a circle divided by 1000, the total number of divisions in the grid. The relative diameter, given in the rightmost column, is the square root of the included area ratio.

4.3 *Wafers with a Primary Flat*

4.3.1 For wafers with a primary flat, a standard included angle of 43.2° is used for all wafer sizes. This angle was chosen because it lies between the maximum and minimum included angles of the primary flats specified in SEMI M1 for 100 mm, 125 mm, 150 mm, and 200 mm diameter wafers. In addition, if a fixed quality area of radius 3 mm less than the nominal wafer radius is used, the grid will not in any case extend beyond the edge of the wafer in the region of the primary flat.

4.3.2 This flat is propagated into the wafer as illustrated in Figure 2. The diameter of each circle is the same as for wafers without a primary flat. The flat is propagated vertically downward (starting with circle number 3) by the intersection of the circle with a horizontal chord which subtends 43.2° .

4.3.3 The areas of the grid elements within the propagated flat region are slightly smaller than the areas of the regular grid elements. This difference is ignored when counting grid elements for wafers with a primary flat. All grid elements are assumed to be 0.001 of the total fixed quality area.

4.4 *Secondary Flats*

4.4.1 The grid ignores secondary flats. These are shallow enough that the outer circle does not extend beyond the wafer edge if a fixed quality area of radius 3 mm less than the nominal wafer radius is used.