SEMI M17-1110 (Reapproved 1121)
GUIDE FOR A UNIVERSAL WAFER GRID

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NOTICE: Paragraphs entitled 'NOTE:' are not an official part of this Standard or Safety Guideline and are not intended to modify or supersede the official Standard or Safety Guideline. These have been supplied by the global technical committee to enhance the usage of the Standard or Safety Guideline.

1 Purpose

1.1 Maximum allowable slip and other non-uniformly distributed defects are frequently specified when procuring polished and epitaxial silicon wafers. SEMI M62 specifies a maximum allowable fraction of the epitaxial wafer surface area that can contain slip.

1.2 This Guide provides a design for and guidance for use of a wafer grid that facilitates the determination of the fraction of the wafer surface area covered by observed defects.

2 Scope

2.1 This Guide defines a grid pattern that is useful for quantifying surface defects on a nominally circular semiconductor wafer. The grid is defined such that it contains 1000 elements of approximately equal area. Each grid element thus contains 0.1% of the total quality area of the surface being inspected. Defects that are non-uniformly distributed (e.g., slip) can be quantified in terms of the percent defective (or percent useful) area on the wafer surface.

2.2 The grid described is referenced to the center of the wafer. A concept of a 'fixed quality area' is used, based on nominal wafer diameter, such as is specified in SEMI M1.

2.3 Methods for observing these defects on silicon wafer surfaces are outside the scope of this Guide. Such methods may be found in SEMI MF1725, SEMI MF1726, JIS H 0609, and DIN 50434.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards and Safety Guidelines*

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M59 — Terminology for Silicon Technology

SEMI M62 — Specification for Silicon Epitaxial Wafers

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF1725 — Practice for Analysis of Crystallographic Perfection of Silicon Ingots

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1809 — Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon

3.2 *DIN Standards*[1]

DIN 50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

[1] Deutsches Institut für Normung e.V., Available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany; http://www.din.de

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3.3 *JIS Standards*[2]

JIS H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Acronyms, terms, and symbols related to silicon technology, including those used in this Guide, are listed and defined in SEMI M59. Additional information and illustrations of various surface defects are provided in SEMI MF154, SEMI MF1809, and JIS H 0609.

5 Grid Element Layout

5.1 *Grid Element Scheme*

5.1.1 Two types of grids are defined: one for wafers without a primary flat (e.g., wafers where the primary fiducial is a notch), and one for wafers with a primary flat. The grid is divided by 18 concentric circles containing radial divisions which are assigned according to the diameter of each circle (see Table 1). The relative diameters of the concentric circles are established by the areas of each annulus. To find the actual diameter of any circle, multiply the relative diameter by the outer diameter of the grid.

5.1.2 The outer diameter of the grid is chosen to be the size appropriate for a particular application. This diameter would normally be chosen to be the nominal diameter of the fixed quality area to allow for such things as an edge exclusion, tolerance variations in the wafer diameter, and edge rounding. Table 2 shows the circle diameters for a series of grids which have a fixed quality area radius 3 or 4 mm smaller than the nominal radius of selected wafers specified in SEMI M1.

5.1.3 Identification of each grid element is done by referring to a circle number and a division number on that circle. Circles are numbered from the center out, with the center circle being number 01 and the outermost circle being number 18. The divisions are numbered starting with the first division counterclockwise from the horizontal line which starts at the center of the grid and extends to the right, when the primary fiducial (flat or notch) is placed at the bottom of the grid. Divisions are progressively numbered counterclockwise from 01 to n, where n equals the total number of divisions on the circle. An element's address is given by two sets of numbers separated by a comma: circle (0–18), division (01–n). Elements 18, 01 and 18, 100 are identified in Figure 1.

5.2 *Wafers Without a Primary Flat*

5.2.1 The grid elements for wafers without a primary flat are illustrated in Figure 1. This pattern is generated by making concentric circles with relative diameters and radial divisions as specified in Table 1. In this table the circle number is given in the leftmost column. The number of divisions and the included angle of each division in the circle are given in the second and third columns. The total number of divisions (from the center outward) is given in the fourth column. The included area ratio, given in the fifth column, is the total number of divisions included within a circle divided by 1000, the total number of divisions in the grid. The relative diameter, given in the rightmost column, is the square root of the included area ratio.

5.3 *Wafers With a Primary Flat*

5.3.1 For wafers with a primary flat, a standard included angle of 43.2° is used for all wafer sizes. This angle was chosen because it lies between the maximum and minimum included angles of the primary flats specified in SEMI M1 for 100 mm, 125 mm, 150 mm, and 200 mm diameter wafers. In addition, if a fixed quality area of radius 3 mm less than the nominal wafer radius (or smaller) is used, the grid will not in any case extend beyond the edge of the wafer in the region of the primary flat.

5.3.2 This flat is propagated into the wafer as illustrated in Figure 2. The diameter of each circle is the same as for wafers without a primary flat. The flat is propagated vertically downward (starting with circle number 3) by the intersection of the circle with a horizontal chord which subtends 43.2°.

[2] Japanese Standards Association, 4-1-24 Akasaka, Minato-ku, Tokyo 107-8440, Japan; Telephone: +81.3.3583.8005, Fax: +81.3.3586.2014, http://www.jsa.or.jp

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