

SEMI M18-0304

FORMAT FOR SILICON WAFER SPECIFICATION FORM FOR ORDER ENTRY

This format was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on December 4, 2003 and the Japanese Regional Standards Committee on January 9, 2004. Initially available at www.semi.org February 2004; to be published March 2004. Originally published in 1990; last published July 2002.

1 Purpose

1.1 This format provides a standard form for specifying several classifications of silicon wafers, as follows:

1.1.1 Polished Silicon Wafers.

1.1.2 Epitaxial Silicon Wafers.

1.1.3 Epitaxial Silicon Wafers with Buried Layer.

1.1.4 Annealed Silicon Wafer.

1.1.5 SOI Wafers for CMOS Applications.

1.2 This format also lists the Electronic Data Interchange (EDI) codes used in SEMI T6 to identify the type of data being reported in the EDI message.

2 Scope

2.1 The form is designed to be used in conjunction with other SEMI specifications where details of the dimensional, physical, electrical, and chemical properties are defined or specified. However, the form includes many items that are not currently included in the SEMI specifications. Also, many items are not now commonly specified, but may find increased importance in the future. The intention is to provide for flexibility and expansion of the technology.

2.2 This format provides for specifying and ordering silicon wafers with varying levels of complexity. The minimum level of completeness is shown in each case, with additional options included to allow for customization of the wafer to the specific processing requirements of the user. If a particular item is not of interest, no entry is required. The only required entries are those marked as such for the purpose of minimal specification (diameter, orientation, dopant, resistivity, etc.).

2.3 Values for many items are listed either in the polished silicon wafer standards in SEMI M1 or in the defect limits tables in SEMI M1, SEMI M2, or SEMI M11. If these standard specifications are sufficient for defining the wafers, only a single entry is required in each section of the form.

2.4 This format also lists the codes required by SEMI T6 to identify the parameter being reported in the EDI message. Where necessary, secondary characteristics or identifier codes are listed within a generalized characteristic.

2.5 For referee purposes, U.S. Customary units shall be used for wafers of 2- and 3-inch diameters, and SI (System International, commonly called metric) units for 100 mm and larger diameter wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 SEMI Standards

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M2 — Specifications for Silicon Epitaxial Wafers for Discrete Device Applications

SEMI M11 — Specifications for Silicon Epitaxial Wafers for Integrated Circuit (IC) Applications

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specifications for Alphanumeric Marking of Silicon Wafers

SEMI M20 — Specification for Establishing a Wafer Coordinate System

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M47 — Specification for Silicon-on-insulator (SOI) Wafers for CMOS LSI Applications

SEMI MF26 — Standard Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF28 — Test Method for Minority-Carrier Lifetime in Bulk Germanium and Silicon by Measurement of Photoconductive Decay

SEMI MF42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF81 — Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Probe Array

SEMI MF95 — Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Standard Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-implanted Layers Using an In-Line Four-Point Probe

SEMI MF391 — Standard Test Methods for Minority-Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

SEMI MF398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wave Number or Wavelength of the Plasma Resonance Minimum.

SEMI MF523 — Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surface

SEMI MF525 — Test Method Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF533 — Standard Test Method for Thickness and Thickness of Variation of Silicon Wafers

SEMI MF534 — Standard Test Method for Bow of Silicon Wafers

SEMI MF657 — Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Material

SEMI MF672 — Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe

SEMI MF673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

SEMI MF723 — Practice for Conversion Between Resistivity and Dopant Density for Boron-Doped, Phosphorus-Doped, and Arsenic-Doped Silicon.

SEMI MF847 — Standard Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF951 — Test Method for Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF978 — Standard Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

SEMI MF1049 — Standard Practice for Shallow Pit Detection on Silicon Wafers

SEMI MF1152 — Standard Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1188 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

SEMI MF1239 — Standard Test Methods for Oxygen Precipitation Characterization of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1241 — Standard Terminology of Silicon Technology

SEMI MF1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectroscopy

SEMI MF1388 — Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of Metal-Oxide-Silicon (MOS) Capacitors

SEMI MF1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1391 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by

Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1393 — Test Method for Determining Net Carrier Density Profile in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1451 — Standard Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1526 — Standard Test Method for Measuring Surface Metal Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy

SEMI MF1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1528 — Test Method for Measuring Boron Contamination in Heavily Doped N-Type Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1535 — Standard Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

SEMI MF1617 — Standard Test Method for Measuring Surface Sodium, Aluminum, and Potassium on Silicon and EPI Substrates by Secondary Ion Mass Spectroscopy

SEMI MF1619 — Standard Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle

SEMI MF1620 — Standard Practice for Calibrating a Scanning Surface Inspection System Using Monodisperse Polystyrene Latex Spheres Deposited on Polished or Epitaxial Surfaces

SEMI MF1621 — Standard Practice for Determining Positional Accuracy Capabilities of a Scanning Surface Inspection System

SEMI MF1725 — Standard Guide for Analysis of Crystallographic Perfection of Silicon Ingots

SEMI MF1726 — Standard Guide for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon

SEMI MF1810 — Test Method for Counting Preferentially Etched or Decorated Structural Defects on Silicon Wafers

SEMI MF1982 — Test Method for Analyzing Organic Contamination on Silicon Wafers Surfaces by Thermal Desorption Gas Chromatography

SEMI T1 — Specification for Back Surface Bar Code Marking of Silicon Wafers

SEMI T2 — Specification for Marking of Wafers with a Two-Dimensional Matrix Code Symbol

SEMI T6 — Procedure and Format for Reporting of Test Results by Electronic Data Interchange (EDI)

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 ANSI Standard¹

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 ASTM Standards²

D 523 — Standard Test Method for Specular Gloss

E 122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

F 416 — Standard Test Method for Detection of Oxidation Induced Defects in Polished Silicon Wafers

F 419 — Test Method for Determining Carrier Density in Silicon Epitaxial Layers by Capacitance-Voltage Measurement on Fabricated Junction of Schottky Diodes

F 613 — Standard Test Method for Measuring Diameter of Semiconductor Wafers

3.4 DIN Standards³

NOTE 1: DIN Standards are available in both German and English editions. ASTM equivalents are given in square brackets following the title.

50431 — Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Colinear Four-Probe Array

¹ American National Standards Institute, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023 Website: www.ansi.org

² American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

³ Available from Deutsches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, website: www.din.de

50432 — Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hot-Probe

50433/1 — Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction

50433/2 — Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure

50433/3 — Determination of the Orientation of Single Crystals by Means of Laue Back Scattering

50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

50435 — Determination of the Radial Resistivity Variation of Silicon or Germanium Slices by Means of a Four-Point-DC-Probe

50436 — Measurement of Metallurgical Thickness of Epitaxial Layers of Silicon by the Stacking Fault Method

50437 — Measuring the Thickness of Silicon Epitaxial Layers of Silicon by Infrared Interference Method [F95]

50438/1 — Determination of Impurity Content in Silicon by Infrared Absorption: Oxygen

50438/2 — Determination of Impurity Content in Silicon by Infrared Absorption: Carbon

50439 — Determination of the Dopant Concentration Profile of Single Crystalline Semiconductor Material by Means of the Capacitance-Voltage Method and Mercury Contact [F 1392, F 1393]

50438/3 — Determination of Impurity Content in Silicon by Infrared Absorption: Boron and Phosphorus

50440/1 — Measurement of Recombination Carrier Lifetime in Silicon Single Crystals by Means of Photoconductive Decay Method; Measurement on Bar-Shaped Test Samples [F28]

50441/1 — Determination of the Geometric Dimensions of Semiconductor Slices: Measurement of Thickness

50441/2 — Determination of the Geometric Dimensions of Semiconductor Slices: Testing of Edge Rounding

50441/3 — Measurement of the Geometric Dimensions of Semiconductor Slices; Determination of Flatness Deviation of Polished Slices by Means of Multiple Beam Interference

50441/4 — Determination of the Geometrical Dimensions of Semiconductor Slices: Diameter and Flat Depth of Slices

50443/1 — Recognition of Defects and Inhomogeneities in Semiconductor Single Crystals by X-Ray Topography: Silicon

50444 — Conversion Between Resistivity and Dopant Density; Silicon [F723 (phosphorous and boron only)]

50445 — Contactless Determination of the Electrical Resistivity of Semiconductor Wafers with the Eddy Current Method

50446 — Determination of Defect Types and Defect Densities of Silicon Epitaxial Wafers [no direct ASTM equivalent, compare F 1726 and associated standards]

3.5 ISO Standards⁴

ISO 4287/1 — Surface Roughness – Terminology – Part 1: Surface and its Parameters

ISO 14644/1-7 — Clean Room and Associated Controlled Environments

3.6 JEITA (formerly JEIDA) Standards⁵

43 — Terminology of Silicon Wafer Flatness

53 — Test Method for Recombination Lifetime in Silicon Wafers by Measurement of Photoconductivity Decay by Microwave Reflectance

56 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

61 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

EM-3602 — Determining the Orientation of a Semiconductor Silicon Single Crystal

EM-3501 — Standard Specification for Dimensional Properties of Silicon Wafers with Specular Surface

EM-3505 — Height calibration in 1nm order for AFM

3.7 JIS Standards⁶

NOTE 2: ASTM equivalents are given in square brackets following the title.

H 0602 — Testing Method of Resistivity for Silicon Crystals and Silicon Wafers with Four-Point Probe

⁴ International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembe, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch

⁵ Japanese Electronic and Information Technology Industries Association, Tokyo Chamber of Commerce and Industry Bldg. 2-2, Marunouchi 3-chome, Chiyoda-ku, Tokyo 100-0005, Japan. Website: www.jeita.or.jp

⁶ Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp

H 0604 — Measurement of Minority Carrier Life Time in Silicon by Photoconductive Decay Method [F 28]

H 0607 — Testing Methods for Conductivity Type of Semiconductor Materials

H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

H 0611 — Methods of Measurement of Thickness, Taper, and Bow of Silicon Wafers

H 0612 — Testing Method of Resistivity for Single Crystal Silicon Wafers (with Four Point Probe) [F 84]

H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

Z 8741 — Method of Measurement for Specular Glossiness

3.8 Other Standard⁷

ANSI/ASME B46.1 — Surface Texture (Surface Roughness, Waviness, and Lay)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 The items listed in the form are referenced and defined in various documents. A reference for most items in Parts 2 and 3 of the form is listed in Table 1. The entries in the table are keyed to the form by item number. Because terms related to epitaxial wafers with buried layer are defined in this standard and because no standardized test methods for the buried layer parameters exist, Table 1 does not include line items from Part 4 of the form.

4.2 General term used in this standard:

4.2.1 *required (req. or req'd)* — when applied to a parameter listed in the order form, a user-supplied value is necessary to minimally define the material for manufacture.

4.3 Terms related to epitaxial wafers with buried layers:

4.3.1 *buried layer* — a diffused region in a substrate that is, or is intended to be, covered with an epitaxial layer.

4.3.2 *alignment precision* — pattern displacement in first mask photolithography process.

NOTE 3: Alignment precision is specified by maximum values of X and Y, the displacement of the center of the pattern from a reference position defined in the wafer

specification in terms of the wafer coordinate system defined in SEMI M20, and the maximum value of θ , the angle between the x-axis of the pattern and the primary orientation flat (see Figure 1).

4.3.3 *pattern distortion ratio* — absolute magnitude of the quotient of the (1) difference between the width of the pattern on the substrate and the width of the pattern on the top surface of the epitaxial layer and (2) the thickness of the epitaxial layer.

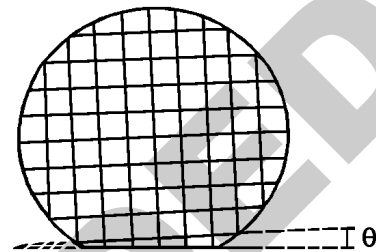


Figure 2
First Mask Showing Angular Displacement θ

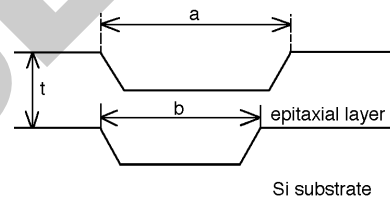


Figure 3
Cross-Section View of Epitaxial Layer Showing the Pattern Widths, a , at the Epi Surface, and b , at the Layer-Substrate Interface

4.3.4 *pattern shift ratio* — lateral distance between the center point of the pattern on the surface of the substrate and the center point of the pattern on the surface of the epitaxial layer divided by the epitaxial layer thickness.

NOTE 4: Pattern shift ratio, d/t (see Figure 4), is specified in terms of a nominal value, X , and a tolerance, $\pm Y$, both of which are dimensionless because both d and t are in μm .

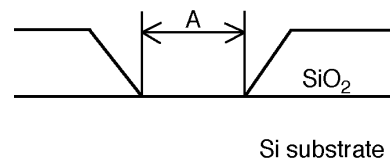


Figure 4
Schematic Diagram Showing Line Width, A , of Pattern on Substrate Wafer

⁷ The American Society of Mechanical Engineers, United Engineering Center, 345 E. 47th St., New York, NY 10017.

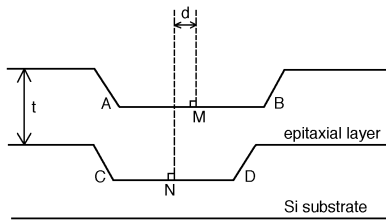


Figure 5
Cross-Section View of Epitaxial Wafer Showing the Pattern Shift, d . Not to scale: $AM = MB$ and $CN = ND$

4.3.5 *pattern step height* — difference in vertical position of the diffused (buried layer) surface and the original substrate surface, after removal of oxide.

NOTE 5: Pattern step height, A , is specified as a nominal value, X , and a tolerance $\pm Y$, both in nm. See Figure 5.

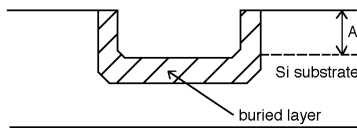


Figure 6
Cross-Sectional View of Epitaxial Substrate After Oxide Removal but Before Deposition of the Epitaxial Layer Showing the Pattern Step Height, A

4.4 Terms Related to Annealed Wafers

4.4.1 *annealed wafer* — wafer that has defects (COP) free zone near the surface produced by high temperature annealing.

4.4.1.1 *hydrogen annealed wafer* — annealed wafer produced under hydrogen atmosphere.

4.4.1.2 *argon annealed wafer* — annealed wafer produced under argon atmosphere.

4.5 Terms Related to SOI Wafers

4.5.1 *SOI wafer* — wafer that has a buried oxide layer (BOX).

4.5.1.1 *SIMOX wafer* — SOI wafer made by oxygen implantation and high temperature annealing technology.

4.5.1.2 *Bonded wafer* — SOI wafer made by bonding two silicon wafers with an insulating layer between them. The insulating layer is typically grown oxide.

5 Use of the Form

5.1 Different parts of the specification form are used for ordering different types of silicon wafers:

5.1.1 For polished wafers, complete Parts 1 and 2.

5.1.2 For epitaxial wafers, complete Parts 1, 2, and 3.

5.1.3 For epitaxial wafers with buried layer, complete Parts 1, 2, 3, and 4.

5.1.4 For annealed wafers, complete parts 1, 2, and 5.

5.1.5 For SOI wafers, complete Parts 1, 2, and 6. If necessary, complete Parts 3, 4, or 5.

5.2 In all cases, items listed as required must have a value or choice indicated to minimally specify the material.

5.3 Certain required dimensional items may be specified as a group according to the standard values presented in the applicable SEMI specification, or they may be specified individually.

5.4 Visual inspection criteria may be specified as a group according to the standard values listed in the applicable SEMI specification, or they may be specified individually.

5.5 For either dimensional values or visual inspection criteria, the appropriate SEMI specification may be marked and an optional line item (or items) marked as well. In this case, the value marked on each individual line item takes precedence over the standard value.

5.6 If the suggested form included in this format is not reproduced and used as a fill-out form, the items and responses must be adequately identified so that the information and requirements are clear to all parties.

6 Test Methods

6.1 Measurements shall be made or certifiable to the ASTM, JEITA, JIS, or DIN standard test method as cited in Table 1.

6.2 When standard test methods from different geographic regions are available, the default method shall be the method in common usage for the region of the purchaser of the wafer.

6.3 If several different standard test methods for an item are commonly used within a region, a specific entry must be made to identify which method of test is applicable.

6.4 If no standard test method for an item is available, the test procedure must be specified.

7 Testing Level and Certification

7.1 Material ordered using this format shall be tested and/or certified to the limits set forth in the individual criteria.

7.2 The actual testing level, whether the test is performed on all wafers, a sample of the wafers, special test pieces representing all portions of the material, or a sample of the test pieces, may be specified using this format.

7.3 In some cases, the material may be certified as “capable of meeting” certain requirements. In this context, the supplier is not required to perform the tests outlined in this format. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

8 EDI Codes and Sub-Parameter Codes

8.1 The EDI Codes for each parameter are listed in the following Table. Where necessary for clarity, additional sub-parameters are listed. These sub-parameter identify a specific measurement technique or method to be used.

8.2 If additional codes are required in the future, they will be added to the table, beginning with the next available EDI code identifier. This will allow the table to be rearranged for clarity while maintaining unique and consistent EDI codes for existing parameters. Table 2 provides a numerically sorted list of the EDI Codes.

SEMI Silicon Wafer Specification Form For Order Entry (Page 1)

Part 1 General Information

ITEMS	INFORMATION	Date:
Customer Name		
Purchase Order Number		
Line Number		
Item Number		
General Specification Number		
Revision Level		
Part Number/Revision		

Part 2 Polished Wafer

CUSTOMER:			PART NUMBER:		REVISION		DATE:						
REQUIRED	ITEM		SPECIFICATION			TESTING LEVEL				EDI		Sub	
						WAFER		TEST PIECE		Code		Param	
						100%	SAMP LE	100%	SAMP LE	ID		ID	
1. GENERAL CHARACTERISTICS													
◆	1.1	Growth Method	[]Cz []FZ []MCz								100001		
◆	1.2	Crystal Orientation	[](100) [](111) [] ()								100002		
◆	1.3	Conductivity Type	[]p []n								100003		
◆	1.4	Dopant	[]B []Phos []Sb []As []NTD								100004		
	1.5	Nominal Edge Exclusion Distance for Fixed Quality Area	Applies to Sections 6.10–6.14; 11 []3 mm; []5 mm; []Other__mm Applies to Sections 7, 8, 12, 13 []3 mm; []5 mm; []Other__mm (except edge defects)								100005		
2. ELECTRICAL CHARACTERISTICS													
◆	2.1	Resistivity	Nominal [] ± Tolerance [] Ω–cm								100006		
		Measurement Position	[]Center Point; []Other:										
		Measurement Method	[]SEMI MF81; []SEMI MF673; []JIS H 612; []JEIDA 18; []DIN 50431										
	2.2	Radial Resistivity Variation (RRG)	Not greater than []%								100007		

		Measurement Position	SEMI MF81 Fig. 1 - []A, []B, []C, []D; [] JEIDA 18; []DIN 50435						
		Calculation Method	[]SEMI MF81; []JEIDA 18; []DIN 50435; []Other:						
	2.3	Resistivity Striations	Not greater than []%					100008	
	2.4	Minority Carrier Lifetime	Greater than [] μ s					100009	
		Test Method	SEMI MF28 []A, []B; SEMI MF391 []A, []B; []SEMI MF1388; []SEMI MF1535; []JEIDA 53; []JIS H604; []DIN 50440; []Other						
3. CHEMICAL CHARACTERISTICS									
	3.1	Oxygen Concentration	Nominal [] $\pm$ Tolerance [] ; [] $\times 10^{17} \text{ cm}^{-3}$; []ppma					100010	
		Calibration Factor	[]SEMI MF1188; []ASTM F121(79); []ASTM F121(83); [] JEIDA 61; []DIN 50438/1; []Other						
		Measurement Method	IR (Interstitial): [] SEMI MF1188; [] SEMI MF1619; [] JEIDA 61; [] DIN 50438-1 SIMS (Total): [] SEMI MF1366 []GFA (Total)						
	3.2	Radial Oxygen Variation	Not greater than []%					100011	
		Measurement Position	SEMI MF951 Plan []A, []B, []B1, []C, []D; []Other:						
		Calculation Method	SEMI F951 Plan []A, []B, []B1, []C, []D; [] Other:						
	3.3	Carbon Concentration	Not greater than [] [] ppma; [] $\times 10^{16} \text{ cm}^{-3}$					100012	
		Measurement Method	[]SEMI MF1391; JEIDA 56; []DIN 50438/2; []Other:						
	3.4	Boron Concentration in Heavily Doped n-type Si	Not greater than [] ppba					100013	
4. STRUCTURAL CHARACTERISTICS									
	4.1	Dislocation Etch Pit Density	[]Not greater than []/cm ²					100014	
	4.2	Slip	[]None []Other					100015	
	4.3	Lineage	[]None []Other					100016	
	4.4	Twin	[]None []Other					100017	
	4.5	Swirl	[]Not greater than []% of wafer area					100018	
	4.6	Shallow Pits	Not greater than []/cm ²					100019	
	4.7	Oxidation Induced Stacking Faults (OSF)	Not greater than []/cm ²					100020	
		Test Cycle	ASTM F 416 Cycle-[]1 []2 []3; [] SEMI MF 1727; []Other:						
	4.8	Oxide Precipitates (BMD)	Range: [] to [] Unit: [] cm ² [] cm ³					100021	
		Test Cycle	SEMI MF1239 []A, []B; [] Other:						
	4.9	Interstitial Oxygen Reduction (ΔO_i)	Range: [] to [] []ppma, [] $\times 10^{17} \text{ cm}^{-3}$					100162	
		Test Cycle	SEMI MF1239 []A, []B; [] Other:						
5. WAFER PREPARATION CHARACTERISTICS									
	5.1	Wafer ID Marking	[]None; []SEMI M12; []SEMI M13; []SEMI T1; []SEMI T2; [] SEMI T7; []Other:					100022	

	5.2	Front Surface Thin Film(s) Appl	[]None []Description:					100023	
	5.3	Denuded Zone	[]None []Description:					100024	
	5.4	Extrinsic Gettering Treatment	[]None []Description:					100025	
	5.5	Backseal	[]None []Description:					100026	
	5.6	Annealing	[]None []Description:					100027	
6. MECHANICAL CHARACTERISTICS									
THE ITEMS LISTED IN THIS SECTION MAY BE									
	6.01	[] Specified According to SEMI M1						100028	
OR SPECIFIED INDIVIDUALLY									
◆	6.1	Diameter ¹	Nominal [] ± Tolerance [] mm					100029	
◆	6.2	Primary Flat Length/Diameter Notch Dimensions ¹	[]SEMI M1.____; []Other: __mm					100030	
◆	6.3	Primary Flat/Notch Orientation ¹	[]SEMI M1.____; []Other: _____					100031	
◆	6.4	Secondary Flat Length ¹	[]SEMI M1.____; []Other: __mm; []None					100032	
◆	6.5	Secondary Flat Location ¹	[]SEMI M1.____; []Other: ____; []None					100033	
◆	6.6	Edge Profile ¹	[]SEMI Standard []Other: _____					100034	
◆	6.7	Thickness ¹	Nominal [] ± Tolerance [] μm					100035	
		Method	[]SEMI MF533; []SEMI MF1530; []JIS H 611; []DIN 50441/1; []Other: _____						
	6.8	Thickness Variation (TTV) ¹	[]SEMI M1.____; []Other: [] μm					100036	
		Measurement Position	[]SEMI MF533; []SEMI MF657; []SEMI MF1530; []JIS H 611; []DIN 50441/1; []Other: _____						
◆	6.9	Surface Orientation	[]0.00 ± 0.50; []2.50 ± 0.50; []4.00 ± 0.50; []Other: _____					100037	
		Method	[]SEMI MF26; []JEIDA 18; []DIN 50433; []Other: _____						
	6.10	Bow ¹	[]SEMI M1.____; []Other: __μm					100038	
		Method	[]SEMI MF534; []JIS H 611; []Other: _____						
	6.11	Warp ¹	[]SEMI M1.____; []Other: __μm						
		Method	[]SEMI MF657; []SEMI MF1390; []Other: _____					100039	SEMI MF657
								100040	SEMI MF1390
	6.12	Sori	[]____μm					100041	
		Method	[]SEMI MF1451; []JEIDA 43						
	6.13	Flatness/Global	Acronym: ² [] [] [] [] [] Value: [] μm					100042	
		Method	[]SEMI MF1530; []DIN 50441/3; []Other: _____						

6.14	Flatness/Site	Acronym: ² [] [] [] [] Value: [] μ m Site Size ____ $\times$ ____ mm Total Sites ____ % Usable Area ____ [] Include partial sites [] Offset: x = [] mm, y = [] mm					100043 SF3R 100044 SF3D 100045 SFLR 100046 SFLD 100047 SFQR 100048 SFQD 100049 SBIR 100050 SBID 100221 SFSD
6.15	Fixed Quality Area	Value: [] mm dia					100164
7. FRONT SURFACE CHEMISTRY							
7.1	Surface Metal Contamination						
	Sodium	[] Not greater than [] atoms/cm ² ; [] Other					100051
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1617 (SIMS); [] Other: _____					
	Aluminum	[] Not greater than [] atoms/cm ² ; [] Other					100052
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1617 (SIMS); [] Other: _____					
	Potassium	[] Not greater than [] atoms/cm ² ; [] Other					100053
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1617 (SIMS); [] SEMI M33 (TXRF); [] Other: _____					
	Chromium	[] Not greater than [] atoms/cm ² ; [] Other					100054
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] SIMS; [] Other: _____					
	Iron	[] Not greater than [] atoms/cm ² ; [] Other					100055
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] SEMI MF1617 (SIMS); [] Other: _____					
	Nickel	[] Not greater than [] atoms/cm ² ; [] Other					100056
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] Other: _____					
	Copper	[] Not greater than [] atoms/cm ² ; [] Other					100057
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] Other: _____					
	Zinc	[] Not greater than [] atoms/cm ² ; [] Other					100058
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] Other: _____					
	Others (List Separately)						
		[] Not greater than [] atoms/cm ² ; [] Other					100059
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] SIMS; [] Other: _____					
		[] Not greater than [] atoms/cm ² ; [] Other					100060
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] SIMS; [] Other: _____					
		[] Not greater than [] atoms/cm ² ; [] Other					100061
	Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] SIMS; [] Other: _____					
		[] Not greater than [] atoms/cm ² ; [] Other					100062

		Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] SIMS; [] Other: _____							
			[] Not greater than [] atoms/cm ² ; [] Other					100063		
		Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] SIMS; [] Other: _____							
			[] Not greater than [] atoms/cm ² ; [] Other					100064		
		Method	[] ICP/MS; [] JAAS; [] SEMI MF1526 (TXRF); [] SEMI M33 (TXRF); [] SIMS; [] Other: _____							
	7.2	Surface Organics	[] Not greater than [] ngrams/cm ²					100065		
		Method	[] SEMI MF1982; [] Other: _____							
8. FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS										
THE ITEMS LISTED IN THIS SECTION MAY BE										
	8.01	[] Specified According to SEMI M1 Table 1							100066	
OR SPECIFIED INDIVIDUALLY										
	8.1	Scratches ³	[] SEMI M1 Table 1 [] Other: _____					100067		
	8.2	Pits ³	[] SEMI M1 Table 1 [] Other: _____					100068		
	8.3	Haze ³	[] SEMI M1 Table 1 [] Other: _____					100069		
	8.4	Localized Light Scatterers (LLS) ³	[] SEMI M1 Table 1 [] Other: Size: [] μm Count: ≤ [] Size: [] μm Count: ≤ [] Size: [] μm Count: ≤ [] Size: [] μm Count: ≤ [] Size: [] μm Count: ≤ []					100070 100071 100072 100073 100074 100075 100076 100077 100078 100079 100080 100081 100082 100083 100084 100085 100086 100087 100088 100089 100090	≥0.50 μ ≥0.30 μ ≥0.20 μ ≥0.19 μ ≥0.18 μ ≥0.17 μ ≥0.16 μ ≥0.15 μ ≥0.14 μ ≥0.13 μ ≥0.12 μ ≥0.11 μ ≥0.10 μ ≥0.09 μ ≥0.08 μ ≥0.07 μ ≥0.06 μ ≥0.05 μ ≥0.04 μ ≥0.03 μ ≥0.02 μ	
		Method	[] SEMI MF523; [] SEMI MF1620; [] JIS H 614; [] JEIDA 24; [] Other: _____							
	8.5	Contamination/Area ³	[] SEMI M1 Table 1 [] Other: _____					100091		
	8.6	Edge Chips ³	[] SEMI M1 Table 1 [] Other: _____					100092		
	8.7	Edge Cracks ³	[] SEMI M1 Table 1 [] Other: _____					100093		
	8.8	Cracks, Crow's Feet ³	[] SEMI M1 Table 1 [] Other: _____					100094		
	8.9	Craters ³	[] SEMI M1 Table 1 [] Other: _____					100095		
	8.10	Dimples ³	[] SEMI M1 Table 1 [] Other: _____					100096		
	8.11	Grooves ³	[] SEMI M1 Table 1 [] Other: _____					100097		
	8.12	Mounds ³	[] SEMI M1 Table 1 [] Other: _____					100098		
	8.13	Orange Peel ³	[] SEMI M1 Table 1 [] Other: _____					100099		
	8.14	Saw Marks ³	[] SEMI M1 Table 1 [] Other: _____					100100		
	8.15	Dopant Striation Rings	[]					100101		