SEMI M18-1105
GUIDE FOR DEVELOPING SPECIFICATION FORMS FOR ORDER ENTRY OF SILICON WAFERS

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NOTICE: This document was completely rewritten in its entirety November 2005.

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1 Purpose

1.1 Silicon technology underlies the integrated circuit and device industry. Silicon wafers are the basis for most integrated circuits and devices used in electronic equipment. It is very useful to have common forms that include the parameters that should be included in the specifications for various kinds of silicon wafer products. This guide indicates how to develop such a form for inclusion in the appropriate specification and how the various forms can work together in preparing order entry information for the various silicon wafer products.

2 Scope

2.1 This guide covers the methodology for developing specification forms for order entry including

- how to identify form sections, form columns, and form headings,
- instructions for line format and how to number items,
- how to add new items appropriate to a given wafer product to the form,
- how to reference new items from another section of the form not within the specification
- method for maintaining the Electronic Data Interchange (EDI) codes used in SEMI T6 to identify the kind of data being reported in the EDI message, and
- method to request new additions from a group responsible for a section of the form for order entry that contains essential parameters for the particular wafer but is not included in the order form for that wafer's specifications.

2.2 This guide lists the sections of the order entry form and shows where they appear and how they are used.

2.3 This guide provides information on how to construct the ordering information section for silicon wafer specifications.

2.4 This guide also lists the Electronic Data Interchange (EDI) codes used in SEMI T6 to identify the kind of data being reported in the EDI message.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M6 — Specification for Silicon Wafers for Use as Photovoltaic Solar Cells

SEMI M8 — Specification for Polished Monocrystalline Silicon Test Wafers

SEMI M16 — Specification for Polycrystalline Silicon

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M34 — Guide for Specifying SIMOX Wafers

SEMI M38 — Specification for Polished Reclaimed Silicon Wafers

SEMI M41 — Specification of Silicon-on-Insulator (SOI) for Power Device/ICs

SEMI M47 — Specification for Silicon-on-Insulator (SOI) Wafers for CMOS LSI Applications

SEMI M57 — Guide for Specifying Silicon Annealed Wafers

SEMI M59 — Terminology for Silicon Technology

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SEMI M61— Specification for Silicon Epitaxial Wafers with Buried Layers

SEMI M62 — Specifications for Silicon Epitaxial Wafers

SEMI T6 — Procedure and Format for Reporting of Test Results by Electronic Data Interchange (EDI)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Terms, symbols, and acronyms associated with silicon wafers and silicon technology are listed and defined in SEMI M59.

5 Development of Silicon Wafer Specification Format for Order Entry

5.1 *Location* — Each part of the silicon wafer specification format for order entry appears in only one specification.

5.1.1 Parts 1 and 2, General Information and Polished Wafer or Substrate, respectively, appear in SEMI M1.

5.1.2 Part 3, Epitaxial Wafer, will appear in the common epitaxial wafer specification (see Notes 1 and 2).

5.1.3 Part 4, Epitaxial Wafer with Buried Layer, appears in SEMI M61.

5.1.4 Part 5, Annealed Wafer, appears in SEMI M57.

5.1.5 Part 6, SOI Wafer, appears in this guide until SOI specifications are revised to include it.

5.2 *Developmental Responsibility* — Each international or regional task force responsible for developing the specifications for a certain silicon wafer product is responsible for developing the necessary part of the silicon wafer specification format for order entry, unless the part appropriate to that wafer product appears already in another specification.

5.2.1 For example, specifications for test, premium, and reclaimed wafers use only Parts 1 and 2, which appear in SEMI M1.

5.2.2 If there are several specifications for similar silicon wafer products (for example, several specifications for SOI wafers), the task forces responsible for such specifications must cooperate with each other to identify and use a single location for the part of the silicon wafer specification format for order entry for that wafer product.

5.3 The title of the table that includes a part of the silicon wafer specification format for order entry is in table title format as follows:

Table x. Silicon Wafer Specification Format for Order Entry, Part #, Wafer Product

For example, the title of the table for epitaxial wafers is as follows:

Table 1. Silicon Wafer Specification Format for Order Entry, Part 3, Epitaxial Wafer

5.4 Structure of the Table Containing a Part of the Silicon Wafer Specification Format for Order Entry

5.4.1 Each part of the table is printed in landscape, not portrait, format with a width of 9 in. or 230 mm.

5.4.2 Each part of the table has five columns. The column headers (using table header format but in all caps) and their widths are given in Table 1. Each cell in the table has 0.02 in. or 0.5 mm margins. Column headers appear at the top of each page of the table.

Table 1 Column Headers and Widths for Each Part of the Silicon Wafer Specification Format for Order Entry

Column Title	*Column Width*
ITEM	(a) 0.25 in. or 7 mm, (b) 0.5 in. or 13 mm, (c) 1.65 in. or 42 mm
SPECIFICATION	3.3 in. or 84 mm
MEASUREMENT METHOD	3.3 in. or 84 mm

5.4.3 Text entries are in 9 pt Times Roman type using table text format.

5.4.4 The first column is divided into three sub-columns as follows:

5.4.4.1 Sub-column (a) contains a symbol ♦ for each item that is required in order to minimally specify a silicon wafer, a symbol ➲ for each item specified in accordance with a standard wafer category (in which case a choice for each item need not be made individually, and/or a symbol ➢ for each of a group of items taken from a table in the specification (also in which case a choice for each item need not be made individually).

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5.4.4.2 Sub-column (b) contains the item number constructed as follows: Part number, hyphen, section number, period, and item number within the section (e.g., 2-1.9). In certain circumstances the item number is further subdivided so that there is an additional period and number at the end (e.g., 2-7.1.7). The item number is unique to the item and is used to position it in the specification as well as to identify the EDI code.

5.4.4.3 Sub-column (c) contains the name of the item.

5.4.5 The second column provides a means for indicating the specification. Choices or values are indicated by the symbol [ ]. If there are several choices, the appropriate one should be checked; if values are allowed, they should be filled in with numbers or other symbols as appropriate.

5.4.6 The third column provides the standardized or other measurement methods as appropriate. Again where there are choices, the appropriate one should be checked.

5.4.6.1 If several different standard test methods for an item are commonly used within a region, it is particularly important that the applicable method of test be identified in the purchase order.

5.4.6.2 If no method of test is specified in the purchase order and if standard test methods from different geographic regions are available, the default method shall be a method in common usage for the region of the purchaser of the wafer.

5.4.6.3 If no standard test method for an item is available, the test procedure to be used must be agreed upon between supplier and customer.

5.4.7 *Sections* — Groups of related items are combined into sections within each part of the Silicon Wafer Specification Format for Order Entry. The grouping is under the control of the task force with developmental responsibility, but it is generally convenient to make the groupings similar to the sections already in place.

5.4.7.1 The header for each section is placed in a merged cell comprised of all cells across the width of the table

5.4.7.2 The header is in bold face type and begins with the part number followed by a hyphen, the section number, a period, a space and the section title in all caps, ending without a period.

5.4.8 If sub-column (a) contains a symbol as described in ¶5.4.4.1, the use of this symbol is described in the cell with the section header. See the headers of sections 1, 6, 8, and 9 of Table 1 of SEMI M1 for examples of such descriptions.

5.4.9 An example of the Silicon Wafer Specification Format for Order Entry, showing the first page of the information from Parts 1 and 2 in SEMI M1 at two-thirds scale, is given in Figure 1.

5.5 *Table Footnotes* — Table footnotes can be included where appropriate using the # sign followed by a numeral format defined in the current edition of the SEMI Standards Editorial Guidelines.

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Part 1 General Information

ITEM	*INFORMATION*	*Date:*
Customer Name		
Purchase Order Number		
Line Number		
Item Number		
General Specification Number		
Revision Level		
Part Number/Revision		

Part 2 Polished Wafer or Substrate

ITEM			*SPECIFICATION*	*MEASUREMENT METHOD*
2-1. GENERAL CHARACTERISTICS (*Note that ♦ indicates a required item for which a value or choice* ***must*** *be indicated in order to minimally specify a silicon wafer.*)				
♦	2-1.1	Growth Method	[ ]Cz; [ ]FZ; [ ]MCz; [ ]Supplier option of Cz or MCz	
	2-1.2	Use of Refined Polysilicon	[ ]Permitted; [ ]Not permitted	
♦	2-1.3	Crystal Orientation	[ ](100); [ ](111); [ ](110); [ ]Other: (specify) ( )	[ ]SEMI MF26 (X-Ray); [ ] SEMI MF26 (Optical); [ ]JEITA EM-3501; [ ]DIN 50433/1; [ ]DIN 50433/2; [ ]DIN 50433/3; [ ]Other: (specify)_____
♦	2-1.4	Conductivity Type	[ ]*p;* [ ]*n*	[ ]SEMI MF42; [ ]JIS H 0607; [ ]DIN 50432; [ ]Other: (specify)_____
♦	2-1.5	Dopant	[ ]B; [ ]P; [ ]Sb; [ ]As; [ ]Neutron Transmutation Doped; [ ]Other: (specify) _____	
	2-1.6	Nominal Edge Exclusion[#1] (See Figure 1)	[ ]2 mm; [ ]3 mm; [ ]5 mm; [ ]Other: (specify)_____mm	
	2-1.7	Co-dopant in Crystal	[ ]None; [ ]Nitrogen; [ ]Carbon; [ ]Nitrogen and Carbon; [ ]Argon; [ ]Other: (specify)_____	
♦	2-1.8	Wafer Surface Orientation (with respect to crystal orientation, see item 2-1.3)	[ ]On-orientation: [ ]0.00° ± 1.00°; [ ]0.00° ± _____° [ ]Off-orientation: [ ]0.6° ± 0.4° [ ]2.50° ± 0.50°; [ ]4.00° ± 0.50°; [ ]_____° ± _____°	[ ]SEMI MF26 (X-Ray); [ ] SEMI MF26 (Optical); [ ]JEITA EM-3501; [ ]DIN 50433/1; [ ]DIN 50433/2; [ ]DIN 50433/3; [ ]Other: (specify)_____
	2-1.9	Orthogonal Misorientation (See Figure 2)	[ ] ±5° max; [ ]Other: ±[ ]°, max	

Figure 1
Example Showing Part 1 and Beginning of Part 2 of the Silicon Wafer Specification Format for Order Entry

6 Ordering Information

6.1 Table 2 identifies the parts of the Silicon Wafer Specification Format for Order Entry to be used in specifying the requirements for the particular silicon wafer product being specified.

Table 2 Parts of the Silicon Wafer Specification Format for Order Entry Used in Specifying Various Silicon Wafer Products

Silicon Wafer Product	*Starting Material from Part*	*Finishing Information from Part*
Polished Wafer (or Substrate)		1, 2
Test Wafer		1, 2
Premium Wafer		1, 2
Reclaimed Wafer		1, 2
Epitaxial Wafer	1, 2	3
Epitaxial Wafer with Buried Layer	1, 2, 3	4
Annealed Wafer	1, 2	5
SOI Wafer	1, 2, (3)	6

6.2 The first paragraph of the ordering information section should refer to the required items from Parts 1 and 2 (and, if required, Part 3) of the Silicon Wafer Specification Format for Order Entry, as follows:

6.2.1 Purchase orders for (indicate silicon wafer product) furnished to these specifications shall include the appropriate order entry information from Silicon Wafer Specification Format for Order Entry, Parts 1 and 2, Table 1 in SEMI M1 and if required from Part 3, Table 1 of SEMI Myy.

6.2.2 All information in Part 1, General Information, and the following items from Part 2, Polished Wafer or Substrate, shall be included, after which there follows a bulleted list of items to be included.

6.2.3 Other items from Part 2, Polished Wafer or Substrate, can be included as needed.

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6.2.4 In addition, the purchase order must indicate the test method to be used in evaluating each of the specified items for which alternate test procedures exist.

6.3 Where necessary, the same information should be given for items from Part 3.

6.4 The next paragraph of the ordering information section should refer to the required items from the Parts of the Silicon Wafer Specification Format for Order Entry, appropriate to the finishing information for the silicon wafer product being specified, as follows (see Table 2):

6.4.1 Purchase orders for (indicate silicon wafer product) furnished to these specifications shall also include the items with a ♦ symbol in the left-most column of Table 1, Silicon Wafer Specification Format for Order Entry, Part #. There follows a bulleted list of items to be included.

6.4.2 In addition, the purchase order must indicate the test method to be used in evaluating each of the specified items for which alternate test procedures exist.

6.5 The following items must also be included in the purchase order:

6.5.1 Lot acceptance procedures.

6.5.2 Certification (if required).

6.5.3 Packing and shipping container labeling requirements.

6.6 Examples of the various paragraphs can be found in the specifications listed in ¶5.1.

7 Electronic Data Interchange Codes

7.1 The EDI codes used in SEMI T6 to identify the type of data being reported in the EDI message are listed here in Appendix 1 together with a listing of old and new item numbers for the various parts of the Silicon Wafer Specification Format for Order Entry. New codes are assigned in numerical order as they are requested.

7.2 A task force responsible for developing a part of the Silicon Wafer Specification Format for Order Entry, can request additional EDI codes from the leaders of the Specification Order Form Task Force. Such requests will be acted upon at the next meeting of this latter task force. It is desirable that the request be made at the same time as the specification containing the applicable part of the Silicon Wafer Specification Format for Order Entry is being drafted for letter ballot to modify the specification to include the new item or items for which additional EDI codes are needed. The Specification Order Form Task Force will act upon the request at its next meeting, regardless of the region where this meeting is scheduled to occur. Because the maintenance of the list of EDI codes is an administrative function, no balloting is required and the codes can be assigned immediately upon consideration by the task force.

8 New Parts of the Silicon Wafer Specification Format for Order Entry

8.1 As new silicon wafer products are developed, it may be necessary to add additional parts to the Silicon Wafer Specification Format for Order Entry. Numbers for such parts can be requested from the leaders of the Specification Order Form Task Force. Numbers for new parts will be assigned and recorded by the latter task force at its next meeting. At such time as the new part is completed, EDI codes for the items included should be requested by the leaders of the task force responsible for development of the part in accordance with the procedures in §7.

9 Part 6 of the Silicon Wafer Specification Format for Order Entry

9.1 Until the SOI wafer specifications are revised to include Part 6 of the Silicon Wafer Specification Format for Order Entry, that part continues to be included in Appendix 2 of this Guide as Table A2-1.

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APPENDIX 1
ELECTRONIC DATA INTERCHANGE CODES

NOTICE: The material in this appendix is an official part of SEMI M18 and was approved by full letter ballot procedures on September 8, 2005.

A1-1 Introduction

A1-1.1 This appendix provides two listings of the Electronic Data Interchange Codes used in connection with SEMI T6. Where necessary for clarity additional sub-parameters are listed. These sub-parameters identify a specific measurement technique to be used or parameter range to be covered.

A1-1.1.1 The first, in Table A1-1, is in the order of the items in the various parts of the Silicon Wafer Specification Format for Order Entry. This table contains the original numbers as well as the new numbers that were assigned to the various items in the 2004 and 2005 revisions of the format. This table also includes the section headers in the various parts of the format. For information only, this table shows deletions and additions from the entries in the 0704 edition of SEMI 18 by strikeout and underline, respectively.

A1-1.1.2 The second, in Table A1-2, lists the EDI codes in numerical order. This table does not include the section headers. It also shows deletions and additions from the entries in the 0704 edition of SEMI 18 by strikeout and underline, respectively.

Table A1-1 EDI Codes in Item Number Order Including Section Headings

Item #	*Orig Line #*	*Item*	*EDI Code ID*	*Sub Param ID*
2-1. GENERAL CHARACTERISTICS				
2-1.1	1.1	Growth Method	100001	
2-1.2		Use of Refined Silicon		
2-1.3	1.2	Crystal Orientation	100002	
2-1.4	1.3	Conductivity Type	100003	
2-1.5	1.4	Dopant	100004	
2-1.6	1.5	Nominal Edge Exclusion	100005	
2-1.7		Co-dopant in Crystal		
2-1.8	6.9	Surface Orientation	100037	
2-1.9		Orthogonal Misorientation		
2-2. ELECTRICAL CHARACTERISTICS				
2-2.1	2.1	Resistivity	100006	
2-2.2	2.2	Radial Resistivity Variation (RRG)	100007	
2-2.3	2.3	Resistivity Striations	100008	
2-2.4	2.4	Minority Carrier Lifetime	100009	
2-3. CHEMICAL CHARACTERISTICS				
2-3.1	3.1	Oxygen Concentration	100010	
2-3.2	3.2	Radial Oxygen Variation	100011	
2-3.3	3.3	Carbon Concentration (Background)	100012	
2-3.4	3.4	Boron Concentration in Heavily Doped *n*-type Si	100013	
2-3.5		Total Bulk Iron Content		
2-4. STRUCTURAL CHARACTERISTICS				
2-4.1	4.1	Dislocation Etch Pit Density	100014	
2-4.2	4.2	Slip	100015	
2-4.3	4.3	Lineage	100016	
2-4.4	4.4	Twin Boundary	100017	
2-4.5	4.5	Swirl	100018	
2-4.6	4.6	Shallow Pits	100019	

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Item #	Orig Line #	Item	EDI Code ID	Sub Param ID
2-4.7	4.7	Oxidation Induced Stacking Faults (OSF)	100020	
2-4.8	4.8	Oxide Precipitates (BMD)	100021	
2-4.9	4.9	Interstitial Oxygen Reduction (ΔO_i)	100162	
2-4.10	10.1	Bulk defects by X-ray topography	100169	
2-5. WAFER PREPARATION CHARCTERISTICS				
2-5.1	5.1	Wafer ID Marking	100022	
2-5.2	5.2	Front Surface Thin Film(s)	100023	
2-5.3	5.3	Denuded Zone	100024	
2-5.4	5.4	Extrinsic Gettering Treatment	100025	
2-5.5	5.5	Backseal	100026	
2-5.6	5.6	Annealing	100027	
2-5.7		Edge Surface Condition		
2-5.8		Back Surface Condition		
2-6. DIMENSIONAL CHARACTERISTICS				
	6.01	Dimensions Specified According to Polished Wafer Category 1.___	100028	
2-6.1	6.1	Diameter	100029	
2-6.2	6.2	Fiducial Dimensions	100030	
2-6.3	6.3	Primary Flat/Notch Orientation	100031	
2-6.4	6.4	Secondary Flat Length	100032	
2-6.5	6.5	Secondary Flat Location	100033	
2-6.6	6.6	Edge Profile	100034	
2-6.7	6.7	Thickness	100035	
2-6.8	6.8	Thickness Variation (TTV)	100036	
2-6.9	6.10	Bow	100038	
2-6.10	6.11	Warp	100039	SEMI MF657
2-6.10	6.11	Warp	100040	SEMI MF1390
2-6.11	6.12	Sori	100041	
2-6.12	6.13	Flatness, Global	100042	
2-6.13	6.14	Flatness, Site	100043	SF3R
2-6.13	6.14	Flatness, Site	100044	SF3D
2-6.13	6.14	Flatness, Site	100045	SFLR
2-6.13	6.14	Flatness, Site	100046	SFLD
2-6.13	6.14	Flatness, Site	100047	SFQR
2-6.13	6.14	Flatness, Site	100048	SFQD
2-6.13	6.14	Flatness, Site	100049	SBIR
2-6.13	6.14	Flatness, Site	100050	SBID
2-6.13	6.14	Flatness, Site	100160	SFSR
2-6.13	6.14	Flatness, Site	100221	SFSD
		Deleted Item	100164	
2-7. FRONT SURFACE CHEMISTRY				
2-7.1.1	7.1	Surface Metal Contamination – Sodium	100051	
2-7.1.2	7.1	Surface Metal Contamination – Aluminum	100052	
2-7.1.3	7.1	Surface Metal Contamination – Potassium	100053	
2-7.1.4	7.1	Surface Metal Contamination – Chromium	100054	
2-7.1.5	7.1	Surface Metal Contamination – Iron	100055	

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Item #	Orig Line #	Item	EDI Code ID	Sub Param ID
2-7.1.6	7.1	Surface Metal Contamination – Nickel	100056	
2-7.1.7	7.1	Surface Metal Contamination – Copper	100057	
2-7.1.8	7.1	Surface Metal Contamination – Zinc	100058	
2-7.1.9		Surface Metal Contamination – Calcium		
2-7.2.1	7.1	Surface Metal Contamination – (Producer-User Defined Metal)	100059	
2-7.2.2	7.1	Surface Metal Contamination – (Producer-User Defined Metal)	100060	
2-7.2.3	7.1	Surface Metal Contamination – (Producer-User Defined Metal)	100061	
2-7.2.4	7.1	Surface Metal Contamination – (Producer-User Defined Metal)	100062	
2-7.2.5	7.1	Surface Metal Contamination – (Producer-User Defined Metal)	100063	
2-7.2.6	7.1	Surface Metal Contamination – (Producer-User Defined Metal)	100064	
2-7.3	7.2	Surface Organics	100065	
2-8. FRONT SURFACE VISUAL INSPECTION				
	8.01	Specified According to SEMI M1 Table 10	100066	
2-8.1	8.1	Scratches – Macro	100067	
2-8.2		Scratches – Micro		
2-8.3	8.2	Pits	100068	
2-8.4	8.3	Haze	100069	
2-8.5	8.4	Localized Light Scatterers (LLS)	100070	≥0.50 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100071	≥0.30 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100072	≥0.20 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100073	≥0.19 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100074	≥0.18 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100075	≥0.17 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100076	≥0.16 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100077	≥0.15 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100078	≥0.14 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100079	≥0.13 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100080	≥0.12 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100081	≥0.11 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100082	≥0.10 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100083	≥0.09 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100084	≥0.08 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100085	≥0.07 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100086	≥0.06 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100087	≥0.05 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100088	≥0.04 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100089	≥0.03 µm
2-8.5	8.4	Localized Light Scatterers (LLS)	100090	≥0.02 µm
2-8.6	8.5	Contamination/Area	100091	
2-8.7	8.6	Edge Chips and Indents	100092	
2-8.8	8.7	Edge Cracks	100093	
2-8.9	8.8	Cracks, Crow's Feet	100094	
2-8.10	8.9	Craters	100095	
2-8.11	8.10	Dimples	100096	
2-8.12	8.11	Grooves	100097	

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