

SEMI M2-1103

SPECIFICATION FOR SILICON EPITAXIAL WAFERS FOR DISCRETE DEVICE APPLICATIONS

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NOTICE: This Document is no longer supported by the global technical committee. It has been replaced by SEMI M62.

1 Purpose

1.1 This Specification defines silicon epitaxial wafer requirements for discrete semiconductor device manufacture. It is restricted to wafers with device feature sizes in excess of 1 μm or wafers with epi layers thicker than 25 μm . By defining inspection procedures and acceptance criteria, suppliers and consumers may uniformly define product characteristics and quality requirements.

2 Scope

2.1 This Specification covers characteristics of both the substrate (through reference to SEMI M1) and the epitaxial layer including handling and packaging.

2.2 This Specification is specifically directed to silicon homoepitaxial deposits thicker than 25 μm on homogeneous silicon substrates or similar epitaxial wafers that are to be used to make discrete devices. Specifications for silicon epitaxial wafers with greater uniformity and more stringent surface defect criteria are given in SEMI M11.

2.3 The primary standardized properties set forth in this specification relate to physical, electrical, and surface defect parameters.

2.4 A complete purchase specification requires that additional physical properties be specified along with suitable test methods for their measurement. SEMI M18 may be used for this purpose.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards and Safety Guidelines

SEMI M1 — Specification for Polished Monocrystalline Silicon Wafers

SEMI M11 — Specifications for Silicon Epitaxial Wafers for Integrated Circuit (IC) Applications

SEMI M17 — Specification for a Universal Wafer Grid

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI MF95 — Test Method for Thickness of Epitaxial Layers of Silicon on Substrates of the Same Type by Infrared Reflectance

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, and Ion-Implanted Layers Using an Inline Four-Point Probe with the Single Configuration

SEMI MF398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wavelength of the Plasma Resonance Minimum

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

SEMI MF525 — Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF672 — Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe

SEMI MF723 — Practice for Conversion between Resistivity and Dopant Density for Boron-Doped and Phosphorus-Doped Silicon

SEMI MF1241 — Terminology of Silicon Technology

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafer by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1393 — Test Method for Determining Net Carrier Density in Silicon Wafers by Miller Feedback Profiler Measurements with a Mercury Probe

SEMI MF1726 — Guide for Analysis of Crystallographic Perfection of Silicon Wafers

3.2 Other Standards¹

ANSI/ASQ Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Many terms relating to silicon technology are defined in SEMI MF1241.

4.2 Descriptions of other epitaxial wafer defects covered in Table 1 are given in SEMI MF154.

4.3 Other terms are defined as follows:

4.3.1 *autodoping, of an epitaxial layer* — incorporation of dopant originating from the substrate into the epitaxial layer. Also called *self-doping*.

NOTE 1: Sources of autodoping can be the back and front surfaces and edges of the substrate, other substrates in the reactor, the susceptor, or other parts of the deposition assembly.

4.3.2 *chemical vapor deposition, in semiconductor technology* — a process in which a controlled chemical reaction produces a thin surface film.

NOTE 2: Epitaxial growth is an example of a special case of chemical vapor deposition (CVD).

4.3.3 *edge crown* — the difference between the surface elevation 3.2 mm (1/8 in.) from the edge of the wafer and the elevation at the wafer edge.

4.3.4 *effective layer thickness, of an epitaxial layer* — the depth from the front surface in which the net carrier density is within the specified limits.

4.3.5 *epi profile slope, of an epitaxial layer* — the difference between the net carrier density at 0.75 of the layer thickness and the net carrier density at 0.25 of the layer thickness divided by one-half the layer thickness:

$$\text{epi profile slope} = \frac{N_{0.75t} - N_{0.25t}}{0.5t} \quad (1)$$

where:

N = net carrier density, cm^{-3} , and

t = layer thickness, μm .

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