SEMI M20-0215 (Reapproved 0421)
PRACTICE FOR ESTABLISHING A WAFER COORDINATE SYSTEM

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NOTICE: This Document was reapproved with minor editorial changes.

1 Purpose

1.1 Processing systems now employed in advanced device manufacturing use aligning mechanisms to position the wafer rotationally and in *x*-*y* prior to processing. Many of these scan the wafer periphery and determine the geometric center of the wafer surface. This is most often seen on stepping aligners, to minimize the effects of wafer-to-wafer diameter variation in mixed aligner type fabs. Similar center-referencing subsystems are found on many characterization systems. The wafer coordinate system provides a method for referencing any other coordinate system, such as a site, pattern, or mapping array, to the physical geometry of the wafer surface.

1.2 If the points of the array lie on the front surface of the wafer, only the *x* and *y* (or *r* and θ) coordinates are relevant. It has become increasingly important in semiconductor material and device manufacturing to describe, in unambiguous terms, the position of a point on a wafer that automatic processing, test, or characterization equipment can recognize and locate. For example, characterization equipment needs to report the precise locations of defects and anomalies discovered in wafers before or after processing in order to relate the presence or absence of such defects and anomalies to device yield variations. The wafer coordinate system can be used to establish the coordinates of each point of interest, and, through transformation to the yield analysis coordinate system, relate them to the die yield map.

1.3 In response to these needs, this Practice defines a wafer coordinate system to facilitate the precise locating and reporting of points on the wafer surface. If the point or points lie above or below the surface, the *z*-coordinate must also be used. Because the zero point on the *z*-axis is application specific, this Practice treats the *x*-*y*-*z* (or *r*-θ-*z*) system separately from the surface coordinate system.

2 Scope

2.1 This Practice covers procedures for defining a wafer coordinate system for locating uniquely any point on a wafer surface using the wafer center as the origin and either Cartesian (*x*-*y*) or polar (*r*-θ) coordinates.

2.2 For unpatterned wafers, this wafer coordinate system can be used directly or in conjunction with a rectangular or polar overlay array.

2.3 This wafer coordinate system can also be used to locate the origins or other reference points of other coordinate systems used to define or report position data of site, die, or map arrays on the front or back surface of a patterned or unpatterned wafer. In this way, the array coordinate system may be referenced to the physical geometry of the wafer. Selected modes of application of the wafer coordinate system are given for information only in Related Information 1.

2.4 This Practice also covers procedures for defining a three-dimensional *x*-*y*-*z* (or *r*-θ-*z*) coordinate system for the wafer.

NOTICE: SEMI Standards and Safety Guidelines do not purport to address all safety issues associated with their use. It is the responsibility of the users of the Documents to establish appropriate safety and health practices, and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 Mask alignment conventions are not necessarily consistent with the wafer coordinate system.

3.2 In SEMI M1, the position of the secondary flat on silicon wafers is defined by the clockwise rotation from the primary flat. This is opposite to the convention used for the polar angle in the wafer coordinate system.

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3.3 Also in SEMI M1, the coordinate system for the edge profile template is, unlike the wafer coordinate system, edge referenced. Different coordinate systems are used for template-coordinate based and profile-parameter based edge profiles.

3.3.1 The template-coordinate based edge profile system defines the template with the x coordinate for the radial direction (positive from the wafer edge inward) and the y coordinate for the vertical direction (positive from the wafer surface toward the median plane of the wafer).

3.3.2 The profile-parameter based system defines the cross-section of the edge profile with the q coordinate for the radial direction (positive from the wafer edge inward) and the z coordinate for the vertical direction (positive along the perpendicular to the wafer median plane toward the front surface of the wafer).

3.4 In SEMI E5, the 'normal' position of the wafer is defined similarly to that in the wafer coordinate system; that is, the primary fiducial is downward and its bisector is the negative y-axis. However, the rotational position of the wafer is defined by its clockwise rotation from the 'normal' position, again opposite to the convention used for the polar angle in the wafer coordinate system. Further, in SEMI E5, the coordinate system axes do not rotate; the wafer rotates with respect to these axes. In the wafer coordinate system, the coordinate axes are referenced to the wafer itself, independent of the physical position of the wafer in space.

3.5 SEMI M12 and SEMI M13 specify the mark field location for 100 mm, 125 mm, or 150 mm diameter flatted wafers relative to the flat rather than the wafer center. Thus, the mark field location may vary with respect to the wafer center and the coordinates of the corners of the mark field location (in the wafer coordinate system) may vary from wafer to wafer. However, the mark field location for notched wafers 150, 200, and 300 mm in diameter is referenced to the wafer center.

3.6 There are some circumstances in which the front surface of an unpatterned wafer is not readily distinguished from the back surface.

4 Referenced Standards and Documents

4.1 *SEMI Standards and Safety Guidelines*

SEMI E5 — Specification for SEMI Equipment Communications Standard 2 Message Content (SECS-II)

SEMI M1 — Specification for Polished Single Crystal Silicon Wafers

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M17 — Guide for a Universal Wafer Grid

SEMI M59 — Terminology for Silicon Technology

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Acronyms, terms, and symbols related to silicon technology, including those used in this Practice, are listed and defined in SEMI M59.

6 Summary of Practice

6.1 *Front Surface Coordinate System*

6.1.1 The wafer is positioned with its front surface up.

6.1.2 The wafer center is located.

6.1.3 A right-handed Cartesian coordinate system is erected.

6.1.4 The primary fiducial is located to be in the negative y-direction.

6.1.5 Cartesian or polar coordinates (referenced to the positive x-axis) are chosen according to the intended application.

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